

SN74LV4066A Quadruple Bilateral Analog Switches

1 Features

- 1.65V to 5.5V V_{CC} operation
- Support mixed-mode voltage operation on all ports
- High on-off output-voltage ratio
- Low crosstalk between switches
- Individual switch controls
- Extremely low input current
- ESD protection exceeds JESD 22:
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 750-V Charged-Device Model (C101)

2 Applications

- [Telecommunications](#)
- [eCall](#)
- [Infotainment](#)

3 Description

This quadruple silicon-gate CMOS analog switch is designed for 1.65V to 5.5V V_{CC} operation.

These switches are designed to handle both analog and digital signals. Each switch permits signals with amplitudes up to 5.5V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

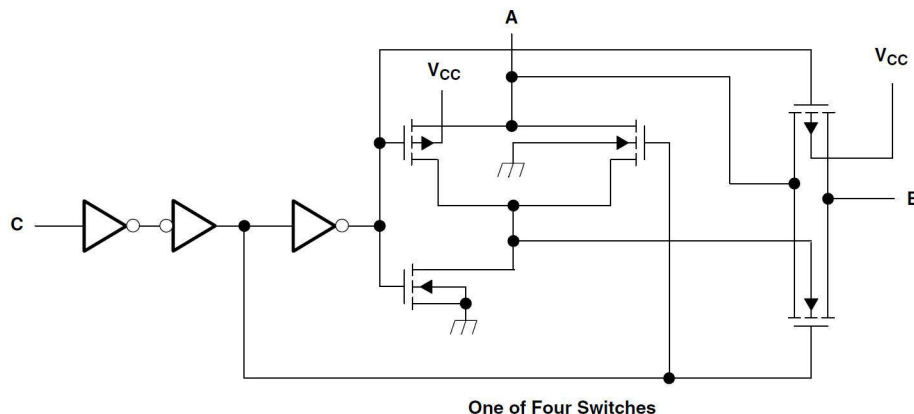
Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
SN74LV4066A	D (SOIC, 14)	8.65mm × 6mm
	PW (TSSOP, 14)	5mm × 6.4mm
	RGY (QFN, 14)	3.5mm × 3.5mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)



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4 Pin Configuration and Functions

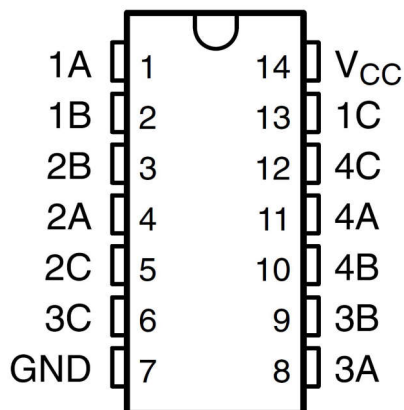


Figure 4-1. D or PW Package, 14-Pin SOIC or TSSOP (Top View)

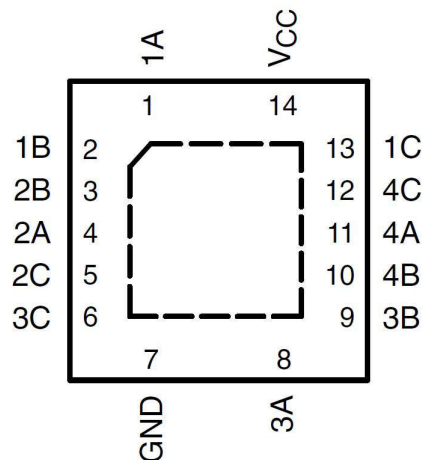


Figure 4-2. RGY Package, 14-Pin QFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I/O	Input/Output to switch channel 1
1B	2	I/O	Input/Output to switch channel 1
2B	3	I/O	Input/Output to switch channel 2
2A	4	I/O	Input/Output to switch channel 2
2C	5	I	Control line for channel 2. Switch is ON when control pin is high.
3C	6	I	Control line for channel 3. Switch is ON when control pin is high.
GND	7	—	Ground (0V) reference
3A	8	I/O	Input/Output to switch channel 3
3B	9	I/O	Input/Output to switch channel 3
4B	10	I/O	Input/Output to switch channel 4
4A	11	I/O	Input/Output to switch channel 4
4C	12	I	Control line for channel 4. Switch is ON when control pin is high.
1C	13	I	Control line for channel 1. Switch is ON when control pin is high.
V _{CC}	14	—	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between VDD and GND.
Thermal pad		—	It is recommended to tie the pad to GND for the best performance.

(1) Signal types: I = input, O = output, I/O = input or output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (3)}

			MIN	MAX	UNIT
V _{CC}	Supply voltage		−0.5	7.0	V
V _I	Logic input voltage range		−0.5	7.0	V
V _{IO}	Switch I/O voltage range ^{(2) (3)}		−0.5	V _{CC} + 0.5	V
I _{IK}	Logic input clamp current	V _I < 0	−20		mA
I _{IOK}	Switch path diode clamp current	V _{IO} < 0 or V _{IO} > V _{CC}	−50	50	mA
I _T	Switch continuous current	V _{IO} = 0 to V _{CC}		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature		−65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5V maximum

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information: SN74LV4066A

THERMAL METRIC ⁽¹⁾		SN74LV4066A			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.8	150.6	91.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.8	78.2	91.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.2	93.7	66.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	39.5	24.6	20.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	83.7	93.1	66.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	50.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		1.65		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 2V	1.5		5.5	V
		V _{CC} = 2.3V to 2.7V	V _{CC} × 0.7		5.5	
		V _{CC} = 3V to 3.6V	V _{CC} × 0.7		5.5	
		V _{CC} = 4.5V to 5.5V	V _{CC} × 0.7		5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 2V	0		0.5	V
		V _{CC} = 2.3V to 2.7V	0	V _{CC} × 0.3		
		V _{CC} = 3V to 3.6V	0	V _{CC} × 0.3		
		V _{CC} = 4.5V to 5.5V	0	V _{CC} × 0.3		
V _I	Logic control input voltage		0		5.5	V
V _{IO}	Switch input or output voltage		0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 2.3V to 2.7V			200	ns/V
		V _{CC} = 3V to 3.6V			100	
		V _{CC} = 4.5V to 5.5V			20	
T _A	Ambient temperature		–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.5 Electrical Characteristics (LV)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON}	ON-state switch resistance	I _T = 2mA, V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 6-1)	1.65V	25°C	60	150	Ω
				–40°C to 85°C		225	
				–40°C to 125°C		225	
			2.3V	25°C	38	180	
				–40°C to 85°C		225	
				–40°C to 125°C		225	
			3V	25°C	29	150	Ω
				–40°C to 85°C		190	
				–40°C to 125°C		190	
			4.5V	25°C	21	75	Ω
				–40°C to 85°C		100	
				–40°C to 125°C		100	

5.5 Electrical Characteristics (LV) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C		130	600	Ω
			–40°C to 85°C			700	
			–40°C to 125°C			700	
			25°C		143	500	
			–40°C to 85°C			600	
			–40°C to 125°C			600	
		25°C	3V		57	180	Ω
						225	
						225	
		25°C	4.5V		31	100	Ω
						125	
						125	
Δr _{ON}	Difference in ON-state resistance between switches	I _T = 2mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C		2.5		Ω
			–40°C to 85°C		3		
			–40°C to 125°C		3		
			25°C		3	30	
			–40°C to 85°C			40	
			–40°C to 125°C			40	
		25°C	3V		3	20	Ω
						30	
						30	
		25°C	4.5V		2	15	Ω
						20	
						20	
I _{IH} I _{IL}	Control input current	V _I = 5.5V or GND	25°C			0.1	μA
			–40°C to 85°C	0 to 5.5V		1	
			–40°C to 125°C			1	
I _{S(off)}	OFF-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 6-2)	25°C			±0.1	μA
			–40°C to 85°C	5.5V		±1	
			–40°C to 125°C			±1	
I _{S(on)}	ON-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 6-3)	25°C			±0.1	μA
			–40°C to 85°C	5.5V		±1	
			–40°C to 125°C			±1	
I _{CC}	Supply current	V _I = V _{CC} or GND V _{INH} = 0V	25°C		0.01		μA
			–40°C to 85°C	5.5V		20	
			–40°C to 125°C			20	
C _{IC}	Control input capacitance	f = 10MHz	25°C	3.3V	4		pF
C _{IS}	Switch terminal capacitance	f = 10MHz	25°C	3.3V	5.5		pF
C _{OS(on)}	Common terminal ON-capacitance	f = 10MHz	25°C	3.3V	5.5		pF
C _F	Feedthrough capacitance	f = 10MHz	25°C	3.3V	0.5		pF

5.5 Electrical Characteristics (LV) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITIONS	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _{PD}	Power dissipation capacitance	C _L = 50pF, f = 10MHz	25°C		4.5		pF

5.6 Timing Characteristics V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted)

V_{CC} = 2V ± 0.2V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF (see Figure 6-4)	25°C	1.2	10	ns
				–40°C to 85°C			16	
				–40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF (see Figure 6-5)	25°C	3.3	15	ns
				–40°C to 85°C			20	
				–40°C to 125°C			20	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF (see Figure 6-5)	25°C	6	15	ns
				–40°C to 85°C			23	
				–40°C to 125°C			23	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF (see Figure 6-4)	25°C	2.6	12	ns
				–40°C to 85°C			18	
				–40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50pF (see Figure 6-5)	25°C	4.2	25	ns
				–40°C to 85°C			32	
				–40°C to 125°C			32	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50pF (see Figure 6-5)	25°C	9.6	25	ns
				–40°C to 85°C			32	
				–40°C to 125°C			32	

5.7 Timing Characteristics V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)

V_{CC} = 3.3V ± 0.3V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15pF (see Figure 6-4)	25°C	0.8	6	ns
				–40°C to 85°C			10	
				–40°C to 125°C			10	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15pF (see Figure 6-5)	25°C	2.3	11	ns
				–40°C to 85°C			15	
				–40°C to 125°C			15	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15pF (see Figure 6-5)	25°C	4.5	11	ns
				–40°C to 85°C			15	
				–40°C to 125°C			15	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50pF (see Figure 6-4)	25°C	1.5	9	ns
				–40°C to 85°C			12	
				–40°C to 125°C			12	

5.7 Timing Characteristics $V_{CC} = 3.3V \pm 0.3V$ (continued)

over recommended operating free-air temperature range (unless otherwise noted)

$V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$ (see Figure 6-5)	25°C		8	18	ns
					–40°C to 85°C			22	
					–40°C to 125°C			22	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$ (see Figure 6-5)	25°C		7.2	18	ns
					–40°C to 85°C			22	
					–40°C to 125°C			22	

5.8 Timing Characteristics $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range (unless otherwise noted)

$V_{CC} = 5V \pm 0.5V$ (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 15pF$ (see Figure 6-4)	25°C		0.6	4	ns
					–40°C to 85°C			7	
					–40°C to 125°C			7	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 15pF$ (see Figure 6-5)	25°C		3.5	8	ns
					–40°C to 85°C			10	
					–40°C to 125°C			11	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 15pF$ (see Figure 6-5)	25°C		4.4	8	ns
					–40°C to 85°C			10	
					–40°C to 125°C			10	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50pF$ (see Figure 6-4)	25°C		0.8	6	ns
					–40°C to 85°C			8	
					–40°C to 125°C			8	
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50pF$ (see Figure 6-5)	25°C		7	13	ns
					–40°C to 85°C			16	
					–40°C to 125°C			16	
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50pF$ (see Figure 6-5)	25°C		6.2	13	ns
					–40°C to 85°C			16	
					–40°C to 125°C			16	

5.9 AC Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS			MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	4066	C _L = 50pF, R _L = 50Ω, F _{in} = 1MHz (sine wave) (see Figure 6-6) (1)	V _{CC} = 2.3V		60	MHz		
					V _{CC} = 3V		75			
					V _{CC} = 4.5V		100			
Charge Injection (control input to signal output)	INH	COM or Yn	ALL	C _L = 50pF, F _{in} = 1MHz (sine wave) (see Figure 6-7)	V _{CC} = 2.3V		15	mV		
					V _{CC} = 3V		20			
					V _{CC} = 4.5V		50			

5.9 AC Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 50Ω, F _{in} = 1MHz (sine wave) (see Figure 6-8(2))	V _{CC} = 2.3V		–40	dB
					V _{CC} = 3V		–40	
					V _{CC} = 4.5V		–40	
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 50Ω, F _{in} = 1MHz (sine wave) (see Figure 6-9(2))	V _{CC} = 2.3V		–45	dB
					V _{CC} = 3V		–45	
					V _{CC} = 4.5V		–45	
Sine-wave distortion	COM or Yn	Yn or COM	ALL	C _L = 50pF, R _L = 10kΩ, F _{in} = 1kHz (sine wave) (see Figure 6-10)	V _I = 2V _{p-p} , V _{CC} = 2.3V		0.1	%
					V _I = 2.5V _{p-p} , V _{CC} = 3V		0.1	
					V _I = 4V _{p-p} , V _{CC} = 4.5V		0.1	

6 Parameter Measurement Information

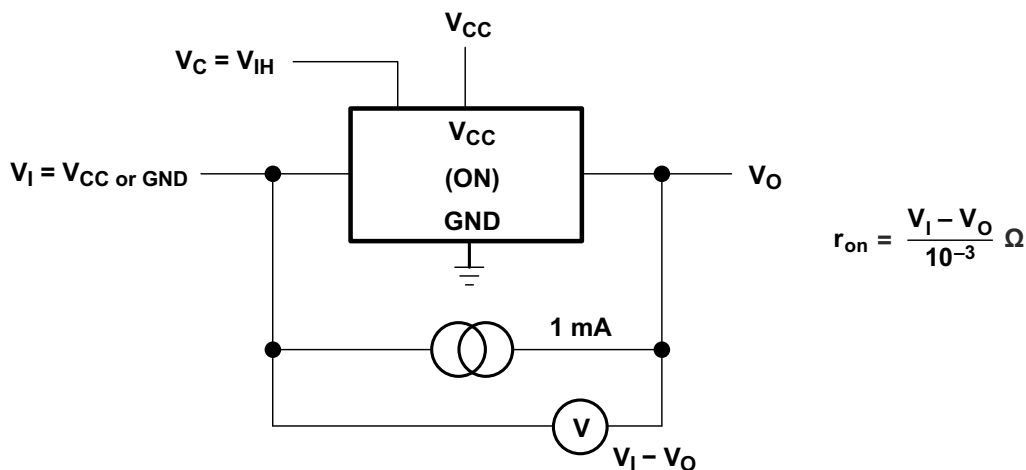


Figure 6-1. ON-State Resistance Test Circuit

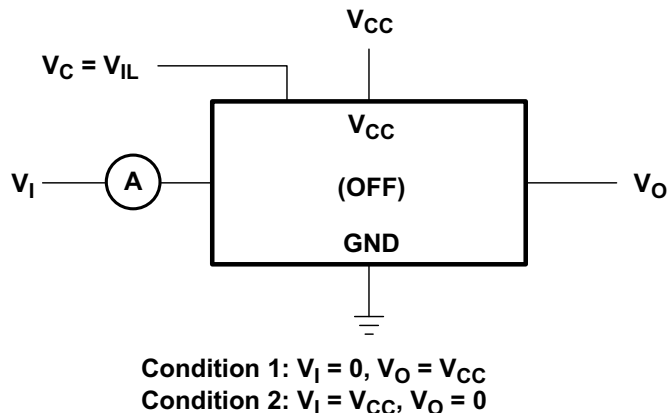


Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

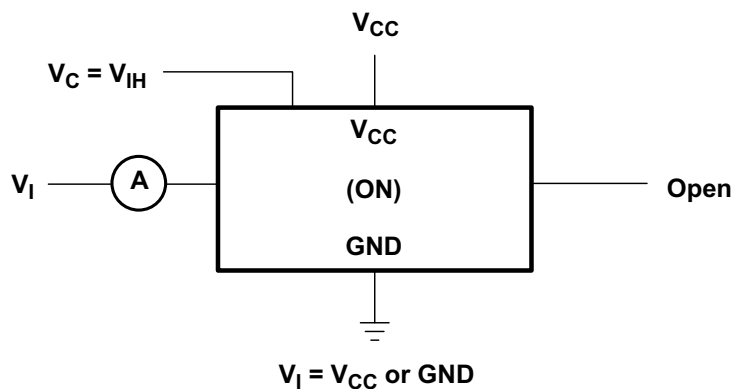


Figure 6-3. ON-State Leakage-Current Test Circuit

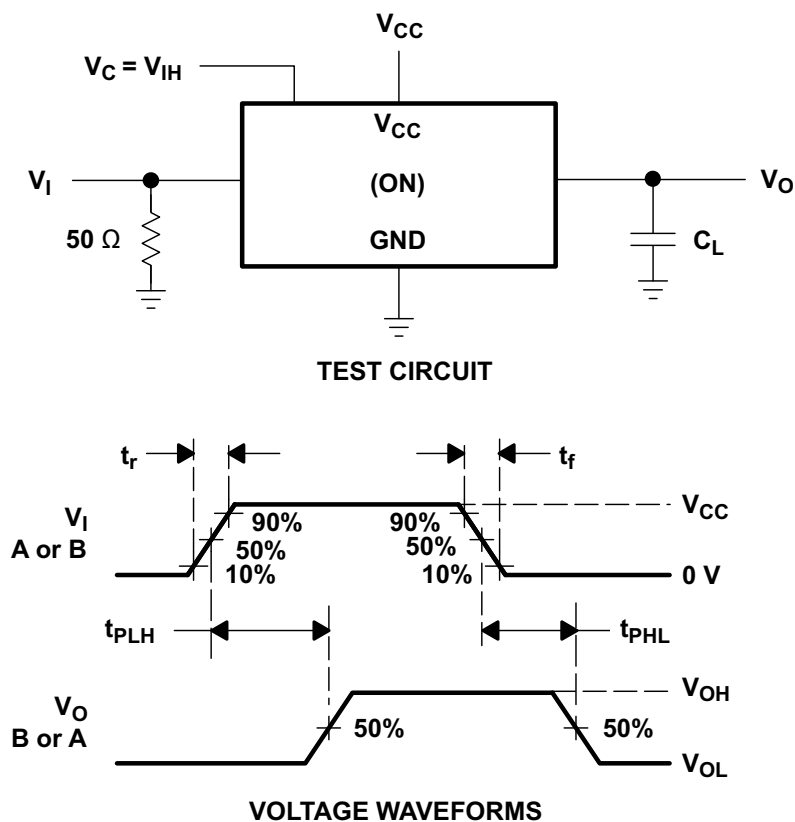
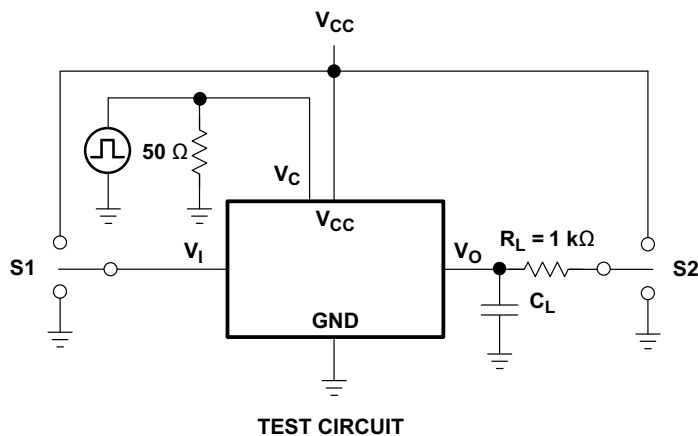
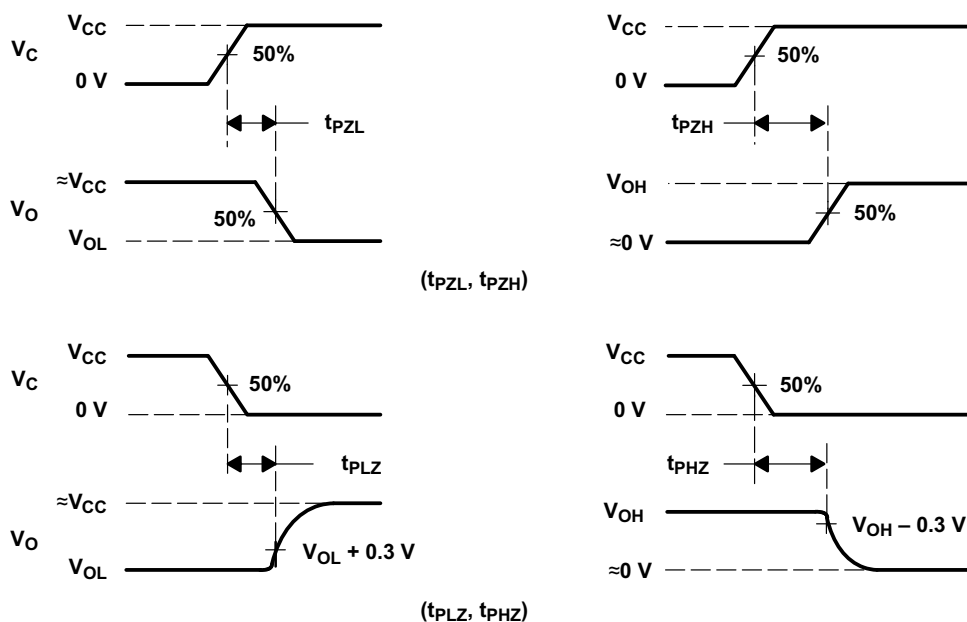


Figure 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PZL}	GND	V_{CC}
t_{PZH}	V_{CC}	GND
t_{PLZ}	GND	V_{CC}
t_{PHZ}	V_{CC}	GND



VOLTAGE WAVEFORMS

Figure 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

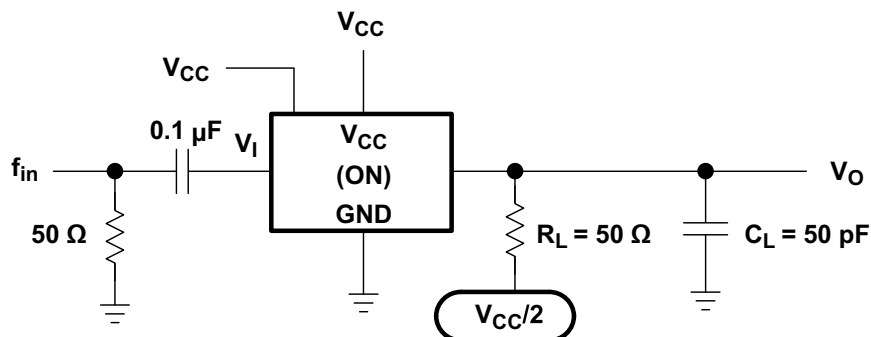


Figure 6-6. Frequency Response (Switch ON)

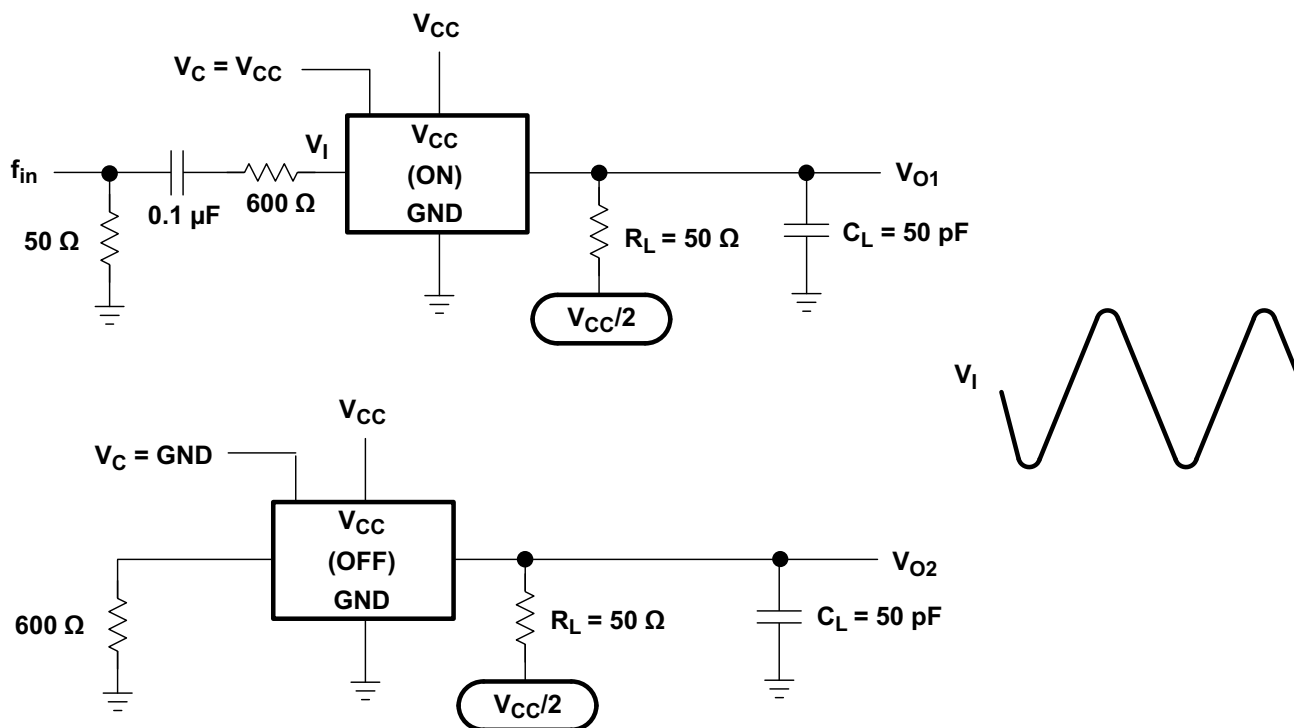


Figure 6-7. Crosstalk Between Any Two Switches

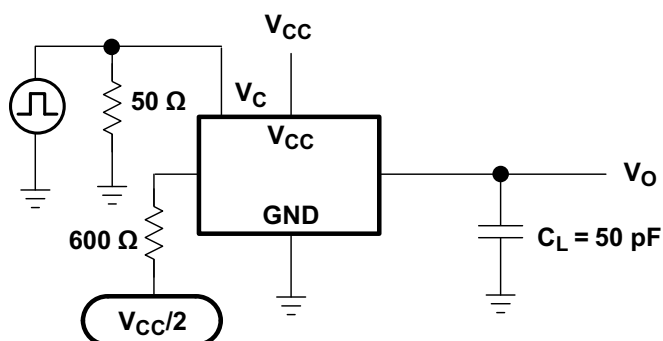


Figure 6-8. Crosstalk (Control Input – Switch Output)

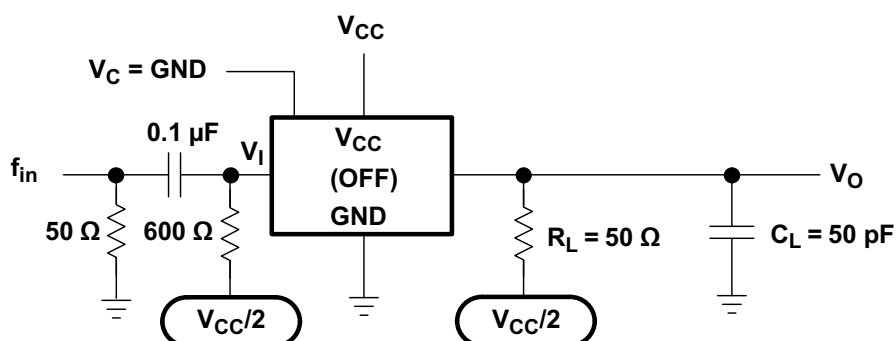


Figure 6-9. Feed-Through Attenuation (Switch OFF)

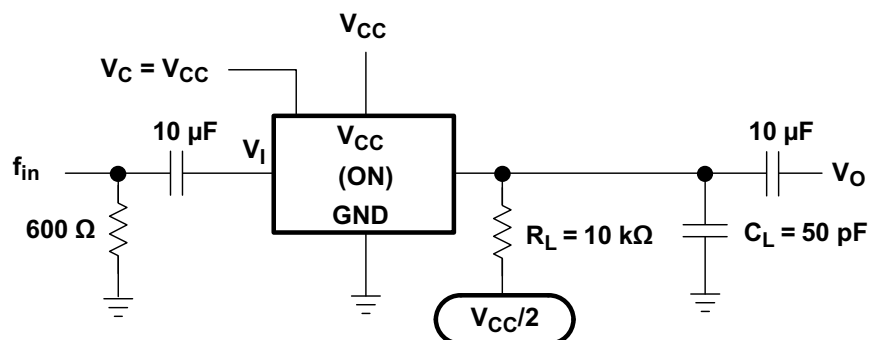


Figure 6-10. Sine-Wave Distortion

7 Detailed Description

7.1 Functional Block Diagram

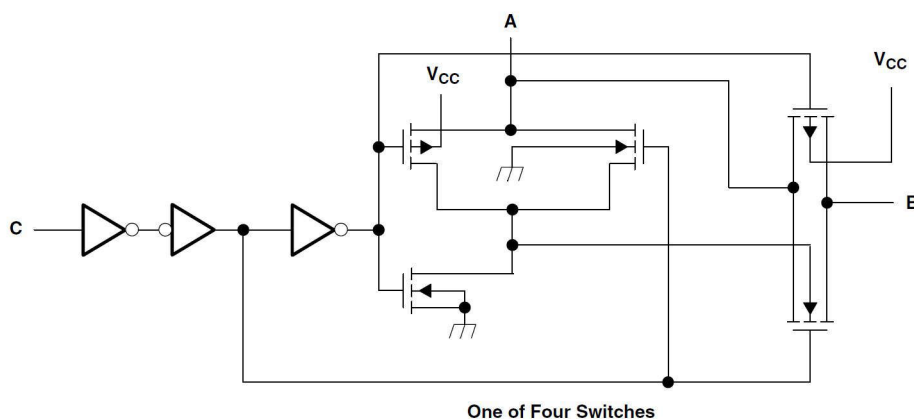


Figure 7-1. Logic Diagram (Positive Logic)

7.2 Device Functional Modes

Table 7-1. Function Table

Input Control (C)	Switch
L	OFF
H	ON

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2006) to Revision J (February 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Removed the SN54LV4066A information from the data sheet.....	1
• Increased V_{CC} operation from: 2V to 5.5V to: 1.65V to 5.5V, and updated specifications such as r_{ON} , $r_{ON(p)}$ Δr_{ON} accordingly.....	1
• Changed RL value from: 600Ω to: 50Ω for frequency response, crosstalk, and feed-through attenuation, and their associated figures.....	10

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4066AD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-40 to 85	LV4066A
SN74LV4066ADBR	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADBR.A	NRND	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066ADGVR	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW066A
SN74LV4066ADGVR.A	NRND	Production	TVSOP (DGV) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4066A
SN74LV4066AN	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74LV4066AN
SN74LV4066AN.A	NRND	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74LV4066AN
SN74LV4066ANSR	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4066A
SN74LV4066ANSR.A	NRND	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV4066A
SN74LV4066APW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LW066A
SN74LV4066APWT	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-40 to 85	LW066A
SN74LV4066ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LW066A
SN74LV4066ARGYRG4	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW066A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4066ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV4066ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4066ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV4066ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV4066ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV4066APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4066APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4066ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4066ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV4066ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV4066ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV4066ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV4066ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LV4066APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LV4066APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV4066ARGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

TUBE



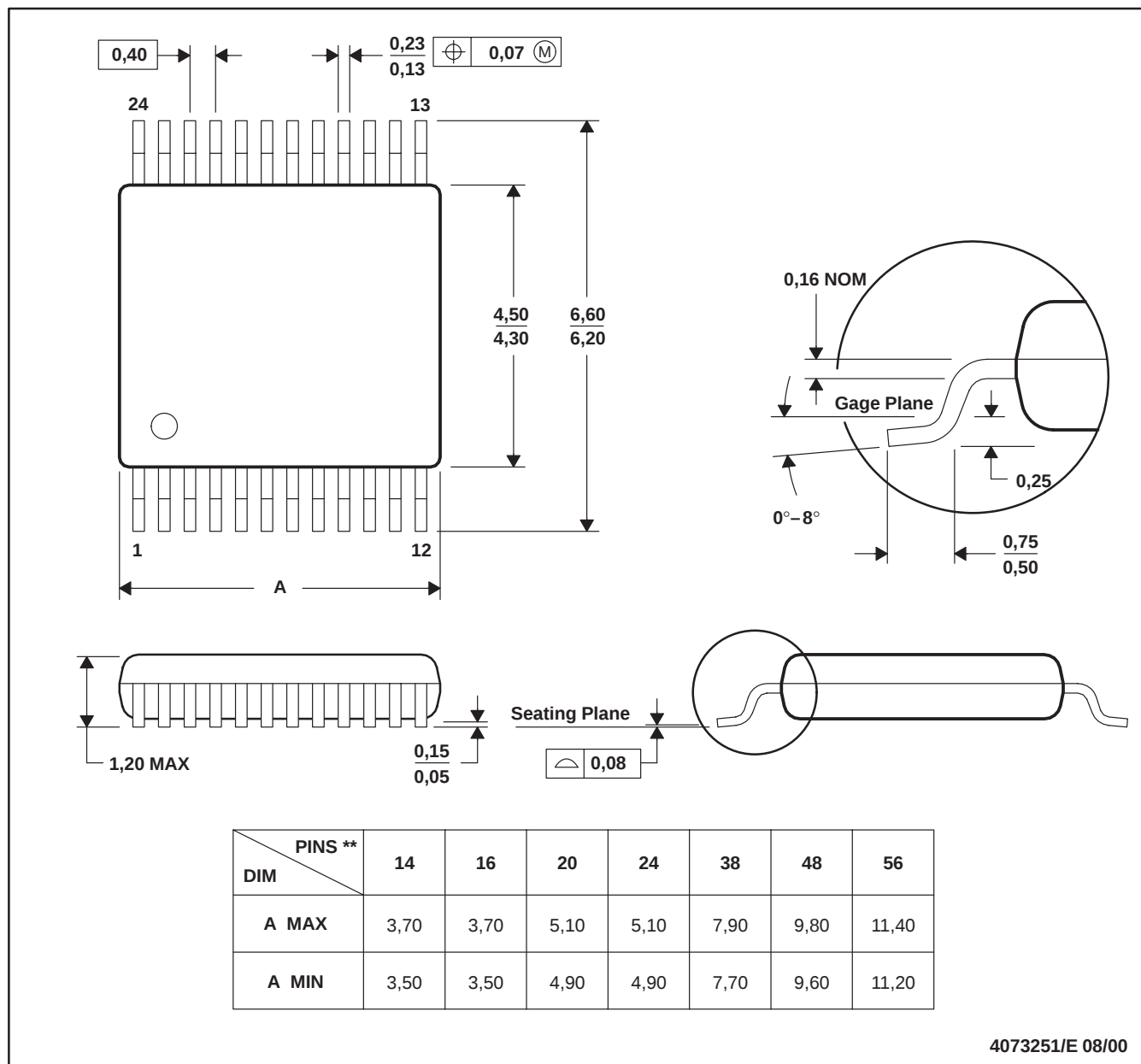
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74LV4066AN.A	N	PDIP	14	25	506	13.97	11230	4.32

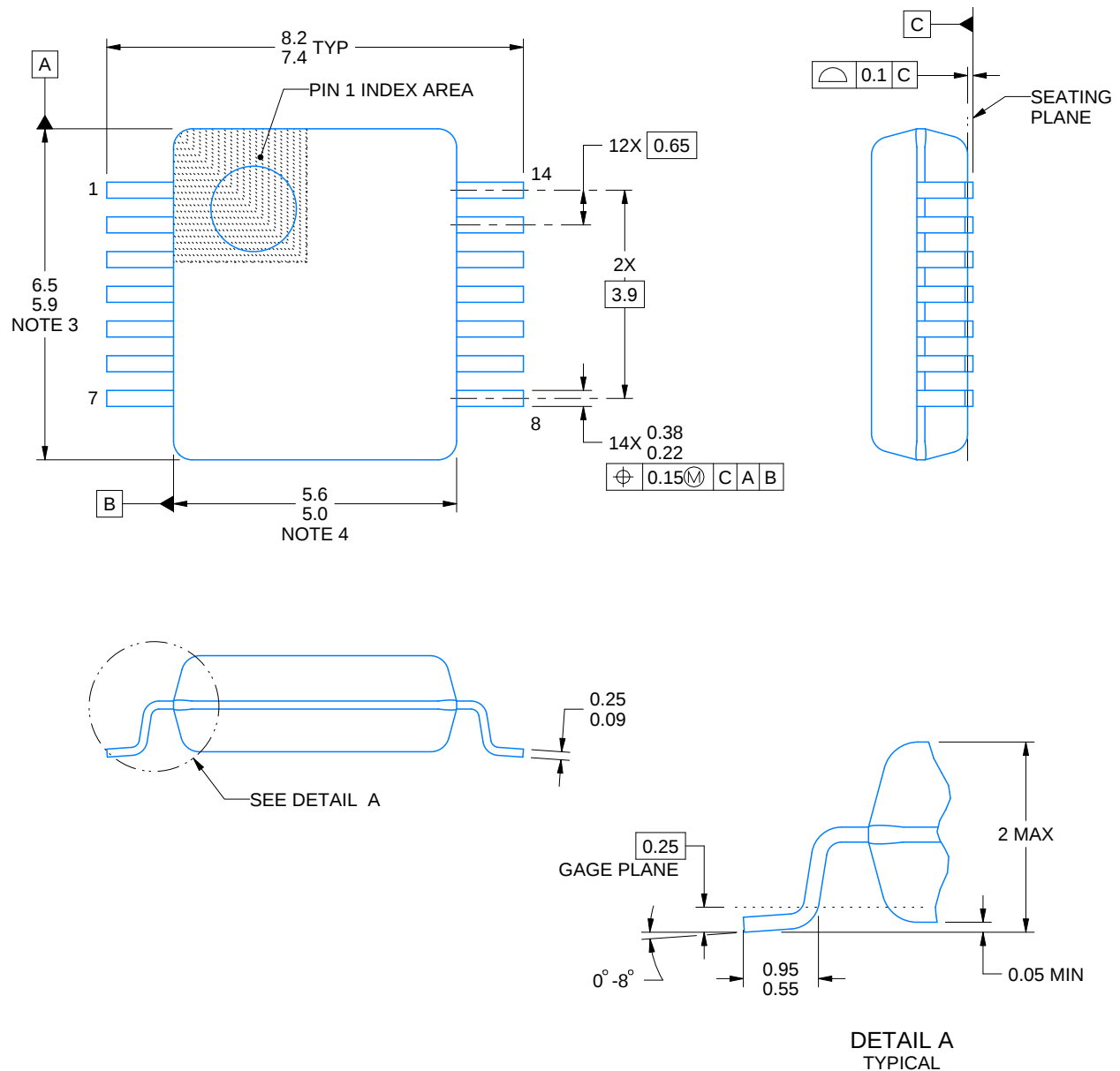
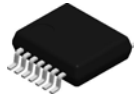
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

NOTES:

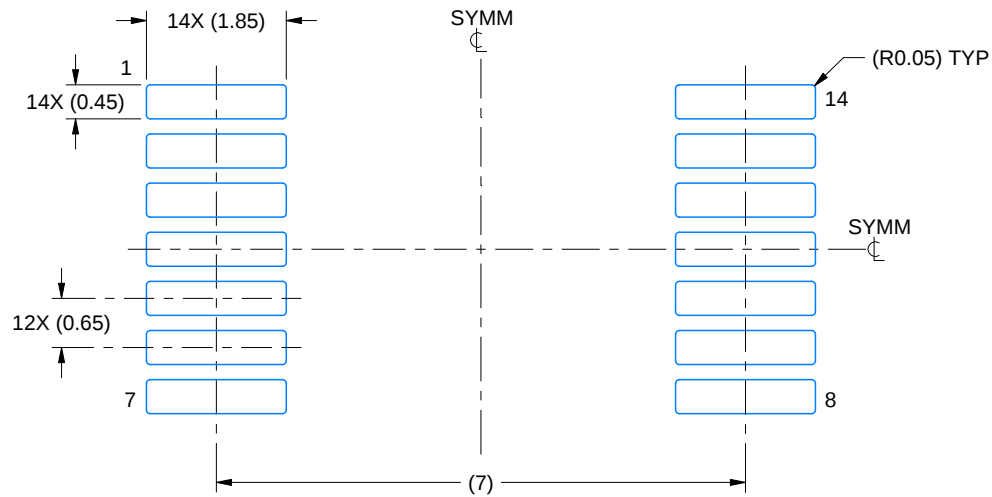
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

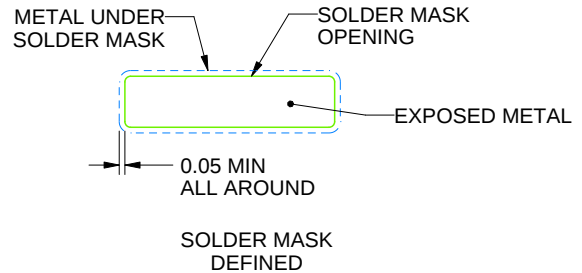
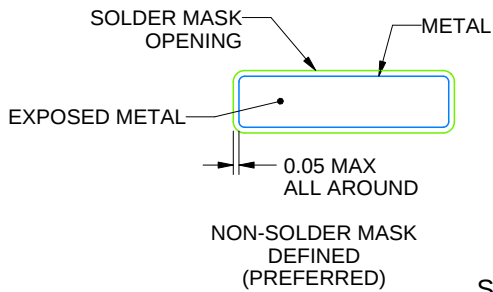
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

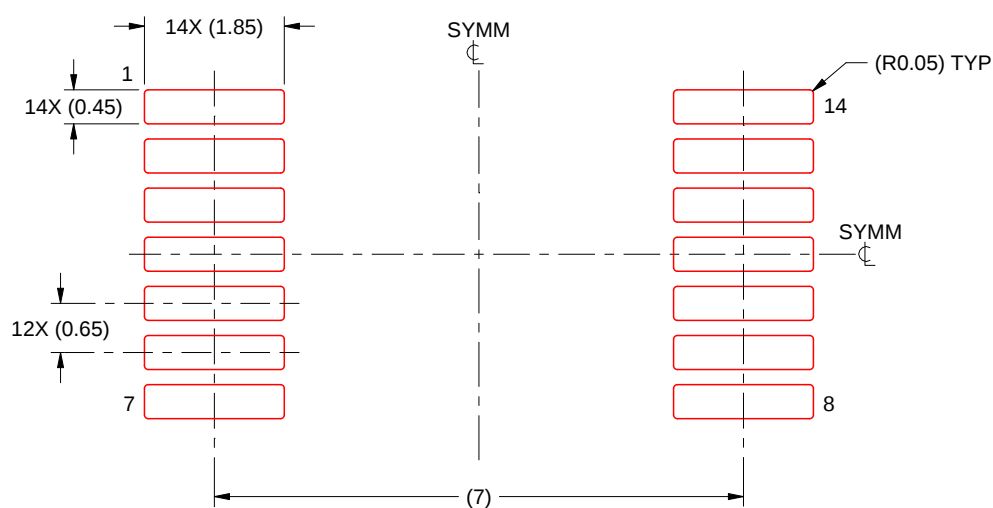
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

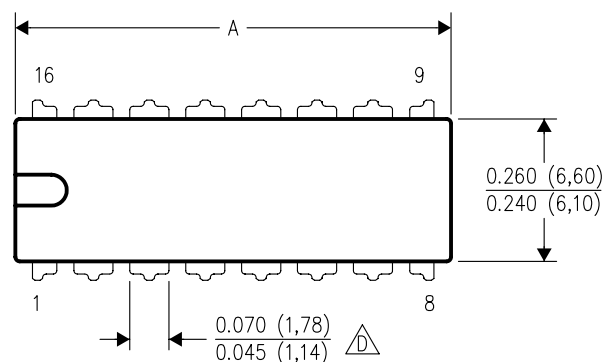
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

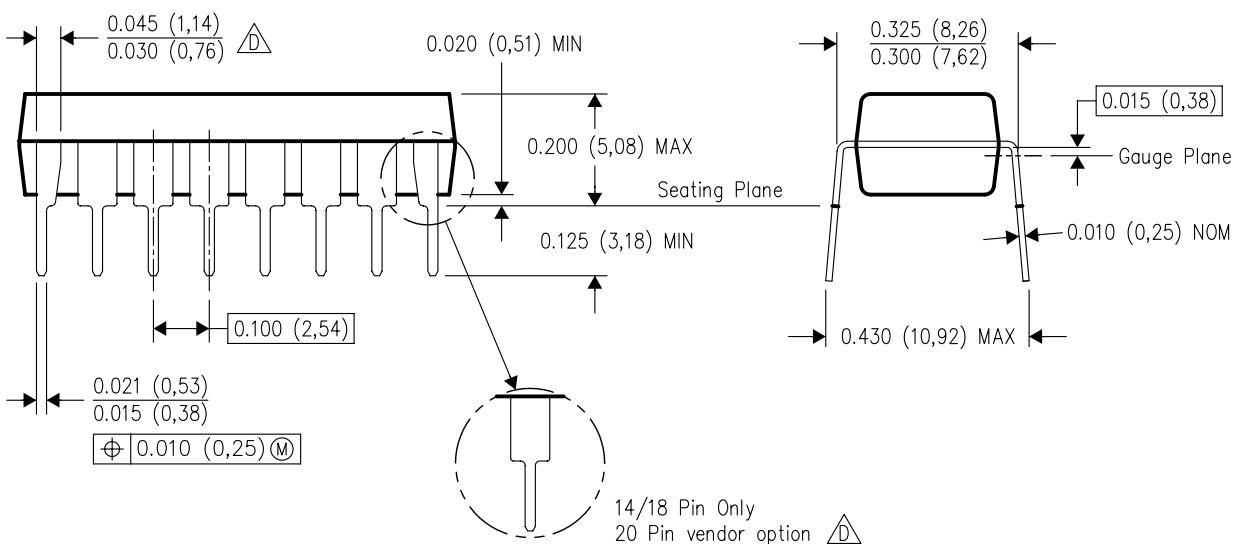
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



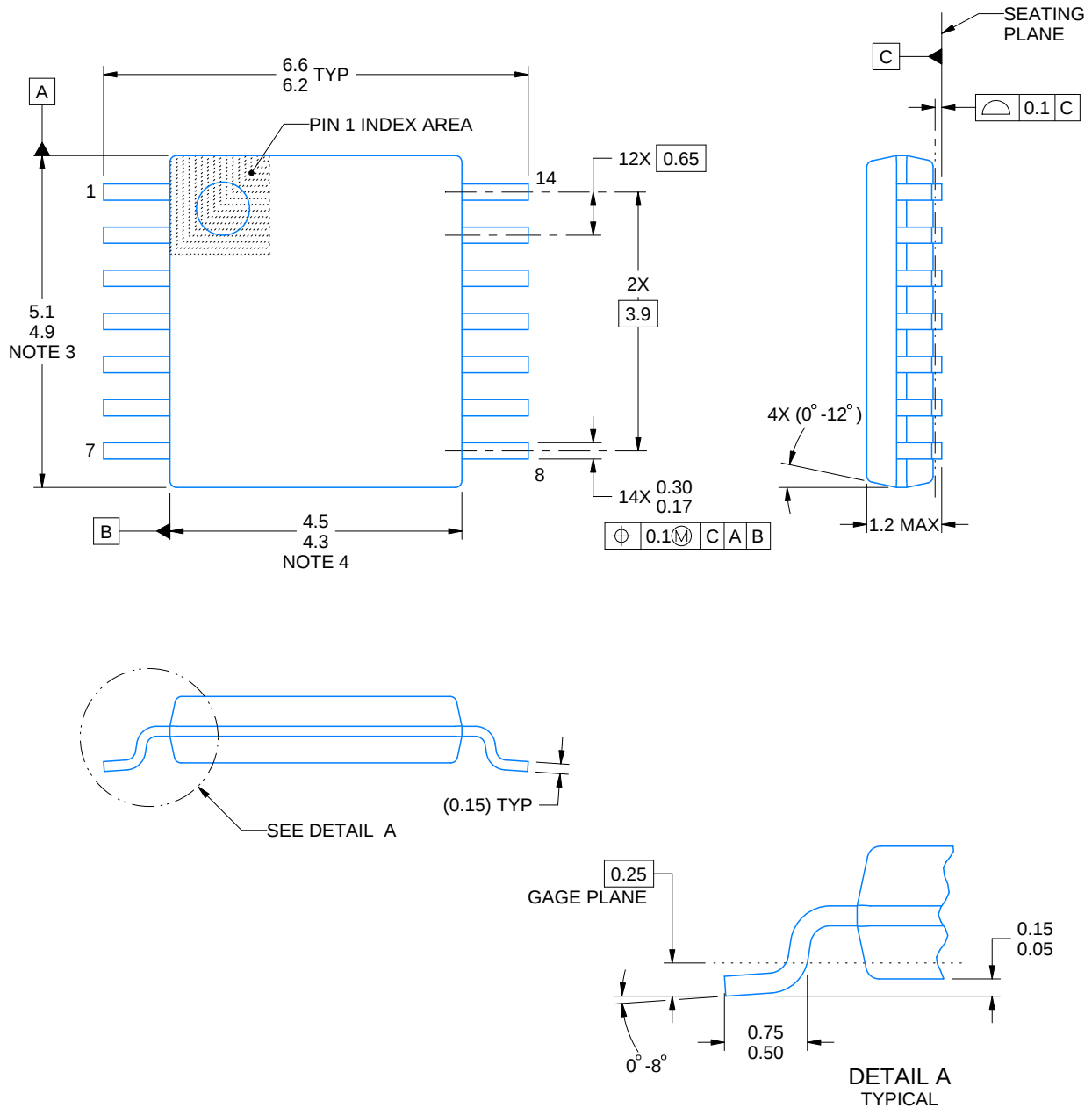
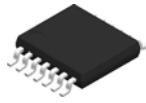
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

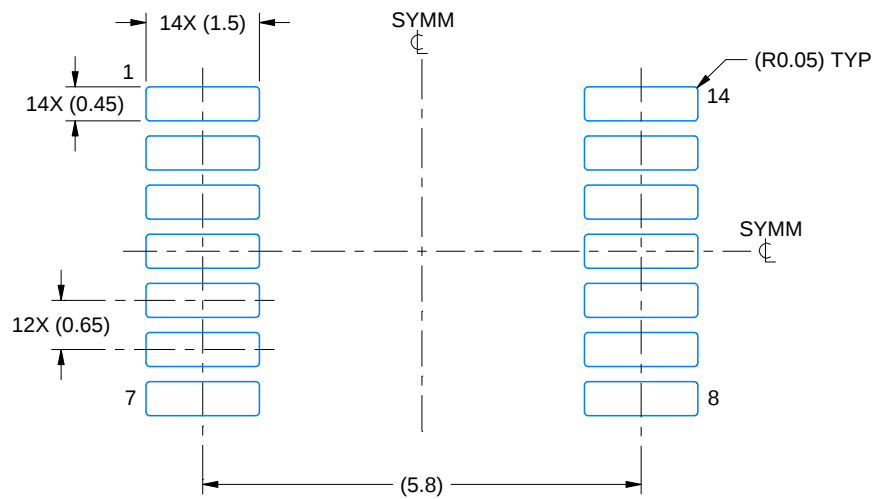
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

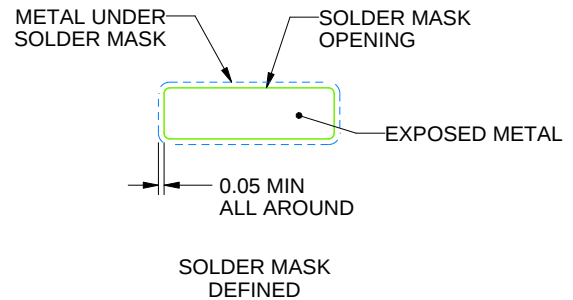
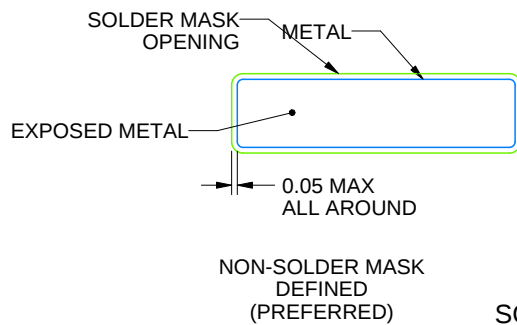
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

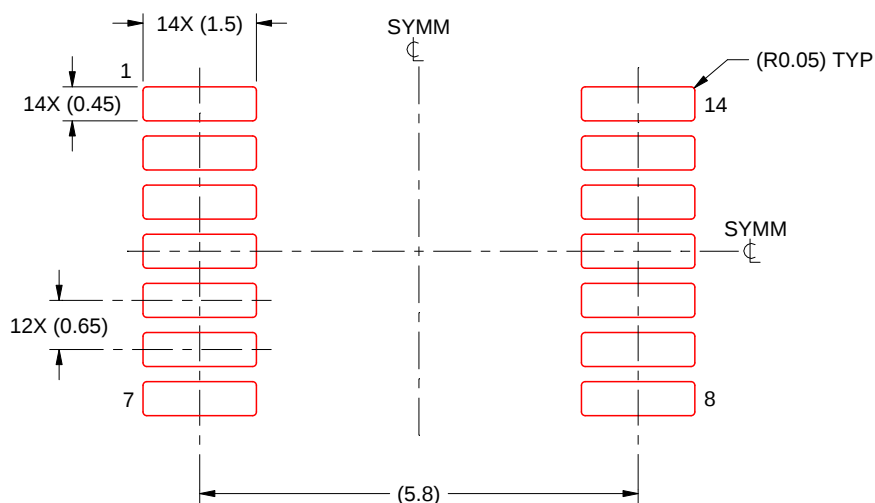
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

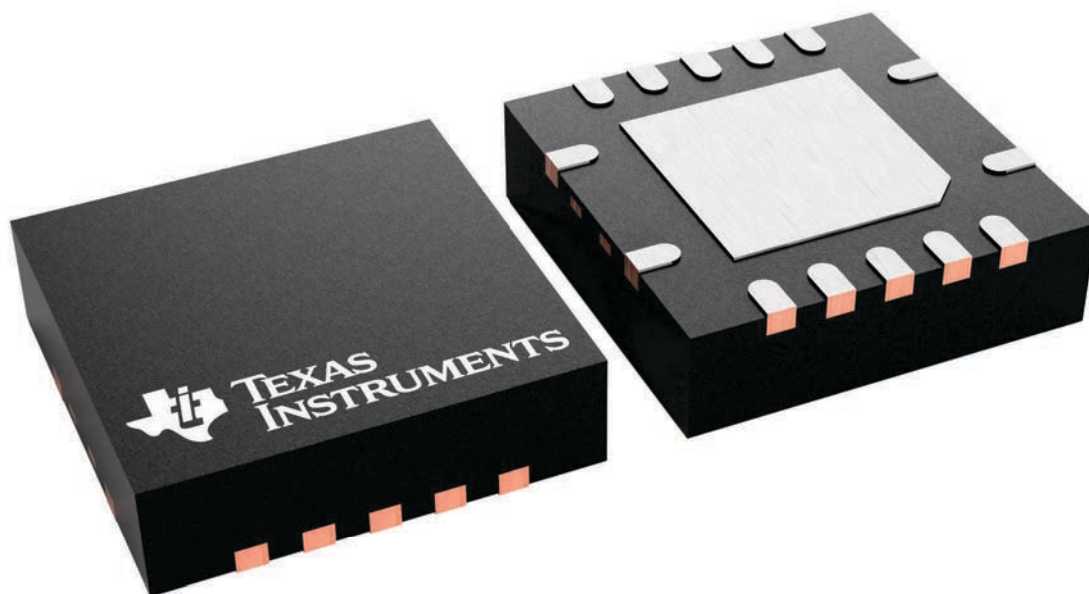
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

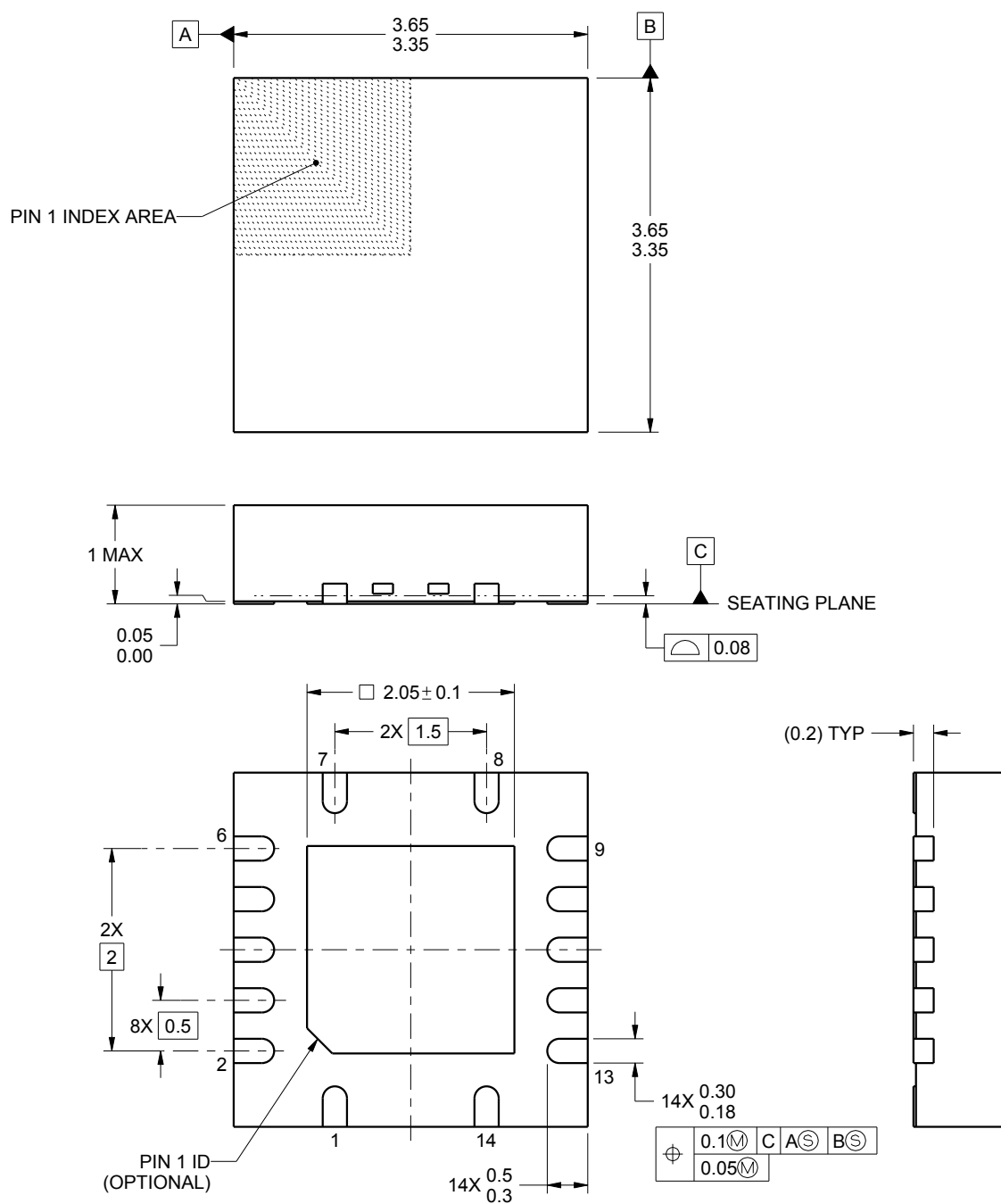


4231541/A



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

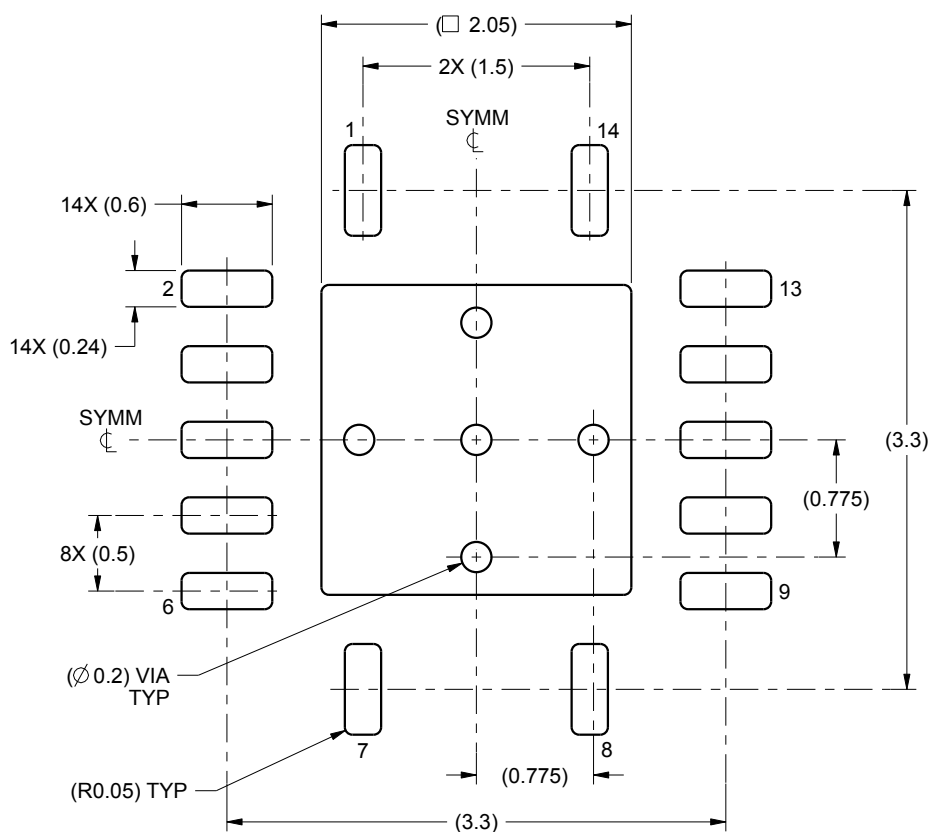
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

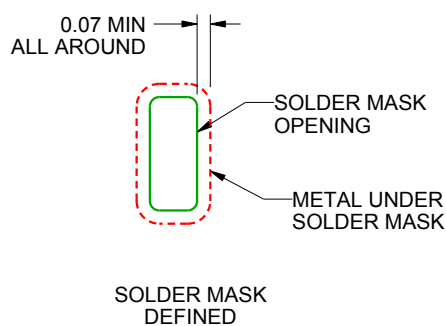
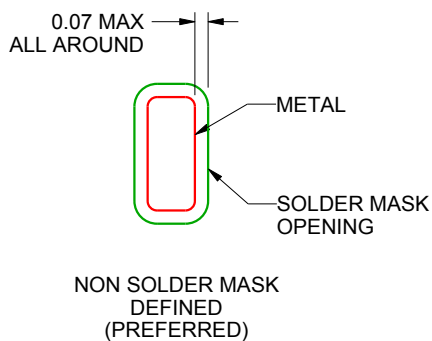
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

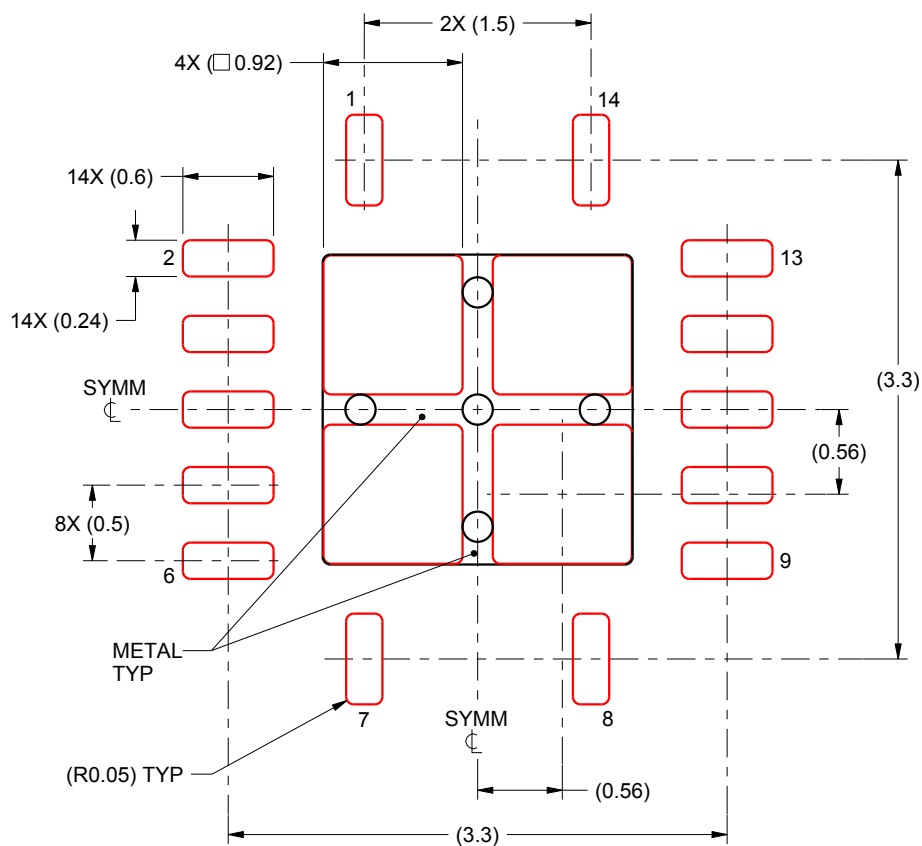
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



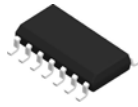
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

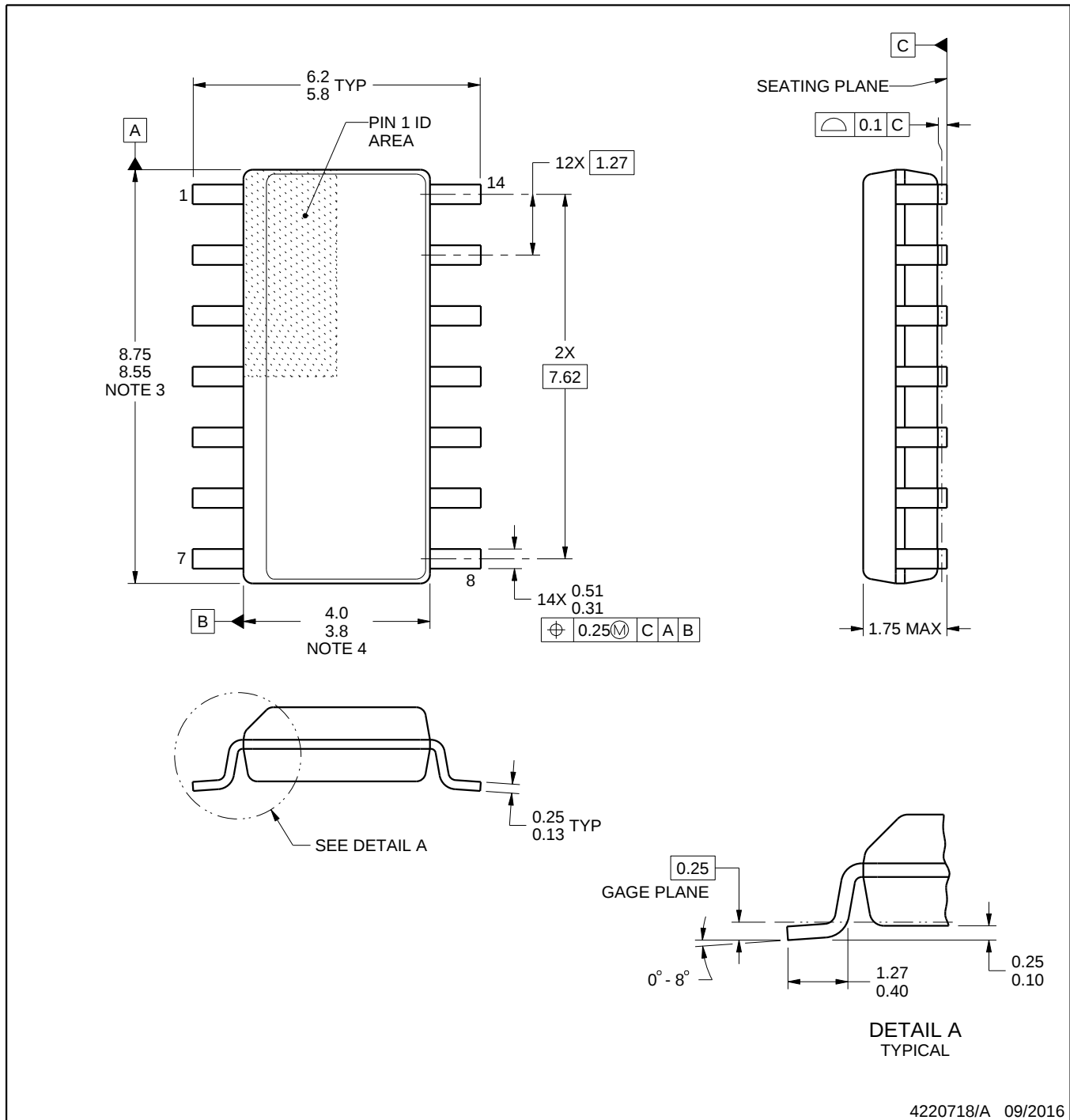
4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

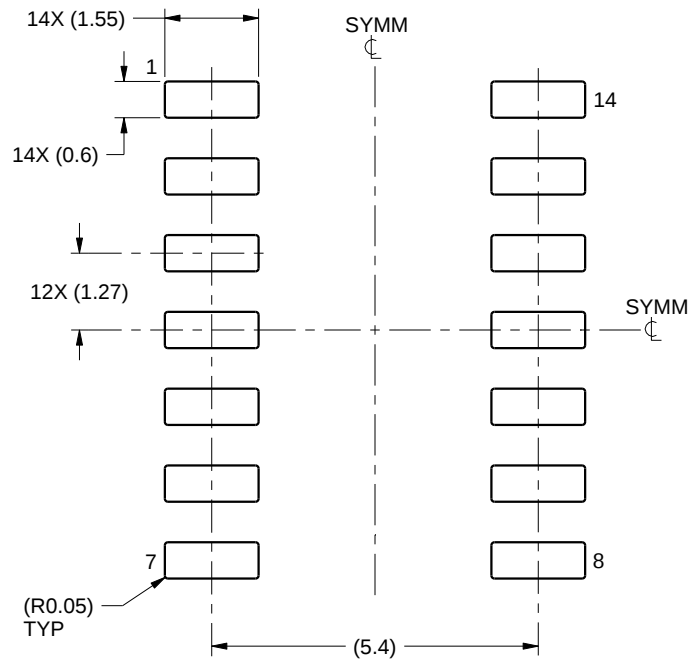
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

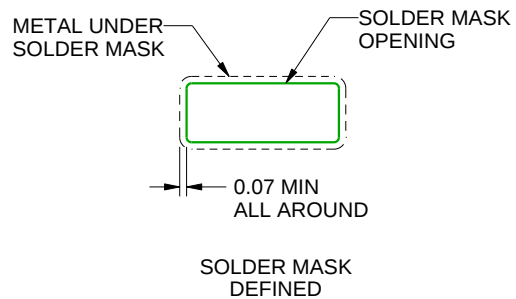
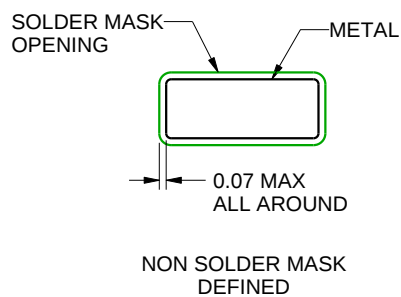
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

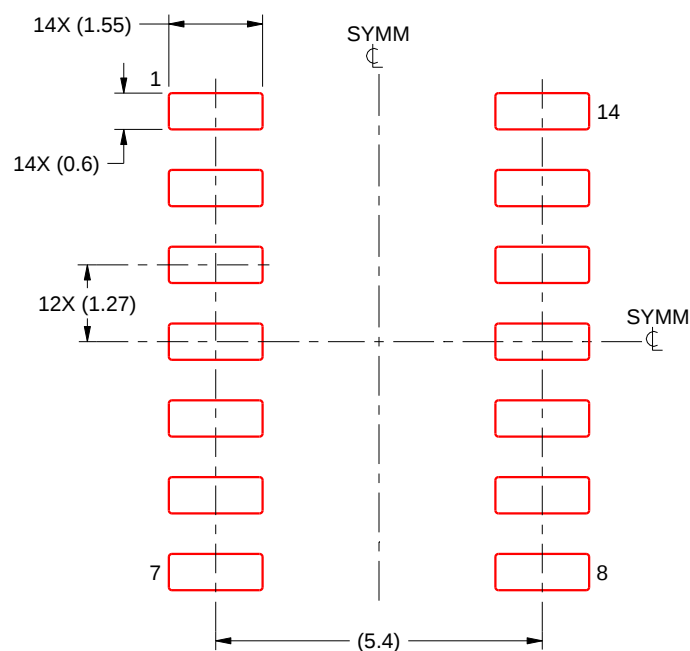
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

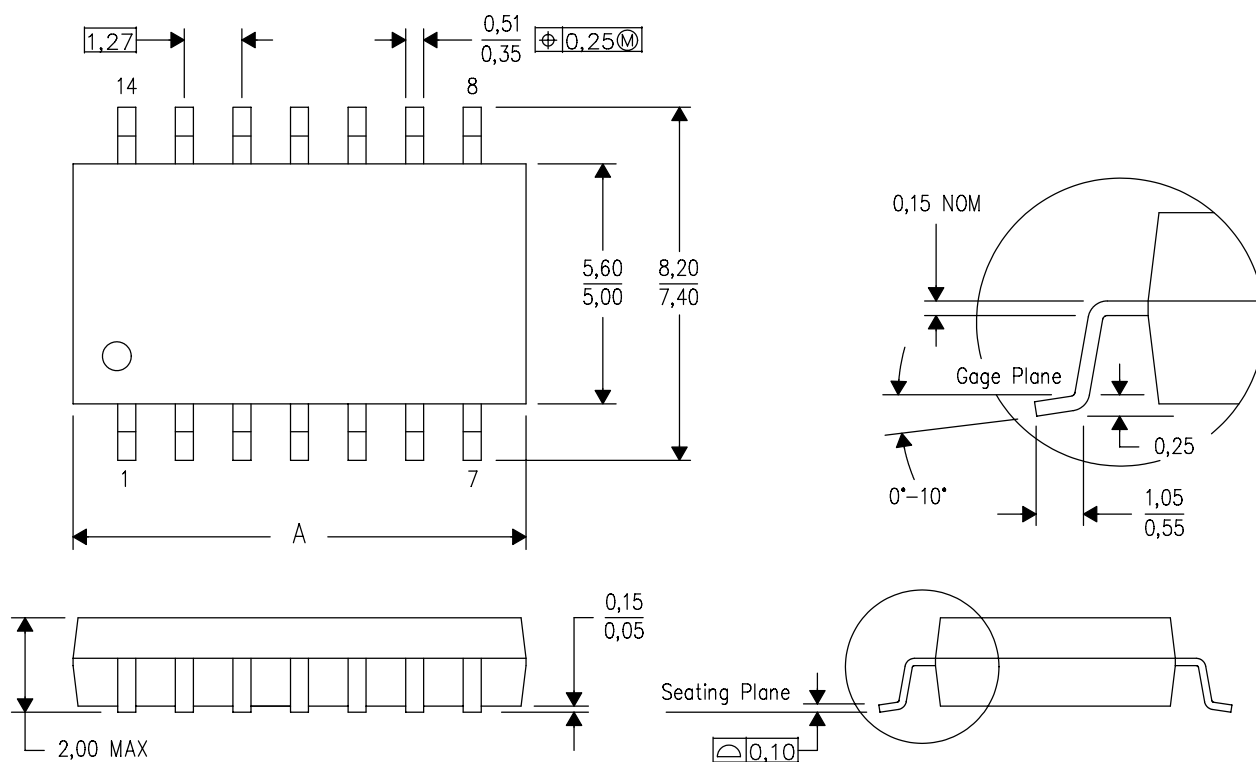
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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TI objects to and rejects any additional or different terms you may have proposed.

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