

SN74AVC4T245 Dual-Bit Bus Transceiver with Configurable Voltage Translation and 3-State Outputs

1 Features

- Control inputs V_{IH}/V_{IL} levels are referenced to V_{CCA} voltage
- Fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range
- I/Os Are 4.6V tolerant
- I_{off} supports partial power-down-mode operation
- Maximum data rates:
 - 380Mbps (1.8V to 3.3V translation)
 - 200Mbps (< 1.8V to 3.3V translation)
 - 200Mbps (translate to 2.5V or 1.8V)
 - 150Mbps (translate to 1.5V)
 - 100Mbps (translate to 1.2V)
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
 - 8000V Human-Body Model (A114-A)
 - 150V Machine Model (A115-A)
 - 1000V Charged-Device Model (C101)

2 Applications

- Personal electronics
- Industrial
- **Enterprise**
- Telecom

3 Description

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2V to 3.6V. The SN74AVC4T245 is optimized to operate with $V_{\text{CCA}}/V_{\text{CCB}}$ set at 1.4V to 3.6V. It is operational with V_{CCA}/V_{CCB} as low as 1.2V. This allows for universal low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

SN74AVC4T245 device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (OE) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC4T245 device is designed so that V_{CCA} supplies the control pins (1DIR, 2DIR, 1 OE, and 2 OE).

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature is designed so that if either V_{CC} input is at GND, then both ports are in the highimpedance state.

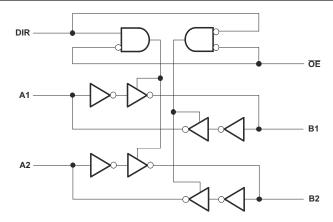
To put the device in the high-impedance state during power up or power down, tie \overline{OE} to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE(2)
	D (SOIC, 16)	9.9mm × 6mm
	DGV (TVSOP, 16)	3.6mm × 6.4mm
	PW (TSSOP, 16)	5mm × 6.4mm
SN74AVC4T245	RGY (WQFN, 16)	4mm × 3.5mm
	RSV (UQFN, 16)	2.6mm × 1.8mm
	BQB (WQFN, 16)	3.5mm × 2.5mm
	DYY (SOT, 16)	4.2mm × 2mm

- For more information, see Section 11. (1)
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.





Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245



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4 Pin Configuration and Functions

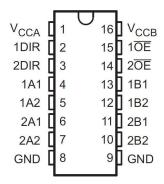


Figure 4-1. D, DGV, or PW Package, 16-Pin SOIC, TVSOP, or PW (Top View)

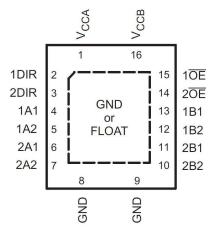
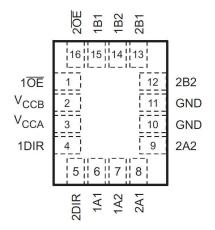


Figure 4-2. RGY Package, 16-Pin WQFN (Top View)



1DIR 2) (15] 10E 2DIR 3 (14 2OE <u>(13</u> 1B1 1A1 (4) Thermal Pad 1A2 5 (12 1B2 2A1 6) (11) 2B1 (10 2B2 2A2 [7] GND GND

Figure 4-4. BQB/WBQB Package, 16-Pin WQFN (Transparent Top View)

Figure 4-3. RSV Package, 16-Pin UQFN (Top View)

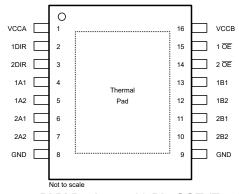


Figure 4-5. DYY Package, 16-Pin SOT (Top View)

Product Folder Links: SN74AVC4T245

Table 4-1. Pin Functions

PIN	NO) .		
NAME	D, DGV, PW, RGY	RSV	TYPE ⁽¹⁾	DESCRIPTION
1A1	4	6	I/O	Input/output 1A1. Referenced to V _{CCA} .
1A2	5	7	I/O	Input/output 1A2. Referenced to V _{CCA} .
1B1	13	15	I/O	Input/output 1B1. Referenced to V _{CCB} .
1B2	12	14	I/O	Input/output 1B2. Referenced to V _{CCB} .
1DIR	2	4	I	Direction-control input for '1' ports
1 ŌĒ	15	1	I	3-state output-mode enables. Pull $\overline{\text{OE}}$ high to place '1' outputs in 3-state mode. Referenced to V_{CCA} .
2A1	6	8	I/O	Input/output 2A1. Referenced to V _{CCA} .
2A2	7	9	I/O	Input/output 2A2. Referenced to V _{CCA} .
2B1	11	13	I/O	Input/output 2B1. Referenced to V _{CCB} .
2B2	10	12	I/O	Input/output 2B2. Referenced to V _{CCB} .
2DIR	3	5	I	Direction-control input for '2' ports
2 OE	14	16	ı	3-state output-mode enables. Pull $\overline{\text{OE}}$ high to place '2' outputs in 3-state mode. Referenced to V_{CCA} .
GND	8, 9	10, 11	_	Ground
V _{CCA}	1	3	_	A-port power supply voltage. 1.2V ≤ V _{CCA} ≤ 3.6V
V _{CCB}	16	2	_	B-port power supply voltage. 1.2V ≤ V _{CCB} ≤ 3.6V

⁽¹⁾ I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN ⁽¹⁾	MAX	UNIT
V _{CCA} V _{CCB}	Supply voltage range		-0.5	4.6	V
		I/O ports (A port)	-0.5	4.6	
VI	Input voltage range ⁽²⁾	I/O ports (B port)	-0.5	4.6	V
		Control inputs	-0.5	4.6	
V	Voltage range applied to any output in the high-impedance or	A port	-0.5	4.6	V
Vo	power-off state ⁽²⁾	B port	-0.5	4.6	v
.,	Voltage range applied to any output in the high or low state ⁽²⁾ (3)	A port	-0.5	V _{CCA} + 0.5	V
Vo	Voltage range applied to any output in the high or low state	B port	-0.5	V _{CCB} + 0.5	v
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} , or GND			±100	mA
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			MIN	MAX	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		8	kV
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		1	KV
		Machine model (C101)		150	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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⁽²⁾ The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.



5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V _{CCI}	V _{cco}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}	Supply voltage				1.2	3.6	V
			1.2V to 1.95V		V _{CCI} × 0.65		
V_{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.95V to 2.7V		1.6		V
	input voltago		2.7V to 3.6V		2		
			1.2V to 1.95V			V _{CCI} × 0.35	
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.95V to 2.7V			0.7	V
	input voltago		2.7V to 3.6V			0.8	
			1.2V to 1.95V		V _{CCA} × 0.65		
V_{IH}	High-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95V to 2.7V		1.6		V
	input voltage	(referenced to VCCA)	2.7V to 3.6V		2		
			1.2V to 1.95V			V _{CCA} × 0.35	
V_{IL}	Low-level input voltage	DIR (referenced to V _{CCA}) ⁽⁵⁾	1.95V to 2.7V			0.7	V
	input voltage	(referenced to VCCA)	2.7V to 3.6V			0.8	
VI	Input voltage				0	3.6	V
.,	0.1.1.11	Active state			0	V _{CCO}	V
Vo	Output voltage	3-state			0	3.6	V
		-		1.2V		-3	
				1.4V to 1.6V		-6	
I _{OH}	High-level output cur	rent		1.65V to 1.95V		-8	mA
				2.3V to 2.7V		-9	
				3V to 3.6V		-12	
				1.1V to 1.2V		3	
				1.4V to 1.6V		6	
I_{OL}	Low-level output curr	ent		1.65V to 1.95V		8	mA
				2.3V to 2.7V		9	
				3V to 3.6V		12	
Δt/Δν	Input transition rise o	r fall rate				5	ns/V
T _A	Operating free-air ter	mperature			-40	85	°C

⁽¹⁾ V_{CCI} is the V_{CC} associated with the input port.

⁽²⁾ V_{CCO} is the V_{CC} associated with the output port.

⁽³⁾ All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. Refer to the *Implications of Slow or* Floating CMOS Inputs application report.

⁽⁴⁾ For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7V$, V_{IL} max = $V_{CCI} \times 0.3V$ (5) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7V$, V_{IL} max = $V_{CCA} \times 0.3V$



5.4 Thermal Information

				SI	N74AVC4T	245				
	THERMAL METRIC ⁽¹⁾	D	BQB	DYY	DGV	PW	RGY	RSV	UNIT	
		16 PINS								
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.5	80.8	163.4	126.0	102.8	68.8	146.9		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	46.9	77.9	90.0	50.8	35.9	70.6	53.6		
$R_{\theta JB}$	Junction-to-board thermal resistance	43.0	50.7	93.1	57.7	57.5	45.0	75.6		
ΨЈТ	Junction-to-top characterization parameter	13.4	7.4	10.9	5.7	1.6	11.9	13.5	°C/W	
ΨЈВ	Junction-to-board characterization parameter	42.7	50.6	92.1	57.2	56.9	44.7	75.6		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	28.4	_	_	_	28.2	_		

⁽¹⁾ For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ⁽¹⁾		TEST CONDI	TIONS	V	V	T,	_A = 25°C		-40°C to 8	5°C	UNIT
	(2)	TEST CONDI	IIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	MIN	MAX	UNII
		I _{OH} = -100μA		1.2V to 3.6V	1.2V to 3.6V				V _{CCO} - 0.2		
		I _{OH} = -3mA		1.2V	1.2V		0.95				
\/		I _{OH} = -6mA	V _I = V _{IH}	1.4V	1.4V				1.05		V
V _{OH}		I _{OH} = -8mA	VI - VIH	1.65V	1.65V				1.2		V
		I _{OH} = -9mA		2.3V	2.3V				1.75		
		I _{OH} = -12mA		3V	3V				2.3		
		I _{OL} = 100μA		1.2V to 3.6V	1.2V to 3.6V					0.2	
		I _{OL} = 3mA		1.2V	1.2V		0.25				
\/		I _{OL} = 6mA	$V_{I} = V_{IL}$	1.4V	1.4V					0.35	V
V_{OL}		I _{OL} = 8mA	V - V L	1.65V	1.65V					0.45	V
		I _{OL} = 9mA		2.3V	2.3V					0.55	
		I _{OL} = 12mA		3V	3V					0.7	
l _l	Control inputs	V _I = V _{CCA} or GND		1.2V to 3.6V	1.2V to 3.6V		±0.025	±0.25		±1	μA
	A Dt	V V 0 to 0 0		0V	0V to 3.6V		±0.1	±1		±5	
l _{off}	A or B port	$V_{\rm I}$ or $V_{\rm O} = 0$ to 3.6	V	0V to 3.6V	0V		±0.1	±1		±5	μA
l _{OZ}	A or B port	$V_O = V_{CCO}$ or GNE $V_I = V_{CCI}$ or GND,	OE = V _{IH}	3.6V	3.6V		±0.5	±2.5		±5	μΑ
				1.2V to 3.6V	1.2V to 3.6V					8	
I_{CCA}		$V_I = V_{CCI}$ or GND,	I _O = 0	0V	0V to 3.6V					-2	μΑ
				0V to 3.6V	0V					8	
				1.2V to 3.6V	1.2V to 3.6V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND,	I _O = 0	0V	0V to 3.6V					8	μΑ
				0V to 3.6V	0V					-2	
I _{CCA} +	· I _{CCB}	$V_I = V_{CCI}$ or GND,	I _O = 0	1.2V to 3.6V	1.2V to 3.6V					16	μA
Ci	Control inputs	V _I = 3.3V or GND		3.3V	3.3V		3.5			4.5	pF
C _{io}	A or B port	V _O = 3.3V or GND		3.3V	3.3V		6			7	pF

 $[\]begin{array}{ll} \hbox{(1)} & V_{CCI} \text{ is the } V_{CC} \text{ associated with the input port.} \\ \hbox{(2)} & V_{CCO} \text{ is the } V_{CC} \text{ associated with the output port.} \\ \end{array}$

5.6 Operating Characteristics

 $T_A = 25^{\circ}C$

P	PARAME	TER	TEST CONDITIONS	V _{CCA} = V _{CCB} = 1.2V	V _{CCA} = V _{CCB} = 1.5V	V _{CCA} = V _{CCB} = 1.8V	V _{CCA} = V _{CCB} = 2.5V	$V_{CCA} = V_{CCB} = 3.3V$	UNIT
			CONDINIONS	TYP	TYP	TYP	TYP	TYP	
	A to B	Outputs enabled		1	1	1	1.5	2	
C _{pdA} (1)	Alob	Outputs disabled	$C_L = 0,$ f = 10MHz,	1	1	1	1	1	pF
OpdA	B to A	Outputs enabled	$t_r = t_f = 1$ ns	12	12.5	13	14	15	ρi
	BIOA	Outputs disabled		1	1	1	1	1	
	A to B	Outputs enabled		12	12.5	13	14	15	
C _{pdB} (1)	Alob	Outputs disabled	$C_L = 0,$ f = 10MHz,	1	1	1	1	1	pF
PdB	Outpu	Outputs enabled	$t_r = t_f = 1 \text{ns}$	1	1	1	1	2	Pi
	BIOA	Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

5.7 Switching Characteristics: $V_{CCA} = 1.2V$

over recommended operating free-air temperature range, $V_{CCA} = 1.2V$ (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = 1.5V ± 0.1V	V _{CCB} = 1.8V ± 0.15V	V _{CCB} = 2.5V ± 0.2V	V _{CCB} = 3.3V ± 0.3V	UNIT		
	(INFOT)	(0011-01)	(0011-01)	(0011 01)	TYP	TYP	TYP	TYP	TYP	
t _{PLH}	Α	В	3.4	2.9	2.7	2.6	2.8	ns		
t _{PHL}	^	Ь	3.4	2.9	2.7	2.6	2.8	115		
t _{PLH}	В	А	3.6	3.1	2.8	2.6	2.6	ns		
t _{PHL}	Ь	A	3.6	3.1	2.8	2.6	2.6	1115		
t _{PZH}	ŌĒ	А	5.6	4.7	4.3	3.9	3.7	no		
t _{PZL}	OE	A	5.6	4.7	4.3	3.9	3.7	ns		
t _{PZH}	ŌĒ	В	5	4.3	3.9	3.6	3.6	ns		
t _{PZL}	OL	В	5	4.3	3.9	3.6	3.6	1115		
t _{PHZ}	ŌĒ	А	6.2	5.2	5.2	4.3	4.8	no		
t _{PLZ}	OE .	A	6.2	5.2	5.2	4.3	4.8	ns		
t _{PHZ}	ŌĒ	В	5.9	5.1	5	4.7	5.5	ns		
t _{PLZ}	OE	ט	5.9	5.1	5	4.7	5.5	1115		

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5.8 Switching Characteristics: $V_{CCA} = 1.5V \pm 0.1V$

over recommended operating free-air temperature range, $V_{CCA} = 1.5V \pm 0.1V$ (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = ± 0.		V _{CCB} = ± 0.1		V _{CCB} = ± 0.		V _{CCB} = ± 0.		UNIT
	(INPUT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	Α	В	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t _{PHL}	A	Ь	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	115
t _{PLH}	В	А	3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
t _{PHL}	Ь		3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	115
t _{PZH}	ŌĒ	А	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
t _{PZL}	OL	Α	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	115
t _{PZH}	ŌĒ	В	4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
t _{PZL}	OL		4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	115
t _{PHZ}	ŌĒ	А	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ne
t _{PLZ}	OE.	_ ^	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
t _{PHZ}	ŌĒ	В	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ne
t _{PLZ}	UE	D	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns

5.9 Switching Characteristics: $V_{CCA} = 1.8V \pm 0.15V$

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = ± 0.1		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = ± 0.3		UNIT			
	(INFOT)	(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX				
t _{PLH}	Α	В	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	ns			
t _{PHL}	A	Б	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	115			
t _{PLH}	В	А	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns			
t _{PHL}	Ь	^	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	115			
t _{PZH}	ŌĒ	А	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	ns			
t _{PZL}	OL	^	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	113			
t _{PZH}	ŌĒ	В	4.1	1.2	9.2	1	7.4	8.0	5.3	0.8	4.6	ns			
t _{PZL}	UE	Б	4.1	1.2	9.2	1	7.4	8.0	5.3	0.8	4.6	115			
t _{PHZ}	<u> </u>	۸	5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	ns			
t _{PLZ}	ŌĒ	Α	A	A	DE A	5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	113
t _{PHZ}	ŌĒ	В	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	ne			
t _{PLZ}	<u> </u>	ט	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	ns			

5.10 Switching Characteristics: $V_{CCA} = 2.5V \pm 0.2V$

over recommended operating free-air temperature range, $V_{CCA} = 2.5V \pm 0.2V$ (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = ± 0.7		V _{CCB} = 1.8V ± 0.15V		V _{CCB} = ± 0.2		V _{CCB} = 3.3V ± 0.3V		UNIT
		(001701)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MIN MAX	
t _{PLH}	Α	В	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
t _{PHL}	^	ь	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	115
t _{PLH}	В	Α	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t _{PHL}	ь	A	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	115
t _{PZH}	ŌĒ	A	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	no
t _{PZL}	OE	A	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
t _{PZH}	ŌĒ	В	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
t _{PZL}	OL	ь	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	115
t _{PHZ}	ŌĒ	Α	4.7	1	8.4	1	8.4	1	6.2	1	6.6	ne
t _{PLZ}	OE	A	4.7	1	8.4	1	8.4	1	6.2	1	6.6	ns
t _{PHZ}	ŌĒ	В	4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	no
t _{PLZ}	UE	В	4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns

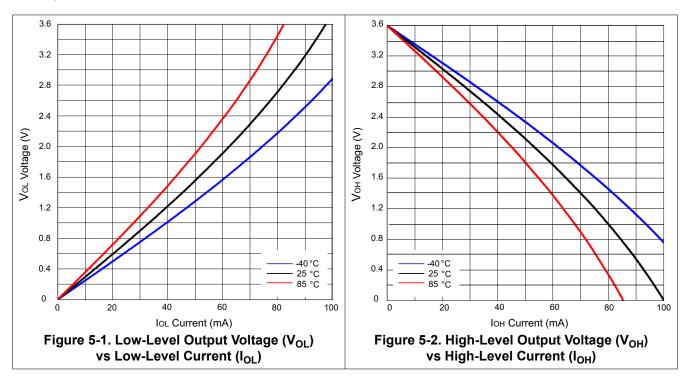
5.11 Switching Characteristics: $V_{CCA} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CCA} = 3.3V \pm 0.3V$ (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2V	V _{CCB} = 1.5V ± 0.1V		V _{CCB} = ± 0.1		V _{CCB} = ± 0.2		V _{CCB} = 3.3V ± 0.3V		UNIT
	(INFOT)	(OUTPUT)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	А	В	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
t _{PHL}	^	ь	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	115
t _{PLH}	В	Α	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
t _{PHL}	ь	A	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	115
t _{PZH}	ŌĒ	А	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
t _{PZL}	OL	^	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	115
t _{PZH}	ŌĒ	В	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
t _{PZL}	OL	ь	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	115
t _{PHZ}	ŌĒ	Α	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
t _{PLZ}	OL	Α	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	115
t _{PHZ}	ŌĒ	В	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
t _{PLZ}	OE	О	5.3	1.4	9.3	1.2	8.1	1	6.4	8.0	6.2	115

Product Folder Links: SN74AVC4T245

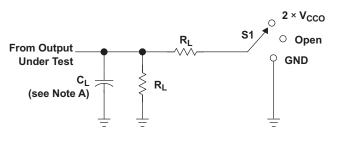
5.12 Typical Characteristics





 $\mathbf{V}_{\mathsf{CCA}}$

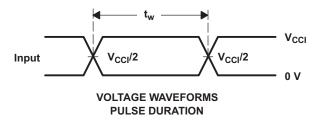
6 Parameter Measurement Information

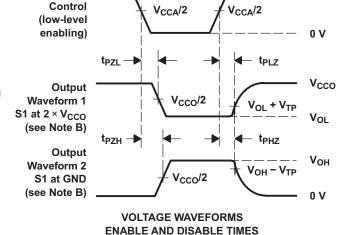


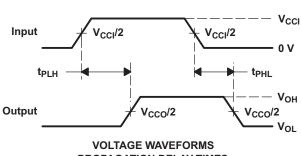
TEST	S 1
t _{pd}	Open
t _{PLZ} /t _{PZL}	2 × V _{CCO}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V _{CCO}	CL	R_L	V _{TP}		
1.2 V	15 pF	2 k Ω	0.1 V		
$1.5~V\pm0.1~V$	15 pF	2 k Ω	0.1 V		
$1.8 V \pm 0.15 V$	15 pF	2 k Ω	0.15 V		
$2.5~V\pm0.2~V$	15 pF	2 k Ω	0.15 V		
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V		







PROPAGATION DELAY TIMES

NOTES: A. C_I includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

Output

- C. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_Ω = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-1. Load and Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The SN74AVC4T245 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. V_{CCA} supports the Ax pins and control pins (1DIR, 2DIR,1 \overline{OE} , and 2 \overline{OE}), and V_{CCB} supports the Bx pins. The A port can accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.2V to 3.6V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when \overline{OE} is set to low. When \overline{OE} is set to high, both Ax and Bx pins are in the high-impedance state.

7.2 Functional Block Diagram

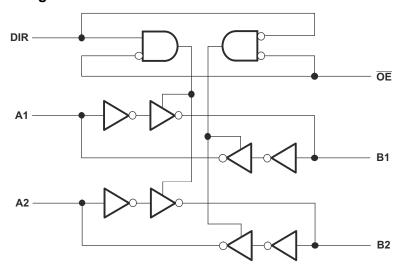


Figure 7-1. Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design

The fully configurable dual-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range. Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2V and 3.6V; thus, making the device an excellent choice for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Supports High Speed Translation

The SN74AVC4T245 device can support high data rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

7.4 Device Functional Modes

Table 7-1. Function Table (Each 2-Bit Section)

CONTRO	L INPUTS	OUTPUT (CIRCUITS	OPERATION ⁽¹⁾		
ŌĒ	DIR	A PORT	B PORT	OPERATION		
L	L	Enabled	Hi-Z	B data to A bus		
L	Н	Hi-Z	Enabled	A data to B bus		
Н	X	Hi-Z	Hi-Z	Isolation		

(1) Input circuits of the data I/Os are always active.

Product Folder Links: SN74AVC4T245

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC4T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T245 device is an excellent choice for applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380Mbps when device translates a signal from 1.8V to 3.3V.

8.2 Typical Application

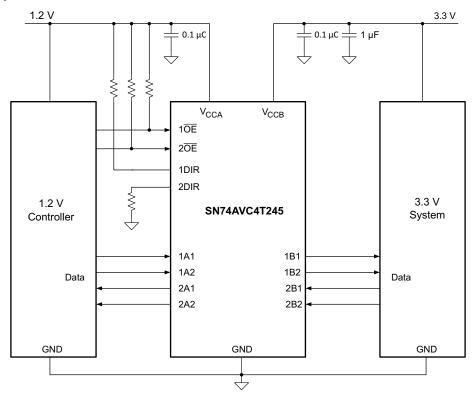


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

For the design example shown in Section 8.2 use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2V to 3.6V
Output voltage range	1.2V to 3.6V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- · Input voltage range
 - Use the supply voltage of the device that is driving the SN74AVC4T245 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
 - Use the supply voltage of the device that the SN74AVC4T245 device is driving to determine the output voltage range.

8.2.3 Application Curves

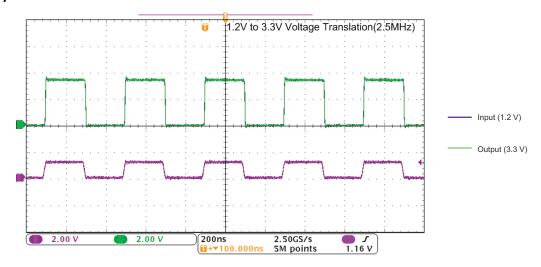


Figure 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz

8.3 Power Supply Recommendations

The SN74AVC4T245 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB} . V_{CCA} accepts any supply voltage from 1.2V to 3.6V and V_{CCB} accepts any supply voltage from 1.2V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V and 3.3V voltage nodes.

The output-enable (\overline{OE}) input circuit is designed so that V_{CCA} supplies \overline{OE} , and when the \overline{OE} input is high, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, the \overline{OE} input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pullup resistor to V_{CCA} .

Product Folder Links: SN74AVC4T245

8.4 Layout

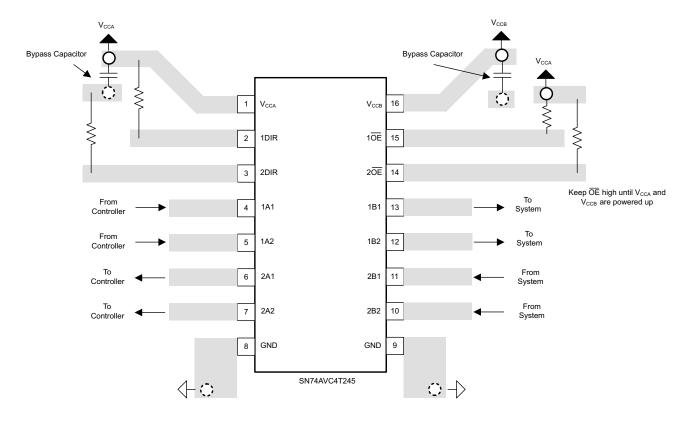
8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines, such as follows:

- · Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

8.4.2 Layout Example





9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on Notifications to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (March 2024) to Revision I (February 2025)							
Updated PW and RGY thermal information	8						
Changes from Revision G (November 2014) to Revision H (March 2024)	Page						
Updated the numbering format for tables, figures, and cross-references throughout the document	1						
Added the BQB and DYY package information throughout the data sheet							
Added the bod and bit i package information throughout the data sheet	1						
Updated the package information table to include package lead size							

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: SN74AVC4T245

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23-May-2025

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
74AVC4T245DGVRE4	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
74AVC4T245RGYRG4	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245
74AVC4T245RSVR-NT	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU
74AVC4T245RSVR-NT.A	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZWU
74AVC4T245RSVR-NT.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZWU
74AVC4T245RSVRG4	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU
SN74AVC4T245BQBR	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245BQBR.A	Active	Production	WQFN (BQB) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245
SN74AVC4T245D.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVC4T245
SN74AVC4T245DG4.B	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVC4T245
SN74AVC4T245DGVR	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245DGVR.B	Active	Production	TVSOP (DGV) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245
SN74AVC4T245DR.B	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVC4T245
SN74AVC4T245DRE4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245
SN74AVC4T245DT	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245
SN74AVC4T245DT.B	Active	Production	SOIC (D) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVC4T245
SN74AVC4T245DYYR	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245DYYR.A	Active	Production	SOT-23-THIN (DYY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245PW	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PW.B	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245PWE4	Active	Production	TSSOP (PW) 16	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245PWR.B	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245PWRE4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PWRG4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245



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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74AVC4T245PWT	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PWT.B	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245
SN74AVC4T245PWTE4	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245PWTG4	Active	Production	TSSOP (PW) 16	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245
SN74AVC4T245RGYR	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245
SN74AVC4T245RGYR.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT245
SN74AVC4T245RGYR.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT245
SN74AVC4T245RGYRG4.A	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT245
SN74AVC4T245RGYRG4.B	Active	Production	VQFN (RGY) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WT245
SN74AVC4T245RSVR	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU
SN74AVC4T245RSVR.A	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZWU
SN74AVC4T245RSVR.B	Active	Production	UQFN (RSV) 16	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZWU

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC4T245:

Automotive: SN74AVC4T245-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter	Reel Width	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
					(mm)	W1 (mm)	` ′	_ ` ′	` ,	` ′	` ,	
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	180.0	8.4	2.0	2.8	0.7	4.0	8.0	Q1
SN74AVC4T245BQBR	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AVC4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVC4T245DYYR	SOT-23- THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74AVC4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T245RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1



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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	189.0	185.0	36.0
74AVC4T245RSVR-NT	UQFN	RSV	16	3000	200.0	183.0	25.0
SN74AVC4T245BQBR	WQFN	BQB	16	3000	210.0	185.0	35.0
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AVC4T245DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AVC4T245DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74AVC4T245PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AVC4T245PWT	TSSOP	PW	16	250	356.0	356.0	35.0
SN74AVC4T245RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0
SN74AVC4T245RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AVC4T245D	D	SOIC	16	40	507	8	3940	4.32
SN74AVC4T245D.B	D	SOIC	16	40	507	8	3940	4.32
SN74AVC4T245DG4.B	D	SOIC	16	40	507	8	3940	4.32
SN74AVC4T245PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74AVC4T245PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74AVC4T245PWE4	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

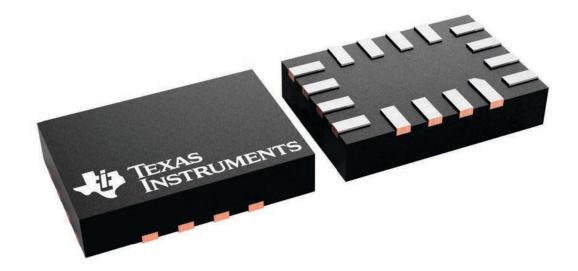
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



1.8 x 2.6, 0.4 mm pitch

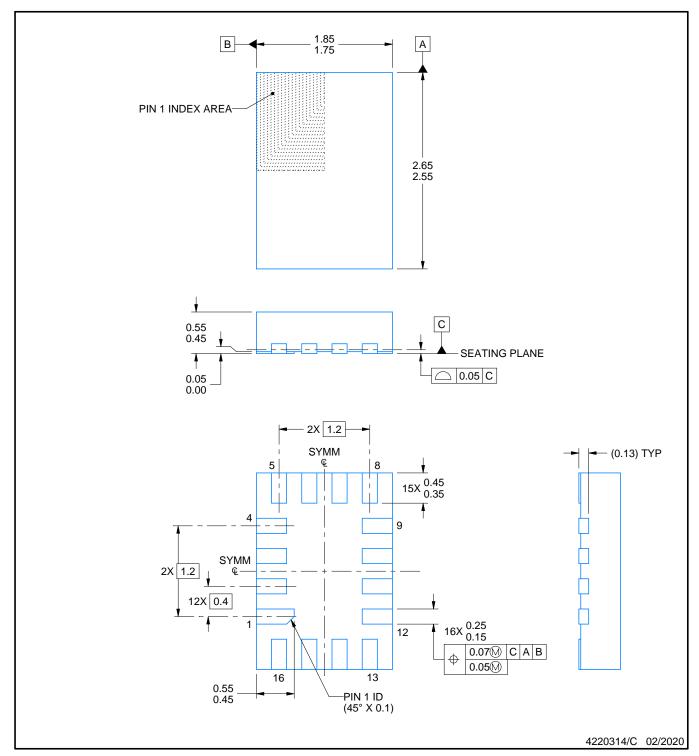
ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





ULTRA THIN QUAD FLATPACK - NO LEAD

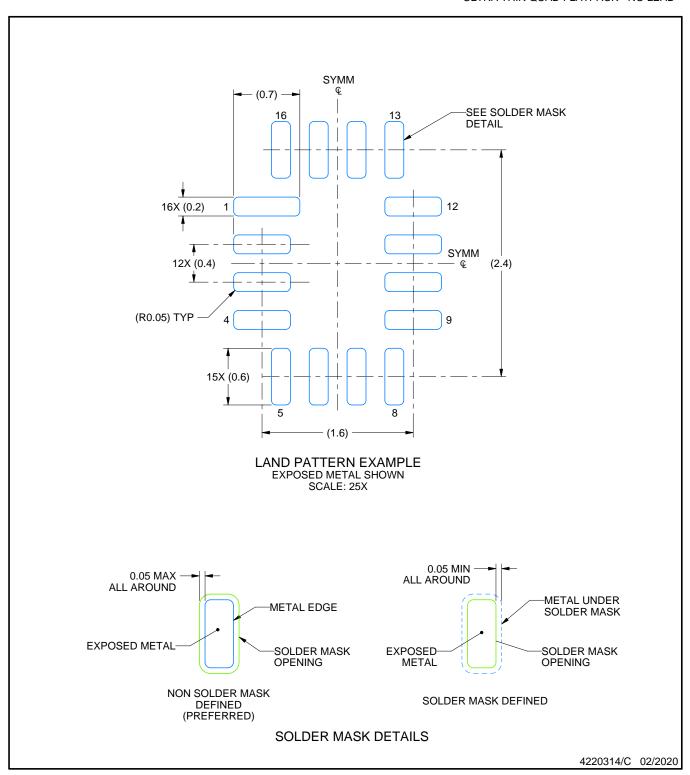


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.



ULTRA THIN QUAD FLATPACK - NO LEAD

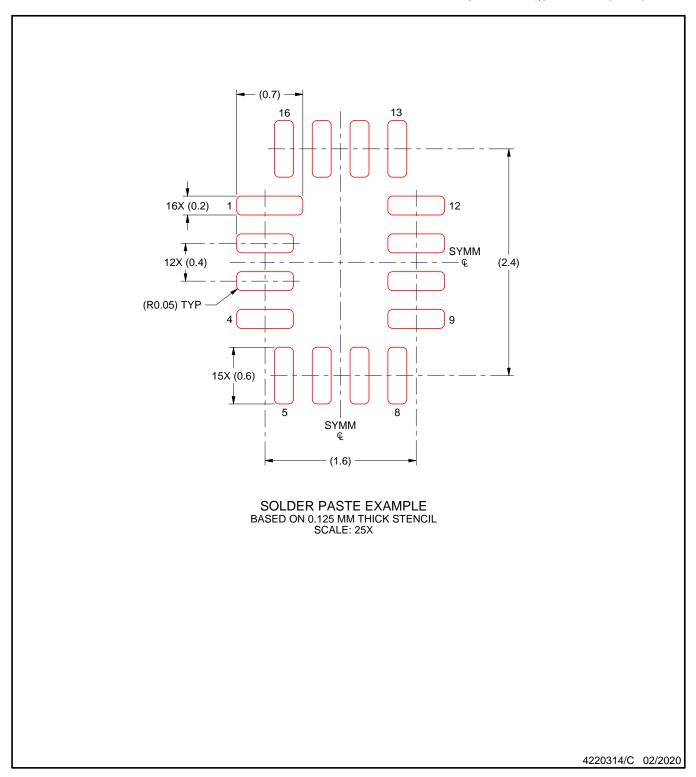


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



ULTRA THIN QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194 2.5 x 3.5, 0.5 mm pitch

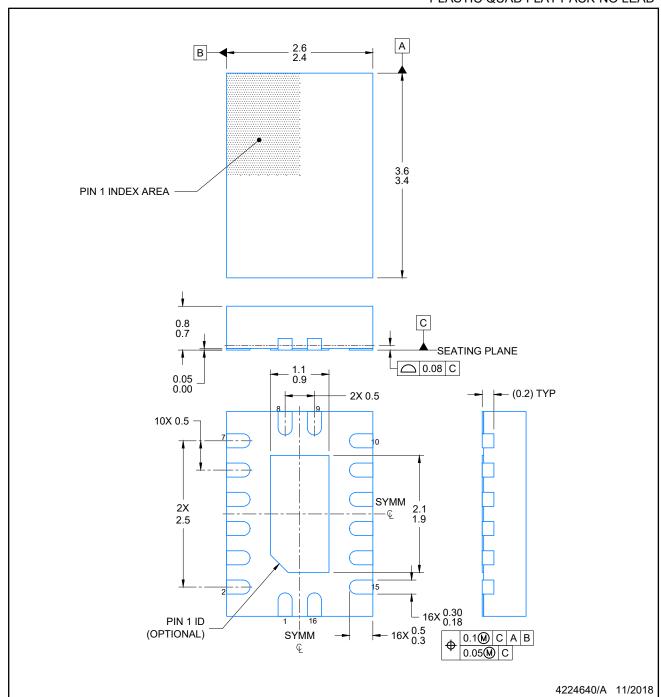
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



INSTRUMENTS www.ti.com

PLASTIC QUAD FLAT PACK-NO LEAD

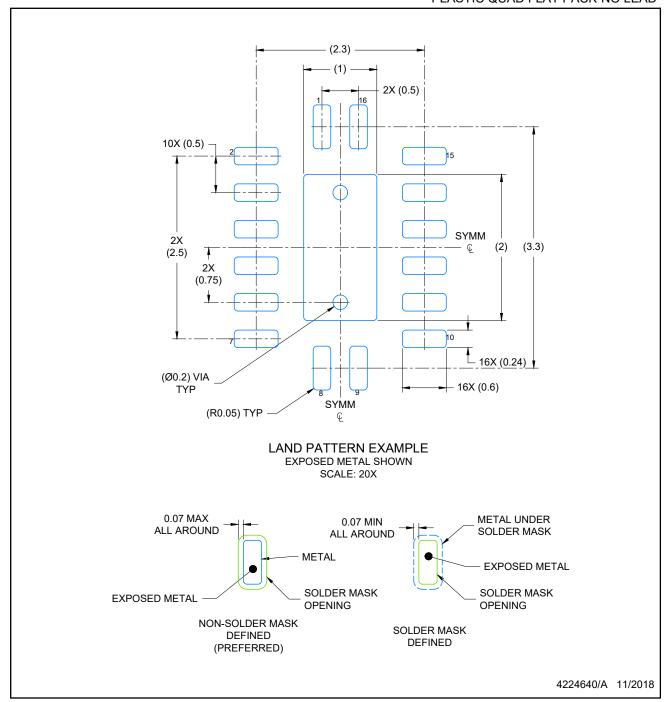


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



PLASTIC QUAD FLAT PACK-NO LEAD

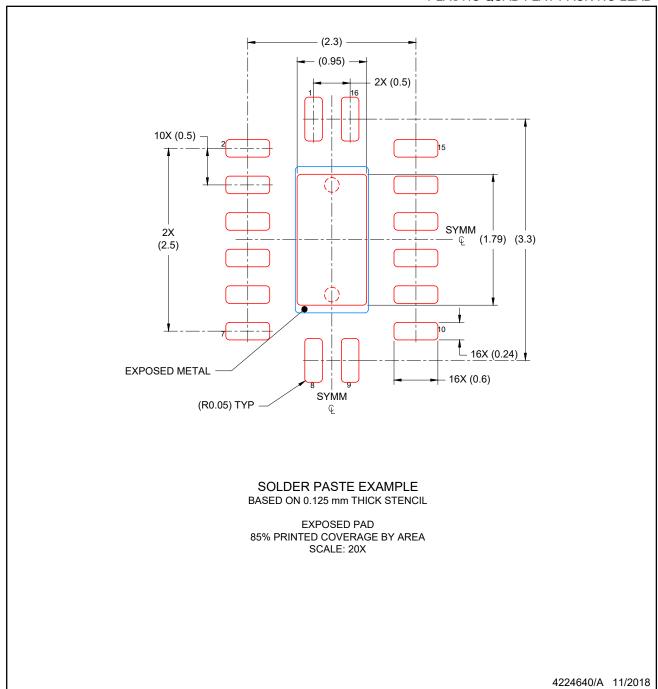


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLAT PACK-NO LEAD

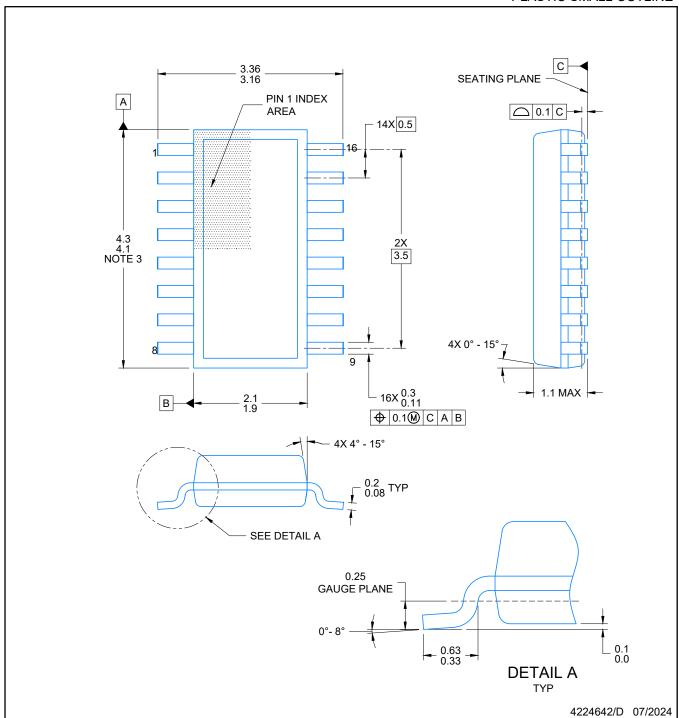


NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



PLASTIC SMALL OUTLINE

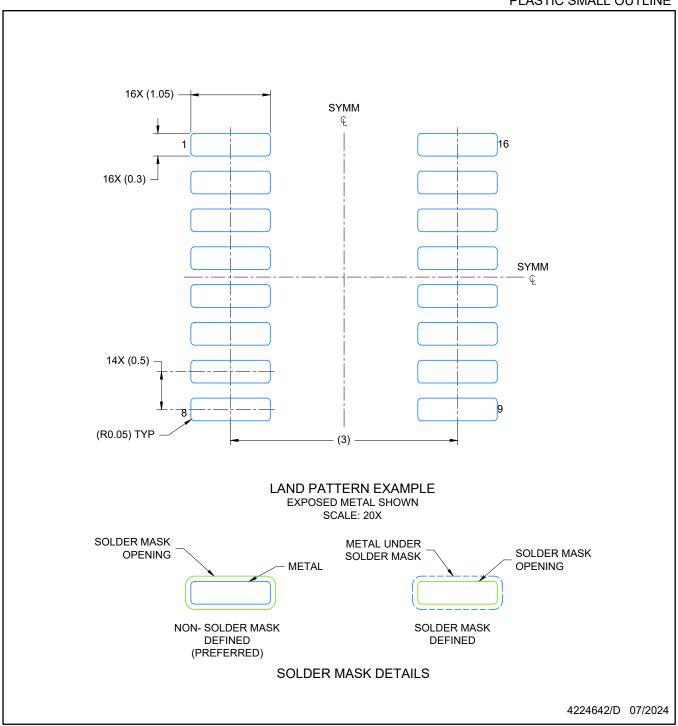


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AA



PLASTIC SMALL OUTLINE

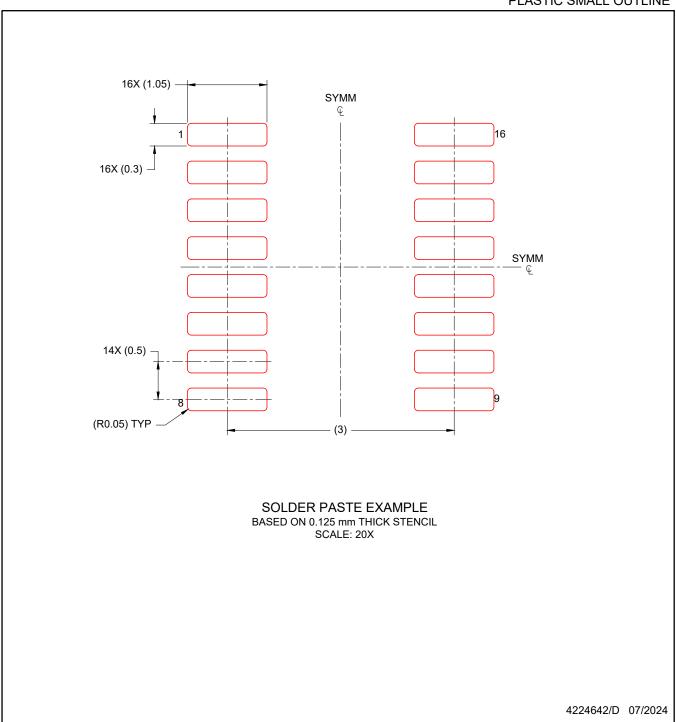


NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com http://www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



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