Application Report
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PCM6xx0-Q1 Sampling Rates and Programmable Processing Blocks Supported

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ABSTRACT

This document describes the available processing blocks in the decimation filter chain of the PCM6xx0-Q1 family of devices, such as the PCM6260-Q1, PCM6240-Q1, PCM6360-Q1, PCM6340-Q1, and PCM6480-Q1. It also explains which configurations of the processing blocks are supported as a function of the sample rate and number of channels.

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1 Introduction

The PCM6xx0-Q1 is a family of multichannel, automotive qualified, audio analog-to-digital converters (ADCs) that includes a highly flexible signal chain with programmable digital processing blocks, making it suitable for a wide variety of automotive applications. Each channel of the PCM6xx0-Q1 device follows the signal processing chain shown in Figure 1. Each channel of the PCM6xx0-Q1 supports an analog differential or single-ended signal or in the case of PCM6480-Q1, up to four pulse density modulation (PDM) digital microphones. In PCM6xx0-Q1 device families, the analog input signal is amplified by a Programmable Gain Amplifier (PGA) and then converted by a high-performance ADC into a digital signal. The PGA gains the input signal to match the full scale of the ADC. The digital signal has a programmable phase calibration to adjust the phase delay of each channel in steps of one modulator clock cycle. This allows the system to match the phase across different channels. The phase-calibrated digital signal is then decimated through a set of linear phase filters or low-latency filters. DC offset is removed from the decimated signal through a Digital High Pass Filter (HPF) with three pre-set cutoff frequencies or a fully programmable cutoff frequency. Note that DC shifts are caused by mismatches in common-mode voltages. The output of the HPF is gain calibrated with 0.1 dB steps and summed with other channels.

The gain calibration matches the gain across different channels, particularly if the channels have microphones with varying gain values. The output is then filtered by the Digital Biquad Filters and gained by the volume control. These device families also support a mixed-signal Automatic Gain Controller (AGC) algorithm for level management of the recorded audio. These features all share the same fixed processing resources. Therefore, the number of channels enabled, the nature of the channel (analog or digital) and the sample-rate determine the configuration possibilities for the processing blocks and filters.

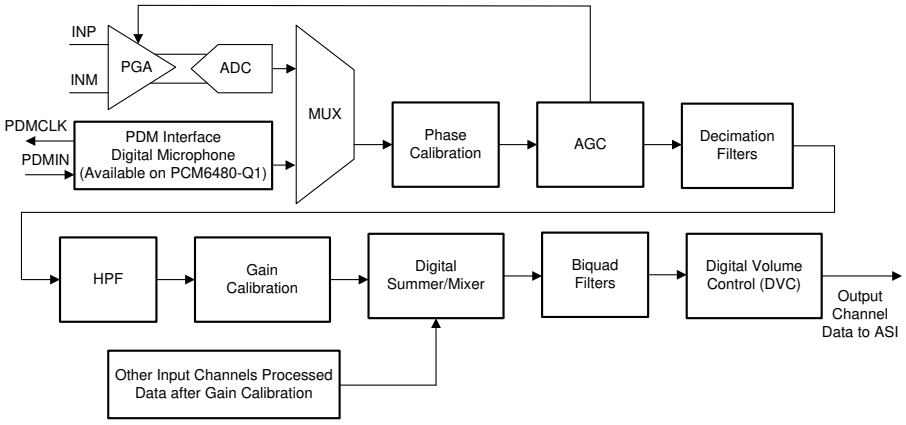

Figure 1. PCM6xx0-Q1 Channel Signal Chain Processing Flow Chart

The PCM6xx0-Q1 device family supports two sets of sample rates. One set of sample rates cover the nine sub-multiples and multiples of 48 kHz, from 8 kHz to 768 kHz. The other set of nine sample rates support the sub-multiples and multiples of 44.1 kHz, from 7.35 kHz to 705.6 kHz. This application note only refers to the set of 48-kHz sample rates, but they are equally applicable to the corresponding sample rate from the set of 44.1-kHz sample rates. For example, features supported for the 8-kHz sample rate are also supported for 7.35 kHz.

Section 2 reviews the processing blocks, configuration options and input channels they are supported on, and the supported sample rates. Section 3 reviews the channel combinations that are supported for different sample rates, and the processing blocks that are supported for the given channel combination.

2 PCM6xx0-Q1 Processing Blocks

The following sections describe the device configurations required to use:

- Decimation filters
- AGC
- Programmable biquads
- Summers
- Digital mixers

2.1 Decimation Filter Mode

The decimation filter processes the over-sampled data from the multi-bit delta-sigma modulator and generates the output PCM samples at the FSYNC rate. In the case of digital channels, the single-bit pulse-density modulated (PDM) stream from the digital microphone is the input to the decimation filter. DECI_FILT, P0_R107_D[5:4] register selects between three types of decimation filters: linear phase, low latency, or ultra-low latency. Table 1 shows the register settings for selecting the desired decimation filter mode for all channels.

Table 1. Decimation Filter Mode Selection for the Record Channel

P0_R107_D[5:4] : DECI_FILT[1:0]	Decimation Filter Mode Selection
00 (default)	Linear phase decimation filters
01	Low-latency approximately linear phase decimation filters

Table 1. Decimation Filter Mode Selection for the Record Channel (continued)

P0_R107_D[5:4] : DECI_FILT[1:0]	Decimation Filter Mode Selection
10	Ultra-low latency decimation filters
11	Reserved

2.1.1 Supported Sample Rates

The response of the default decimation filter is linear phase. It is supported for all sample rates from 8 kHz to 768 kHz. The low latency and ultra-low latency responses are supported for a subset of the sample rates as Table 2 shows. In this table, unsupported decimation filter types are marked as 'NA'. For supported filter types, Table 2 lists the maximum channel count. Note that 8 channels are only available on PCM6480-Q1, while PCM6x60-Q1 and PCM6x40-Q1 devices support no more than 6 channels and 4 channels respectively. Therefore, for PCM6x60-Q1 and PCM6x40-Q1 devices, replace 8 with 6 and 4 respectively. In some cases, to support the channel count shown in Table 2 certain processing blocks may have to be disabled, as Section 3 shows.

Table 2. Maximum Number of Channels Supported for Each Decimation Filter Type

Sample Rate (kHz)	Linear Phase	Low Latency	Ultra-Low Latency
8	8	8	NA
16	8	8	8
24	8	8	8
32	8	8	8
48	8	8	8
96	4	4	4
192	4	3	3
384	2	NA	2
768	1	NA	NA

2.2 AGC

Automatic Gain Control (AGC) is an algorithm that dynamically controls the gain of the ADC channel to maintain a nominally constant output level. AGC is available on all PCM6XX0-Q1 device variants, but only for analog channels since it utilizes the PGA in the analog blocks to dynamically change the input gain. Setting the AGC_SEL bit (shown in Table 3) in DSP_CFG1 (P0_R106_D[3]) enables the AGC.

Table 3. AGC Selection Register Field Description

P0_R106_D[3] : AGC_SEL[1:0]	AGC Selection
0 (default)	AGC is not selected
1	AGC is selected

2.2.1 Supported Sample Rates

AGC supports sample rates from 16 kHz to 192 kHz, but not 8 kHz, nor 384 kHz and 768 kHz sample rates, as Table 4 shows.

2.2.2 Channel Count

Enabling the AGC algorithm increases the processing requirements from the digital engine and can limit the number of channels. Table 4 shows the maximum number of channels supported by the device when AGC is enabled.

Table 4. Number of Channels Supported with AGC Enabled

Sample Rate (kHz)	Number of Channels Supported With AGC Enabled
8	Not supported
16	6
24	6
32	6
48	4
96	2
192	1
384, 768	Not supported

2.3 Digital Signal Processing Blocks (Digital Mixer or Summer, and Biquads)

The device supports one four-channel mixer or two channel-summation modes, with up to three biquads per channel for all sample rates from 8 kHz to 192 kHz. See Table 5 for configuration details of the summer and mixer modes. Clearing CH_SUM[2:0] enables the programmable channel mixer feature for input channel 1 to channel 4. The mixer function is only supported for input channel 1 to channel 4.

The number of biquad filters per channel can be set using the P0_R108:BQ_CFG bits, as Table 6 shows. For additional information on biquad filter configuration, see the *PCM6xx0-Q1 Programmable Biquad Filter Configuration and Applications Application Report*.

Table 5. Channel Summing Mode and Digital Mixer Programmable Settings

P0_R107_D[3:2] : CH_SUM[1:0]	Channel Summing Mode for Input Channels
00 (Default)	Channel summing mode is disabled (Digital mixer is enabled).
01	Output channel 1 = (input channel 1 + input channel 2) / 2
	Output channel 2 = (input channel 1 + input channel 2) / 2
	Output channel 3 = (input channel 3 + input channel 4) / 2
	Output channel 4 = (input channel 3 + input channel 4) / 2
10	Output channel 1 = (input channel 1 + input channel 2 + input channel 3 + input channel 4) / 4
	Output channel 2 = (input channel 1 + input channel 2 + input channel 3 + input channel 4) / 4
	Output channel 3 = (input channel 1 + input channel 2 + input channel 3 + input channel 4) / 4
	Output channel 4 = (input channel 1 + input channel 2 + input channel 3 + input channel 4) / 4
11	Reserved

Table 6. Biquad Configuration Settings

P0_R108_D[6:5] : BQ_CFG[1:0]	Biquad Configuration
00 (Default)	No biquads per channel; biquads are all disabled
01	1 biquad per channel
10	2 biquads per channel
11	3 biquads per channel

Table 7 lists the processing blocks that are available for a given input channel. '√' denotes supported blocks while 'x' denotes unsupported blocks. These assignments are fixed and cannot be changed. The two-channel summer mode is available for the first six channels, and cannot be assigned to channels 7 and 8, even if some of the other channels are disabled. Similarly, the four-channel mixer, four-channel summer, and three biquads per channel are only available for the first four channels. Input channels 1 to 4 support the most processing blocks, while channels 7 and 8 support the least number of processing blocks.

Table 7. Processing Block Assignments Across Input Channels

Post-Processing Block	1	2	3	4	5	6	7	8
Two-channel Summer	√	√	√	√	√	√	x	x
Four-channel Summer	√	√	√	√	x	x	x	x
Four-channel Mixer	√	√	√	√	x	x	x	x
Biquads Available	3	3	3	3	3	3	1	1

3 Processing Blocks Supported for Different Sample Rates

This section describes the specific processing blocks available for different sample rates. Table 8 shows the channel combinations supported for different sampling rates.

Table 8. Channel Combinations Supported for Different Sample Rates with PLL Enabled

Sample Rate (kHz)	Decimation Filter Mode	AGC	#Biquads/Channel	Maximum Supported Channel Combination
8	Linear Phase	Disabled	None(disabled), 1, 2 or 3	8
16,24,32	Linear Phase, Low Latency, or Ultra-Low Latency	Enabled or Disabled	None(disabled), 1, 2 or 3	8
48	Linear Phase, Low Latency, or Ultra-Low Latency	Disabled	None(disabled), 1, 2 or 3	8
		Enabled	None(disabled), 1, 2 or 3	4
96	Linear Phase, Low Latency, or Ultra-Low Latency	Disabled	None(disabled), 1, 2	4
			3	3
		Enabled	None(disabled)	2
			None(disabled), 1, 2 or 3	1
192	Linear Phase	Disabled	None(disabled)	4
		Enabled	None(disabled)	1
	Low Latency, or Ultra-Low Latency	Disabled	None(disabled)	3
		Enabled	None(disabled)	1
384	Linear Phase or Ultra-Low Latency	Disabled	None(disabled)	2
768	Linear Phase	Disabled	None(disabled)	1

3.1 8 kHz Sample Rate

Only the linear phase (default) decimation filter response is supported for the 8 kHz sample rate. Supported processing blocks include biquads, digital mixer, and channel summer. AGC is not supported for the 8 kHz sample rate. Biquads, channel summers, and digital mixer blocks are supported on the respective input channels (Table 7).

3.2 16 kHz–48 kHz Sample Rate

All processing blocks and digital filter options are supported for the sample rates from 16 kHz to 48 kHz.

The decimation filter can be configured to linear phase, low latency, or ultra-low latency. AGC is supported for all analog channels. Biquads, channel summers, and digital mixer blocks are supported on their respective input channels (Table 7). For 48-kHz operation, the maximum number of supported channels is reduced to four when AGC is enabled along with biquads. If biquads are disabled, one additional channel can be enabled with AGC, taking the total to five.

3.3 96 kHz Sample Rate

All three decimation filter options are supported for 96-kHz operation. AGC is supported with 2 channels when biquad is disabled. Otherwise, AGC is supported with 1 channel with up to 3 biquads enabled. 4 channels are supported when AGC is disabled and up to 2 biquads per channel. The number of supported channels reduce to 3, when biquads per channel is increased to 3.

3.4 192 kHz Sample Rate

All three decimation filter options are supported for 192-kHz operation.

For the low latency (and ultra-low latency) decimation filter response option, a maximum of three channels are supported when AGC is disabled. For linear phase decimation filter, with AGC disabled the number of supported channels increases to 4. Only one channel is supported when AGC is enabled. Biquads, channel summers, and digital mixer are not supported for this mode.

3.5 384 kHz Sample Rate

Linear phase (DECI_FILT = 00) and ultra-low latency (DECI_FILT = 10) decimation filter responses are supported for the 384 kHz sample rate. AGC and DRE, biquads, channel summers, and digital mixer blocks are not supported for 384-kHz operation. A maximum of two channels are supported for 384 kHz and they can be analog, digital, or a combination of both.

3.6 768 kHz Sample Rate

Only linear phase (DECI_FILT = 00) decimation filter response is supported for the 768 kHz sample rate. AGC and DRE, biquads, channel summers, and digital mixer blocks are not supported. Just one channel is supported. It can be an analog channel or a digital PDM microphone.

4 Example Configurations

Device configuration scripts for different combinations are presented in *Example 1* and *Example 2*.

Example 1: Two input channels with four output channels using digital mixer.

1. Differential 2-channel input
2. Linear phase decimation filter
3. 24-bit TDM mode
4. Enable digital mixer mode
5. Digital Mixer 3: Ch3 Out = 0.5×Ch1 + 0.5×Ch2
6. Digital Mixer 4: Ch4 Out = 0.5×Ch1 – 0.5×Ch2

```
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# Differential 2-channel 24-bit TDM mode : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
#

w 90 00 00 # Goto Page 0
w 90 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG

w 90 6B 01          # Linear Phase Decimation Filter with digital mixer

# Digital Mixer 3 Configuration
```

```
w 90 00 04          # Goto Page 4
w 90 28 40 00 00 00 # Digital Mixer 3: Channel 1 Coefficient (MIX3_CH1) = 0.5
w 90 2C 40 00 00 00 # Digital Mixer 3: Channel 2 Coefficient (MIX3_CH2) = 0.5
w 90 30 00 00 00 00 # Digital Mixer 3: Channel 3 Coefficient (MIX3_CH3) = 0.0
w 90 34 00 00 00 00 # Digital Mixer 3: Channel 4 Coefficient (MIX3_CH4) = 0.0

# Digital Mixer 4 Configuration
w 90 00 04          # Goto Page 4
w 90 38 40 00 00 00 # Digital Mixer 4: Channel 1 Coefficient (MIX4_CH1) = 0.5
w 90 3C C0 00 00 00 # Digital Mixer 4: Channel 2 Coefficient (MIX4_CH2) = -0.5
w 90 40 00 00 00 00 # Digital Mixer 4: Channel 3 Coefficient (MIX4_CH3) = 0.0
w 90 44 00 00 00 00 # Digital Mixer 4: Channel 4 Coefficient (MIX4_CH4) = 0.0

w 90 00 00 # Goto Page 0
w 90 07 20 # TDM Mode with 24 Bits/Channel
w 90 73 c0 # Enable Ch.1 - Ch.2
w 90 74 f0 # Enable Ch.1 - Ch.4 ASI Output channels
w 90 75 e0 # Power up ADC
```

Example 2: Four input channels with channel summer.

1. Differential 4-channel input
2. Linear phase decimation filter
3. 32-bit TDM mode
4. Two-channel summer mode

```
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 4-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2, INP3/INM3 - Ch3 and INP4/INM4 - Ch4
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
#################################################################
#
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
#

w 90 00 00 # Goto Page 0
w 90 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG

w 90 6B 05 # Linear Phase Filter with 2 channel summer mode (DSP_CFG0)

w 90 00 00 # Goto Page 0
w 90 07 30 # TDM Mode with 32 Bits/Channel
w 90 73 f0 # Enable Ch.1 - Ch.4
w 90 74 f0 # Enable ASI Output channels
w 90 75 e0 # Power up ADC
```

5 References

- Texas Instruments, *PCM6xx0-Q1 Automotive, 4-Channel and 6-Channel, 768-kHz, Audio ADC With Integrated Microphone Bias and Input Fault Diagnostics Data Sheet*
- Texas Instruments, *PCM6xx0-Q1 Programmable Biquad Filter Configuration and Applications Application Report*

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