Application Brief **Optimizing Optical Network Terminal Units With Logic**



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Functional Block Diagram

For the purpose of this brief, a simplified Optical Network Terminal unit (ONT) block diagram is used to illustrate the logic and translation use cases, see Simplified Block Diagram for Optical Network Terminal Units. Each red block has an associated use-case document. Links are provided in Table 1 and Table 2. For a more complete block diagram, see the interactive online end equipment reference diagram for Optical Network Terminal units.



Figure 1. Simplified Block Diagram for Optical Network Terminal Units

Logic and Translation Use Cases

Each use case is linked to a separate short document that provides additional details including a block diagram, design tips, and part recommendations. The nearest block and use-case identifiers are listed to match up exactly to the use cases shown in the provided *simplified block diagram*.

1



Nearest Block	Use-Case Identifier	Use Case			
Non-Isolated DC/DC Power Supply	Supply Sequence	Power Sequencing With RC Circuits and Schmitt-Trigger Logic			
Processing	Timed Restart	Reset a System for a Short Time			
	Combine Error Signals	Combine Error Signals			
Table 2. Translation Use Cases					

Nearest Block	Use-Case Identifier	Use Case		
Sensing	I2C	Translate Voltages for I2C		
RS-232, ZigBee®	UART	Translate Voltages for UART		

Power Sequencing With RC Circuits and Schmitt-Trigger Logic

Optical Network Terminal units (ONTs) have multiple internal modules that can be operating at different voltages and require specific power-up sequencing to prevent spurious data from being sent during the system start-up. In many cases, simple logic gates and RC delays can be used to provide a power-up sequence.

The RC delays produce signals that are too slow for standard CMOS inputs, so logic parts with Schmitt-trigger inputs are required for this application. Fortunately, TI has the HCS logic family which has Schmitt-trigger architecture on every input, so any required logic function is available for use.

AND gates are the most common gate used for logic sequencing. Figure 2 shows an example circuit with 2 input power good signals and three delayed output stages. When PG1 goes high, there is a short delay ($t_1 = R_1 \times C_1$) after which PG2 can directly enable stage one. When PG2 becomes high, stage 1 immediately is activated and the timer for stage two begins ($t_2 = 2 \times R_2 \times C_2$), which then activates stage 2, and finally, after a short delay ($t_3 = R_3 \times C_3$), stage 3 is activated. The connection of PG1 provides an immediate disable signal to stages two and three, while stage 1 takes a short time (t_1) to become disabled. If PG2 becomes low, stage 1 is immediately disabled and stages two and three are disabled after their sequential delays; the same as during the start-up.

Of course, this is just one example. There are infinitely many combinations that can be achieved using discrete logic, and the HCS family enables you to build your own design with reliable operation, low size, and maximum flexibility.



Figure 2. Example Logic Circuit for Sequencing Components

See more about a similar use case in the *Combine Power Good Signals* application report and the *Logic Minute* video *Combining Power Good Signals*.

- Schmitt-trigger input architecture is required for having slow transitioning input signals; a dedicated Schmitt-trigger buffer can be added if a logic gate does not include Schmitt-trigger input architecture
- The best practice is to power the start-up sequence logic gates directly from the primary power source or from a dedicated low I_Q LDO regulator so the logic is powered before all other circuitry
- All HCS logic family devices include positive input clamp diodes, so be sure to add a series resistor to any inputs that can exceed VCC + 0.5 V. Choose resistor values based on the input voltage (V_{IN}), forward voltage (V_F, typically 0.65 V), gate supply voltage (V_{CC}) and maximum clamp diode current (I_{IK}) per the following equation: $R > \frac{V_{IN} V_{CC} V_F}{I_{IK}}$
- Need additional assistance? Ask our engineers a question on the *TI E2E™ Logic Support Forum*



Table 3. Recommended Parts						
Part Number	Automotive Qualified	V _{CC} Range	Туре	Features		
SN74HCS08-Q1	1			Schmitt-trigger inputs		
SN74HCS08		2 V – 6 V	Quad AND gate	Positive input clamp diodes on all pins; add series resistors if input voltage exceeds V_{CC}		
SN74LVC1G17-Q1	1	1.65 V – 5.5 V	Schmitt-trigger buffer	Schmitt-trigger inputs		
SN74LVC1G17				Inputs are over-voltage tolerant; signals can exceed V_{CC}		
SN74LVC1G57		1.65 V – 5.5 V	Configurable Logic Gate	Schmitt-trigger inputs		
SN74LVC1G58				Between the '1G57 and '1G58, all 2-input logic gate functions can be produced. See data sheets for details.		
SN74LV14A-Q1	1	2 V – 5.5 V		Schmitt-trigger inputs		
SN74LV14A			Hex inverter	Overvoltage tolerant inputs Partial power-down support (I _{off}) Improved noise characteristics		
SN74LV08A-Q1	1			Over-voltage tolerant inputs		
SN74LV08A		2 V – 5.5 V	Quad AND gate	Partial power-down support (I _{off}) Improved noise characteristics		
SN74AUP1G57			Configurable Logic Gate	Schmitt-trigger inputs		
SN74AUP1G58		0.8 V – 3.6 V		Ultra low-power operation (0.6 μA max $I_{CC})$ Overvoltage tolerant inputs		

For more devices with Schmitt-trigger input architecture, browse the *online parametric tool* which can be sorted by the desired voltage, output current, and other features.

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