Application Report
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Using ADS8410/13 in Cascade Mode

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ABSTRACT

Many applications require multiple analog-to-digital converters (ADC) in a system. Cascading multiple ADCs enables the use of a single data receiver or a small FPGA. This offers lower power consumption and independent ADC usage. This application report describes how multiple ADCs (ADS8410/13) work in a cascade mode. The ADS8410/13 integrated circuit offers a high-speed (200 Mbps) LVDS serial interface. This report also suggests a way to de-serialize the high-speed serial data. It discusses the board design aspects and test guidelines. It presents reference schematics, layouts for the boards, and the reference board results.

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1 Introduction

In many applications, multiple ADCs are used to convert several analog channels. For stand-alone ADCs (i.e., ADCs without an option for daisy chain or cascade) multiple digital outputs are sometimes multiplexed with a digital multiplexer. In other cases, a high pin-count FPGA or DSP is used to receive multiple digital outputs. To avoid this complexity, the ADS8410/13 offers a cascade mode (explained later in detail) in which data from multiple ADCs are dumped into a single bus and are received with a single de-serializer or an FPGA. Cascading of multiple ADCs offers a power advantage over daisy chaining. Moreover, one or more idle ADCs can be selectively powered down in the system to reduce power even more. The serial LVDS (low-voltage differential signaling) interface offers high-speed (200 Mbps) data transmission to enable the use of more ADCs for a given sampling rate of the ADC. The low differential swing, in LVDS data transmission, causes lower ground bounce in the system and less crosstalk among the digital signals. This helps to achieve a better signal-to-noise ratio in a system.

2 Description of the ADC

The ADS8410 and ADS8413 are 16-bit, 2-MSPS ADCs with a 4-V internal reference. The ADCs include a capacitor-based SAR A/D converter with inherent sample and hold.

These ADCs offer a 200-Mbps serial LVDS interface. The interface is designed to support cascading and daisy chaining of multiple ADCs. There is a mode to select 16/8-bit data frame to interface with shift registers for converting the data to parallel format.

The ADS8410 has a pseudo-differential input stage. The -IN swing of +/- 200 mV is useful for compensating a ground voltage mismatch between the ADC and the sensor and to cancel the common-mode noise.

The ADS8413 has a unipolar differential input range, which supports a differential input swing of –VREF to +VREF with a common mode of +VREF/2. The ADC operates at a lower power when used at lower conversion rates, because of the nap feature. It is available in a 48-pin QFN package.

3 Digital Interface

The ADS8410/13 offers a 200-Mbps LVDS interface. LVDS has current output which terminates at the receiver with a 100-Ω resistor which converts it to voltage. The high speed offers more ADC integration in a system at a given ADC sampling rate. LVDS has a typical differential swing of ±680 mV (680 mV for logic 1 and –680mV for logic 0) which is better in a low-noise system. The differential nature of this signaling filters any common-mode noise.

4 Definition of Cascade

In cascade mode, multiple ADCs are connected in such a fashion that CLK_O (clock output), SDO (digital data output), and SYNC_O (frame sync signal for capturing digital data) of all the ADCs are connected to common CLK_O, SDO, and SYNC_O bus. This means that only one ADC occupies the bus at a particular time, while LVDS outputs of all other ADCs are in a 3-state mode. Unlike SDO and SYNC_O, the clock (CLK_O) is switched out from one ADC only as the receiver requires a continuous clock. So, one ADC outputs the clock (this is called the **Master ADC**; any one - and only one - ADC in the chain can be made master) and CLK_O of all other ADCs are in the 3-state mode by appropriately setting M1+ and M1– input (M1 = logic1 → master, M1 = logic0 → slave).

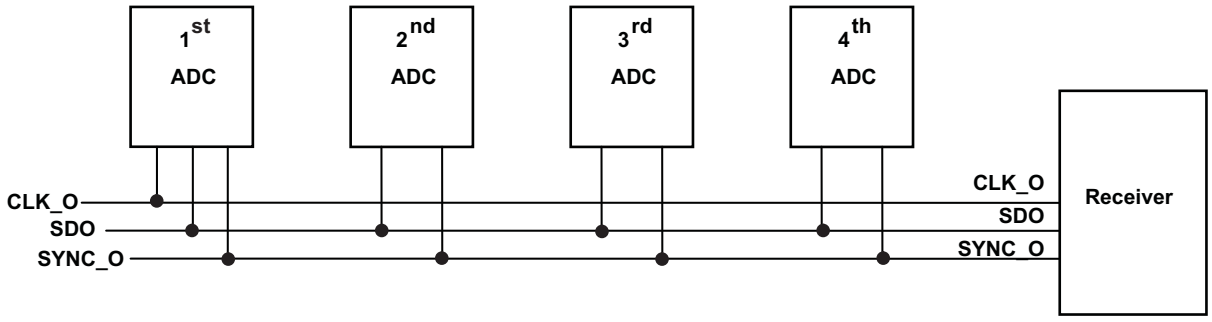


Figure 1. Four ADCs Are Connected in Cascade

5 Block Diagram

Figure 2 and Figure 3 shows four ADS8410/13s, connected in cascade mode. The signals shown with bold lines are LVDS and the lighter lines are CMOS. Cascade mode is selected by setting MODE C/D = 1. The **first ADC** (this ADC offers data **without latency**) in the chain is identified by LAT Y/$\overline{N}$ = 0 (means latency yes or no). For all other ADCs (data **with latency**), LAT Y/$\overline{N}$ = 1. Either $\overline{CSTART}$ (LVDS) or $\overline{CONVST}$ (CMOS) is used as a conversion start signal. Depending on CLK I/$\overline{E}$ signal, a particular ADC either takes in an external clock or generate an internal clock.

The cascade chain can be run with an internal clock or with an external clock.

5.1 Internal Clock Mode

When the internal clock mode is used (see Figure 2), only one ADC generates the internal clock. The clock output (CLK_O) generated from this ADC is not connected to the common clock output bus. This clock is used as external input clock for all the ADCs (including the ADC which has generated it) in cascade and the interface is synchronized with this clock. CLK_O from all other ADCs (except the ADC which has generated the clock) are connected to the common CLK_O bus. One ADC and only one (not necessarily the first ADC, except the ADC which generates the clock) acts as a master ADC (M1 = 1), and all the other ADCs are slave (M1 = 0). The master ADC sends out CLK_O in the common bus. CLK_O from all other ADCs are always in a 3-state mode, and these are connected to the common bus for the purpose of loading. In Figure 2, ADC 3 (CLK I/$\overline{E}$ = 1) generates the common clock for all the ADCs. ADC 2 is used as the **Master ADC** (M1 = logic 1). ADC 1 is identified by LAT Y/$\overline{N}$ = 0.

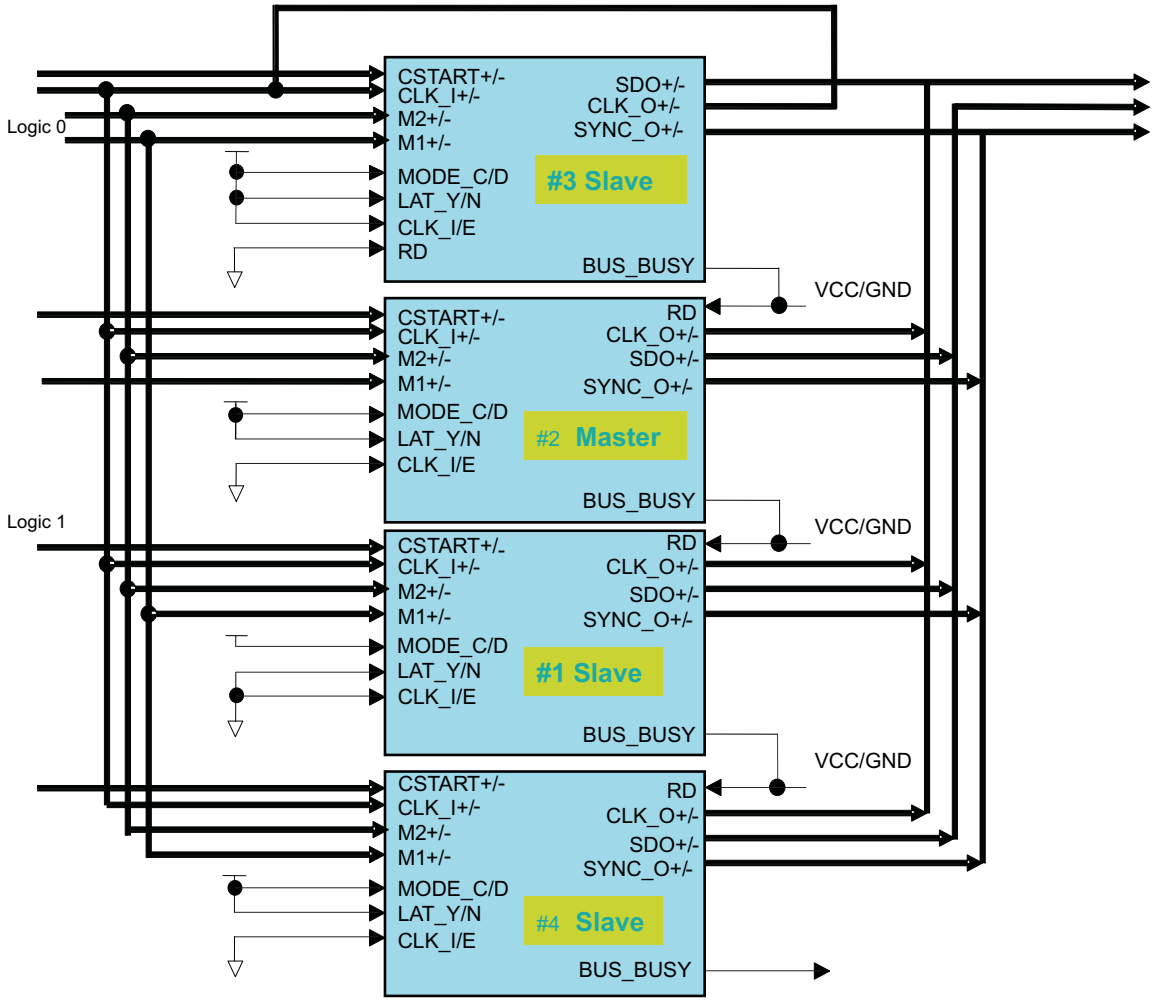


Figure 2. Four ADCs Connected in Cascade With Internal Clock Mode

5.2 External Clock Mode

When an external clock is used (see Figure 3), all the ADCs are fed with the synchronized external clock (CLK_I). Clock output (CLK_O) of all the ADCs are connected to the common CLK_O bus. One ADC and only one (not necessarily the first ADC) acts as a master ADC (M1 = logic 1) and all the other ADCs are slaves (M1 = logic 0). The master ADC always sends out CLK_O in the common bus. CLK_O from all other ADCs are always in a 3-state mode, and these are connected to the common bus for the purpose of loading. In Figure 3, ADC 2 is used as the master ADC.

For both internal and external clock mode, SYNC_O and SDO of all the ADCs are connected to common SYNC_O and SDO bus. BUS_BUSY ($\overline{\text{BUS\_BUSY}}$ = 1 indicates that the ADC is busy sending out serial data to SDO bus) of **first ADC** (LAT Y/$\overline{\text{N}}$ = 0) should be connected to $\overline{\text{RD}}$ ($\overline{\text{RD}}$ = 0 allows an ADC to send out serial data to SDO bus) of second ADC; BUS_BUSY of the second ADC should be connected to $\overline{\text{RD}}$ of third ADC and so on. BUS_BUSY of last ADC should be connected to the $\overline{\text{RD}}$ of first ADC or keep BUS_BUSY of the last ADC floating. $\overline{\text{RD}}$ of the first ADC should be connected to GND in this case.

The ADC has a dual-drive mode in which the ADC can increase the LVDS current to double in case of a lower termination resistor. This mode is selected by M2 = 1. This mode is useful in the case of multiple ADCs connected to a common bus. A detailed explanation is presented later in this document.

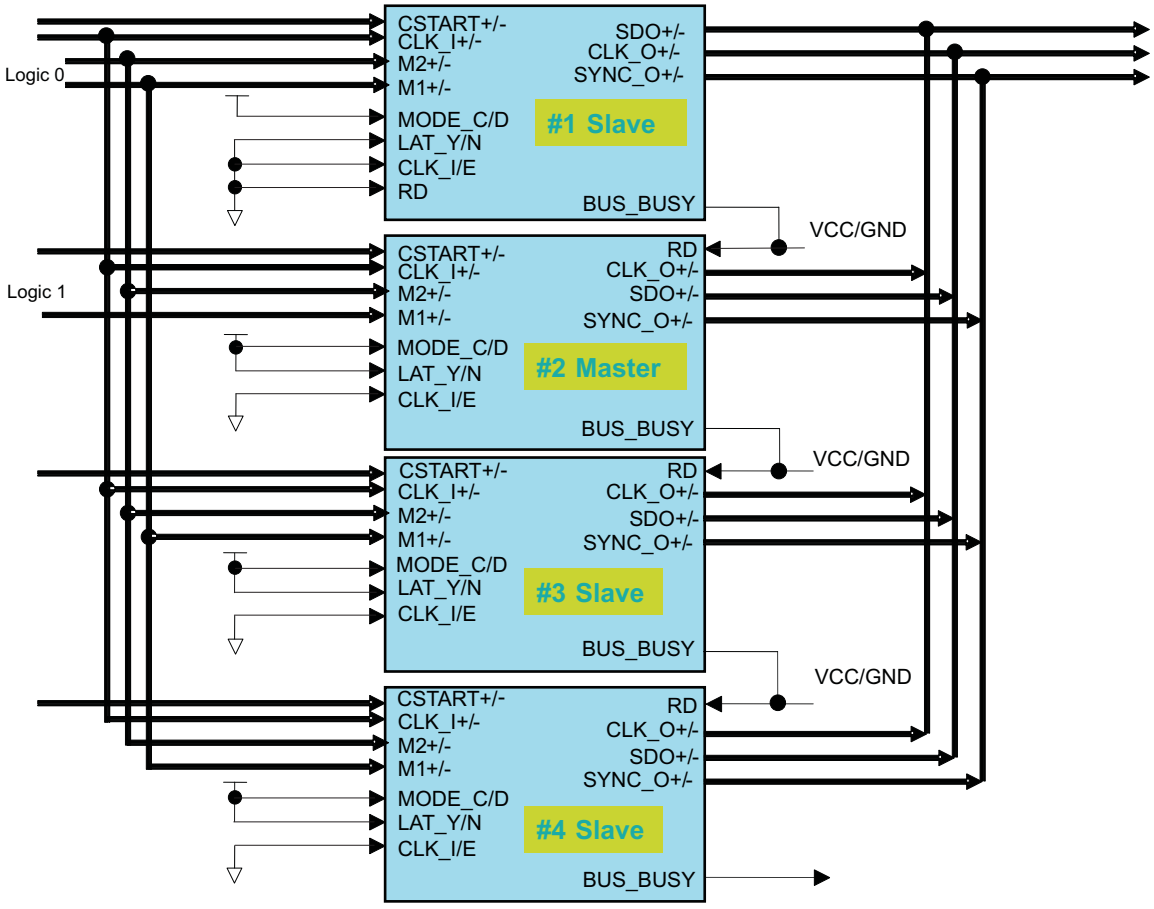


Figure 3. Four ADCs Connected in Cascade With External Clock Mode

6 Timing

6.1 Timing Requirements

The following specifications are typical at –40°C to 85°C, +VA = +5 V, +VBD = +5 V and 3.3 V (unless otherwise noted).

PARAMETER			MIN	TYP	MAX	UNITS
SAMPLING AND CONVERSION RELATED						
t_{acq}	Acquisition time (see Figure 4, Figure 5)		100			ns
t_{conv}	Conversion time (see Figure 4, Figure 5)				391	ns
t_{w1}	Pulse duration, $\overline{\text{CONVST}}$ high (see Figure 4)		100			ns
t_{w2}	Pulse duration, $\overline{\text{CONVST}}$ low (see Figure 4, Figure 5)		40			ns
t_{d1}	Delay time, $\overline{\text{CONVST}}$ rising edge to sample start (see Figure 4)				5	ns
t_{d2}	Delay time, $\overline{\text{CONVST}}$ falling edge to conversion start (see Figure 4, Figure 5)				5	ns
t_{d3}	Delay time, $\overline{\text{CONVST}}$ falling edge to busy high (see Figure 4, Figure 5)	+VBD 5 V			13	ns
		+VBD 3.3 V			14	
t_{d4}	Delay time, conversion end to busy low (see Figure 4, Figure 5)	+VBD 5 V			7	ns
		+VBD 3.3 V			8	
t_{w3}	Pulse duration, $\overline{\text{CSTART}}$ high (see Figure 4 and Table 1)		100			ns
t_{w4}	Pulse duration, $\overline{\text{CSTART}}$ low (see Figure 4, Figure 5 and Table 1)		45			ns

PARAMETER			MIN	TYP	MAX	UNITS
t_{d5}	Delay time, $\overline{\text{CSTART}}$ rising edge to sample start (see Figure 4, Figure 5 and Table 1)				7.5	ns
t_{d6}	Delay time, $\overline{\text{CSTART}}$ falling edge to conversion start (see Figure 4, Figure 5 and Table 1)				7.5	ns
t_{d7}	Delay time, $\overline{\text{CSTART}}$ falling edge to busy high (see Figure 4, Figure 5 and Table 1)	+VBD 5 V			15.5	ns
		+VBD 3.3 V			16.5	
I/O RELATED						
t_{d8}	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to busy high (see Figure 7)				16	ns
t_{d9}	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to SYNC_O and SDO out of 3-state condition (for ADC with LAT_Y/$\overline{\text{N}}$ pulled low)	+VBD 5 V			28	ns
		+VBD 3.3 V			29	
t_{d10}	Delay time, preconversion end (point A) to SYNC_O and SDO out of 3-state condition (see Figure 8)				22	ns
t_{d11}	Delay time, preconversion end (point A) to BUS_BUSY high (see Figure 8)	+VBD 5 V			7	ns
		+VBD 3.3 V			8	
t_{d12}	Delay time, conversion phase end to SYNC_O high (see Figure 8)		6		9 + t_{clk}	ns
t_{d13}	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to SYNC_O high (see Figure 8)	+VBD 5 V	5 + 4× tclk		8 + 5× tclk	ns
		+VBD 3.3 V	5.5 + 4× tclk		8.5 + 5×tclk	
t_{d14}	Delay time, CLK_O rising edge to data valid (see Figure 7, Figure 8)	+VBD 5 V			1.3	ns
		+VBD 3.3 V			1.4	
t_{d16}	Delay time, CLK_O to SDO and SYNC_O 3-state (see Figure 9, Figure 11)				4	
t_{d17}	Delay time, SYNC_O and SDO 3-state to BUS_BUSY low in cascade mode (see Figure 9, Figure 11)		0		2	
t_{d18}	Delay time, $\overline{\text{RD}}$(rising edge to BUS_BUSY high for ADC with LAT_Y/$\overline{\text{N}}$ = 1 (see Figure 10)	+VBD 5 V			7	ns
		+VBD 3.3 V			8	
t_{d19}	Delay time, point A indicating clear for bus 3-state release to BUSY falling edge (see Figure 8)	+VBD 5 V			40	
		+VBD 3.3 V			40.5	
T_{clk}	CLK frequency (serial data rate)		190	200	210	MHz

6.2 Sample and Convert

The sampling and conversion process is controlled by the $\overline{\text{CSTART}}$ (LVDS) or $\overline{\text{CONVST}}$ (CMOS) signal. Both signals are functionally identical. The following diagrams show control with $\overline{\text{CONVST}}$. The rising edge of $\overline{\text{CONVST}}$ (or $\overline{\text{CSTART}}$) starts the sample phase, if the conversion has completed and the ADC is in the wait state. Figure 5 shows the case when the ADC is in the conversion phase at the rising edge of $\overline{\text{CONVST}}$. In this case, the sample phase starts immediately at the end of the conversion phase and there is no wait state.

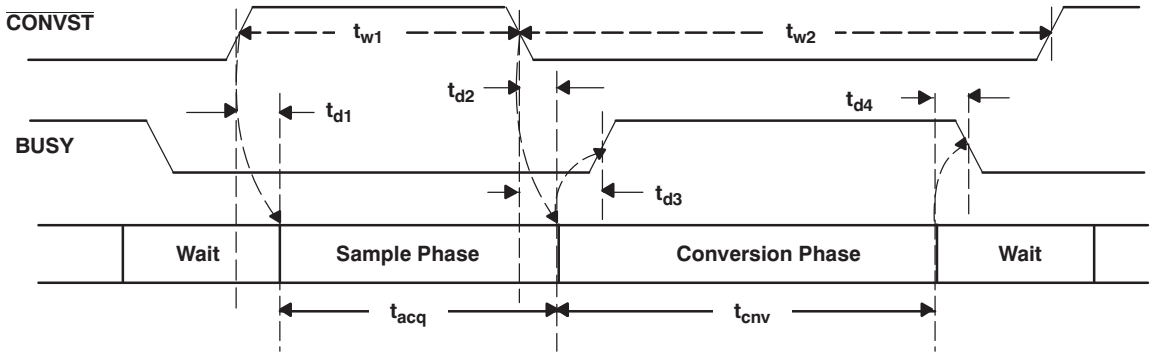


Figure 4. Sample and Convert With Wait (Less Than 2 MSPS Throughput)

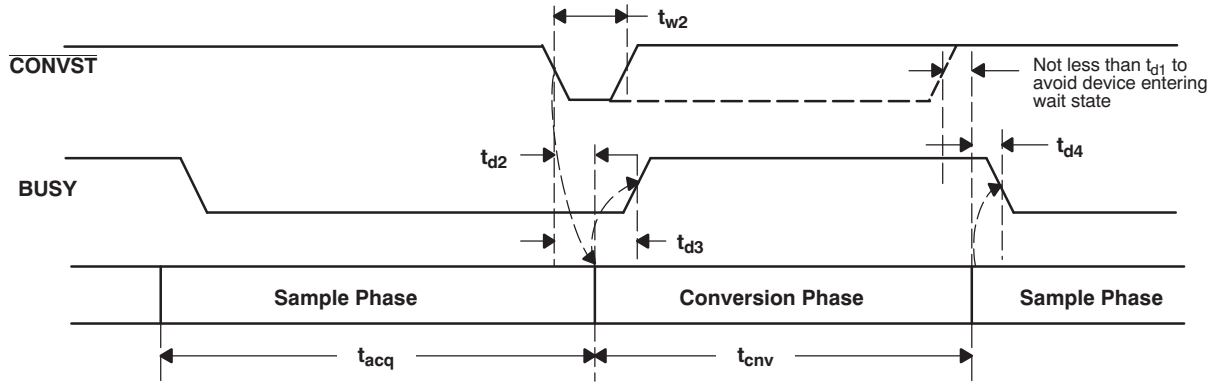


Figure 5. Sample and Convert With No Wait or Back to Back (2 MSPS Throughput)

The ADC ends the sample phase and enters the conversion phase on the falling edge of $\overline{\text{CONVST}}$ ($\overline{\text{CSTART}}$). A high level on the BUSY output indicates an ongoing conversion. The ADC conversion time is fixed. The falling edge of $\overline{\text{CONVST}}$ ($\overline{\text{CSTART}}$) during the conversion phase aborts the ongoing conversion. A data read after a conversion abort fetches invalid data. Valid data is only available after a sample phase and a conversion phase have completed. The timing diagram for control with $\overline{\text{CSTART}}$ is similar to Figure 4 and Figure 5. Table 1 shows the equivalent timing for control with $\overline{\text{CONVST}}$ and $\overline{\text{CSTART}}$).

Table 1. $\overline{\text{CONVST}}$ and $\overline{\text{CSTART}}$ Timing Control

TIMING FOR CONTROL WITH $\overline{\text{CONVST}}$	TIMING FOR CONTROL WITH $\overline{\text{CSTART}}$
tw1	tw3
tw2	tw4
t1	t5
t2	t6
t3	t7

6.3 Data-Read Operation

The ADS8413 supports a 200-MHz serial LVDS interface for a data-read operation. The three-signal LVDS interface (SDO, CLK_O, and SYNC_O) is well-suited for high-speed data transfers. An application with a single ADC or multiple ADCs can be implemented with a daisy-chain or cascade configuration. The following sections discuss data-read timing when a single ADC is used.

6.4 Data Read for a Single ADC

For a single ADC, there are two possible read cycle starts: a data-read cycle start during a wait or sample phase, or a data-read cycle start at the end of a conversion phase. (See Table 1 for ADC configuration.) Read cycle end conditions can change depending on MODE C/$\overline{\text{D}}$ selection. Figure 6 explains the data-read cycle. The details of a read frame start with the two previous listed conditions and a read cycle end with MODE C/$\overline{\text{D}}$ selection are illustrated in Figure 7, Figure 8, and Figure 9, respectively.

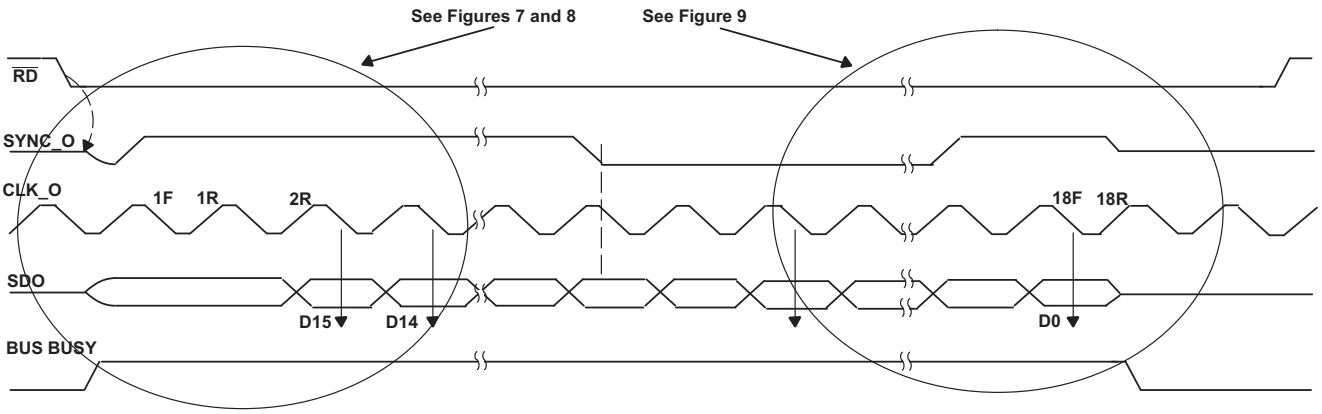


Figure 6. Data Read With $\overline{CS}$ Low and BYTE = 0

As shown in Figure 6, a new data-read cycle is initiated with the falling edge of $\overline{RD}$, if $\overline{CS}$ is low and the ADC is in a wait or sample phase. The ADC releases the LVDS o/p (SYNC_O, SDO) from a 3-state mode and sets BUS_BUSY high at the start of the read cycle. The SYNC_O cycle is 16 clocks wide (rising edge to rising edge) if the BYTE input is held low and can be used to synchronize a data frame. The clock count begins with the first CLK_O falling edge after a SYNC_O rising edge. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of the clock. The next rising edge of SYNC_O coincides with the 16th rising edge of the clock. D0 is latched out on the 17th rising edge of the clock. The receiver can latch the de-serialized 16-bit word on the 18th rising edge (18R, or the second rising edge after a SYNC_O rising edge).

$\overline{CS}$ is high during a data-read, 3-state mode SYNC_O and SDO. These signals remain in the 3-state mode until the start of the next data-read cycle.

6.5 Data-Read Cycle Start During Wait or Sample Phase

As shown in Figure 7, the falling edge of $\overline{RD}$, with $\overline{CS}$ low and the ADC is in a wait or sample phase, triggers the start of a read cycle. The cycle starts when BUS_BUSY goes high and SYNC_O, SDO are released from the 3-state mode. SYNC_O is low at the start and rises to a high level td13 ns after the falling edge of $\overline{RD}$. As shown in Figure 7, the MSB is shifted on the second rising edge of the clock (2R). Other details about the data-read cycle are discussed in the previous section (see Figure 6).

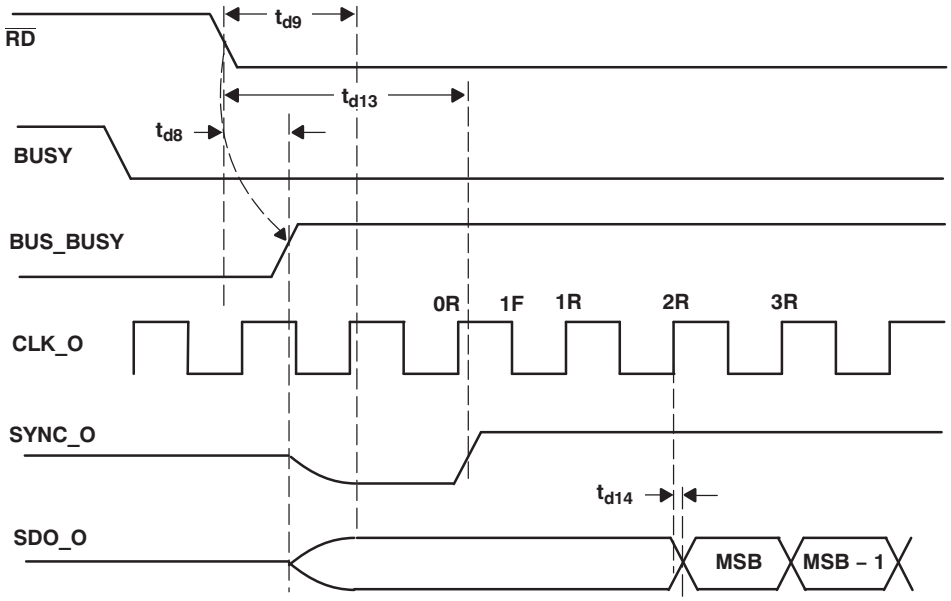


Figure 7. Start of Data-Read Cycle with $\overline{RD}$ and $\overline{CS}$ Low and ADC in Wait or Sample Phase

6.6 Data-Read-Cycle Start at End of Conversion Phase (Read Without Latency, Back-to-Back)

This mode is optimized for a data read immediately after the end of a conversion phase and ensures that the data read is complete before the sample end while running at 2 MSPS. Point A in Figure 8 indicates *pre_conversion_end*; it occurs td19 ns before the falling edge of BUSY (BUSY = 1 indicates that the ADC is busy doing analog to digital conversion) or [(td2 + tcnv + td4) – td19] ns after the falling edge of $\overline{CONVST}$. A read cycle is initiated at point A if $\overline{RD}$ is issued before point A while $\overline{CS}$ is low. Alternately, $\overline{RD}$ and $\overline{CS}$ can be held low. At the start of the read cycle, BUS_BUSY rises to a high level and the LVDS outputs are released from the 3-state mode. The rising edge of SYNC_O, occurs td12 ns after the conversion end. As shown in Figure 8, the MSB is shifted on the second rising edge of the clock (2R). Other details about the data-read cycle are discussed in the previous section (see Figure 6).

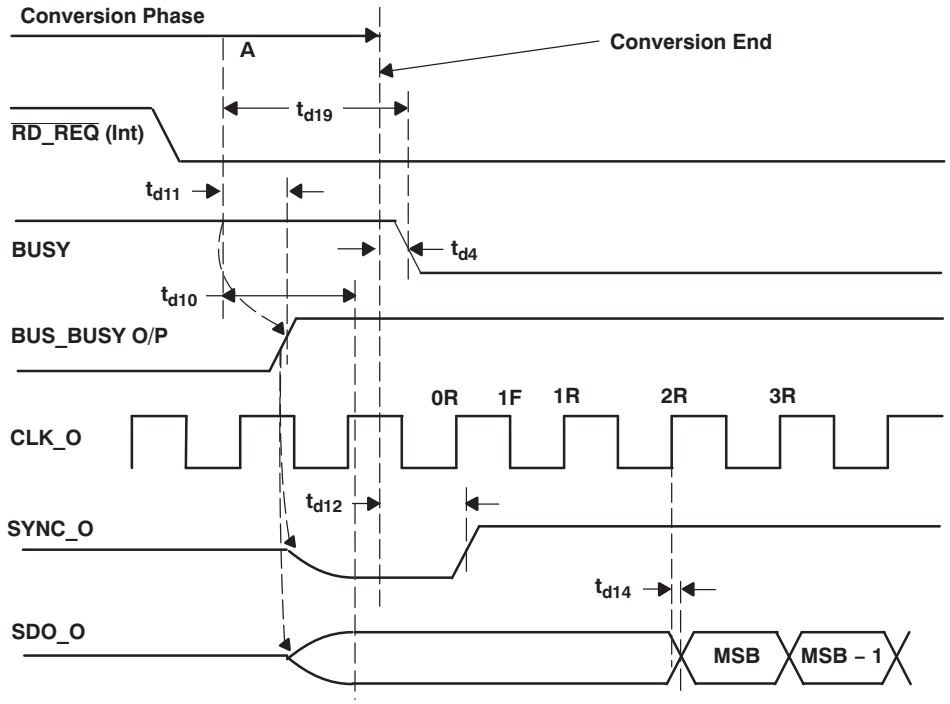


Figure 8. Start of Data-Read Cycle with End of Conversion

6.7 Data-Read Cycle End (With MODE C/$\overline{D}$ = 1)

A data-read cycle ends after all 16 bits have been serially latched out. Figure 9 shows the timing of the falling edge of BUS_BUSY and the rising edge of SYNCO with respect to SDO. SYNC_O rises on the 16th rising edge of CLK_O. As shown in Figure 7 and Figure 8, the MSB is shifted out on the second rising edge of CLK_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK_O.

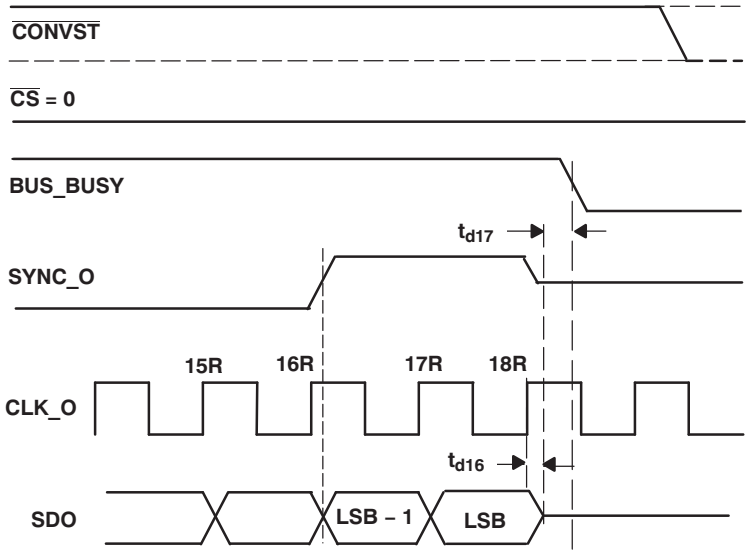


Figure 9. Data-Read-Cycle End with MODE C/$\overline{D}$= 1

The next two rising edges of CLK_O are shown as 17R and 18R in Figure 8. On 17R, the LSB is latched out and on 18R the SDO and SYNC_O go into a 3-state mode. In cascade mode (with MODE C/$\overline{D}$ = 1), unlike daisy-chain mode, BUS_BUSY falling edge occurs after LVDS outputs are in 3-state mode. One can use BUS_BUSY falling edge to allow the LVDS bus usage by any other ADC.

6.8 Timing Diagrams for Cascade Operation

The conversion rate for n ADCs in cascade must be selected such that:

- 1/conversion speed > first ADC read-cycle duration + (n – 1) next ADC read cycle duration
- First ADC read-cycle duration = read start-up delay_1 + data frame duration + (t_{d16} + t_{d17})
- Next ADC read-cycle duration = read start-up delay_n + data frame duration + (t_{d16} + t_{d17})
- Read start-up delay_1 = 10 ns + (t_{d19}– t_{d4} + t_{d12}) + 2/f_{clk}
- Read start-up delay_n = (t_{d13} + 2/f_{clk})
- Data frame duration = 16/f_{clk}

Note that it is unnecessary that all ADCs in the chain sample the data simultaneously. But, all the ADCs must operate with the same exact conversion speed.

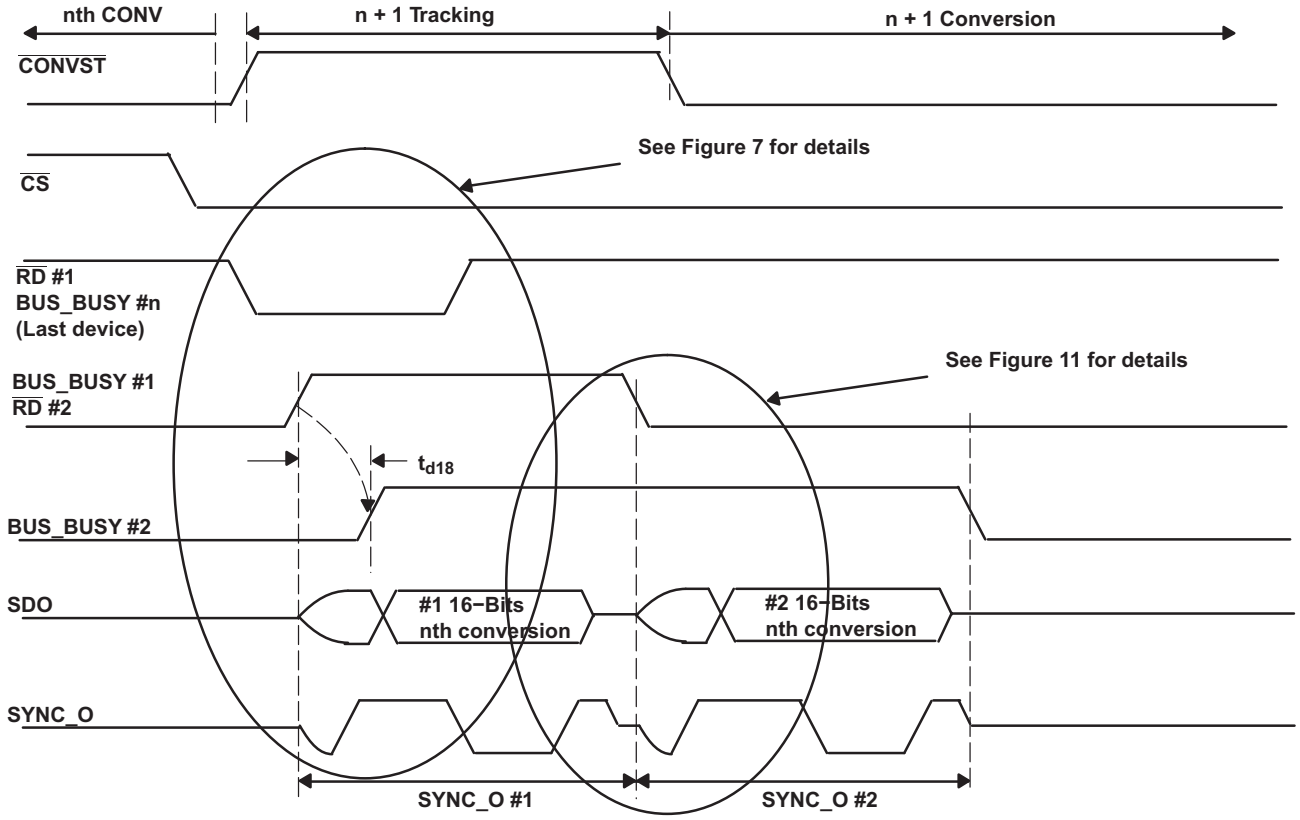


Figure 10. Data-Read Operation for ADCs in Cascade Mode

6.9 Data-Read Operation

On power up, BUS_BUSY for all the ADCs is low. The ADCs receive $\overline{CONVST}$ or $\overline{CSTART}$ to sample and start the conversion. The first ADC starts the data-read cycle at the end of its conversion. BUS_BUSY of ADC 1 (connected to $\overline{RD}$ of ADC 2) goes high on the read-cycle start, indicating that it wants to occupy the bus. BUS_BUSY of ADC 2 goes high on the rising edge of $\overline{RD}$. This propagates until the last ADC.

BUS_BUSY of ADC 1 goes low after it outputs its data; at this time, SDO and SYNC_O of ADC 1 go into a 3-state mode. The falling edge of BUS_BUSY ($\overline{RD}$ of the next ADC) indicates to the next ADC that it is its turn to output the data. The next ADC outputs the data from the last completed conversion. BUS_BUSY of

the last ADC goes low and its SYNC_O and SDO go to a 3-state mode after it outputs its data. BUS_BUSY of the last ADC is fed back to the $\overline{RD}$ of the first ADC ($\overline{RD}$ can also be tied to 0 for ADC 1). This ensures that $\overline{RD}$ of ADC 1 is low before its conversion is over. The data-read sequence continues with only one external signal, $\overline{CONVST}$ or $\overline{CSTART}$, when $\overline{CS}$= 0. For any ADC, $\overline{CS}$ high during the data-read cycle puts SYNC_O and SDO of the ADC in a 3-state mode and halts the data-read sequence. To reset this condition, it is necessary to assert $\overline{CS}$ high for all of the ADCs. The new read sequence starts only after $\overline{CS}$ for all of the ADCs is low before point A as shown in Figure 8. The high pulse on $\overline{CS}$ must be at least 20-ns wide. It is better to connect $\overline{CS}$ for all the ADCs together to avoid undesired halting of the data-read sequence.

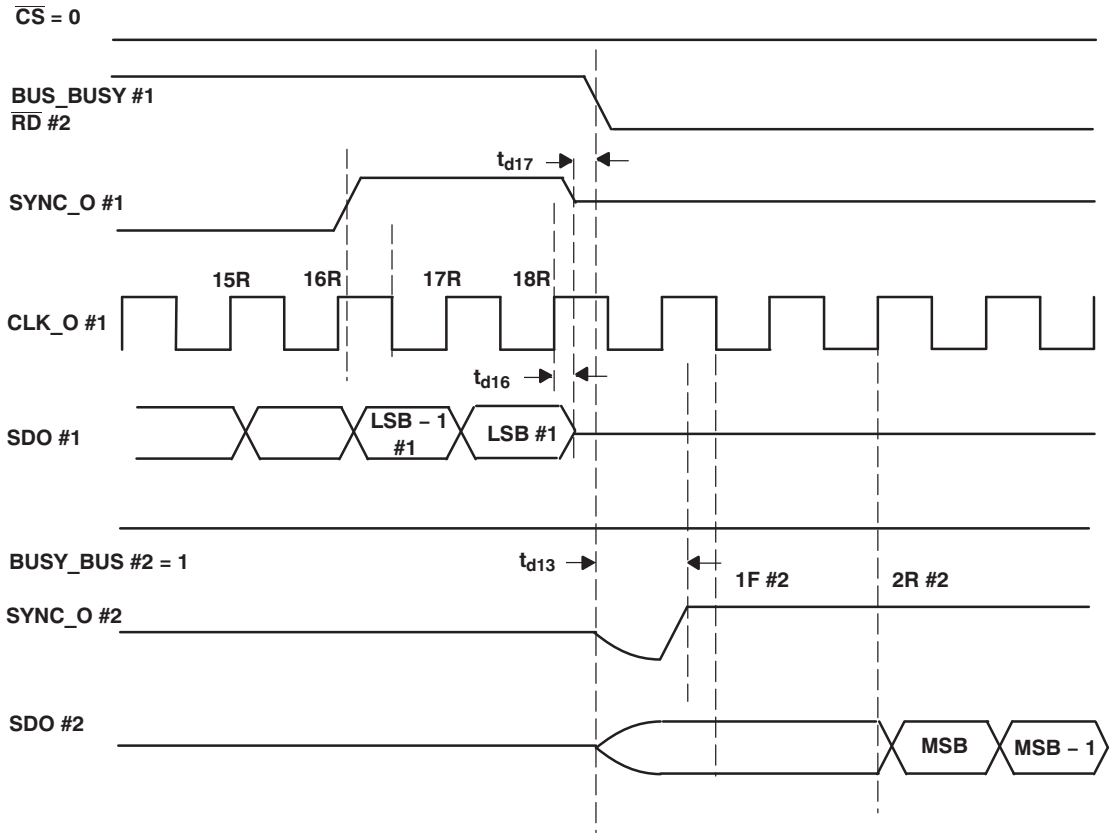


Figure 11. ADC *n* Read-Cycle End and ADC *n+1* Read-Cycle Start

Unlike the daisy-chain mode, the data frames of all the ADCs in cascade are not seamless and there is a loss of time between one ADC 3-state mode to other ADC data valid due to wakeup time from the 3-state mode and a two-clock-phase shift between SYNC and data (see Figure 11 for details). As a result, the number of data frames per second in this mode is less than in daisy-chain mode. Also, a maximum of four ADCs can be cascaded on the same bus. But, I/O power per ADC is considerably lower in cascade as compared to daisy chain as each ADC LVDS o/p goes to a 3-state mode after its data transfer. The de-serializer at the output of the last ADC can shift the data on every clock falling edge, and it can latch the parallel 16-bit word on the second CLK_O rising edge (shown as 18R) after every SYNC_O rising edge.

7 Board Design Aspects

7.1 Placement

Consider an application where four ADCs are operated in cascade mode. There are two ways to do the layout. The chain can be in a straight-line fashion (as in Figure 12) or in two rows (as in Figure 13).

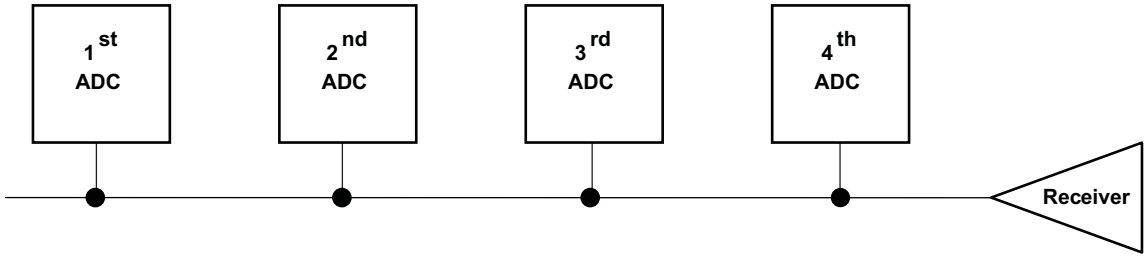


Figure 12. Four ADCs Placed in Straight-Line Fashion

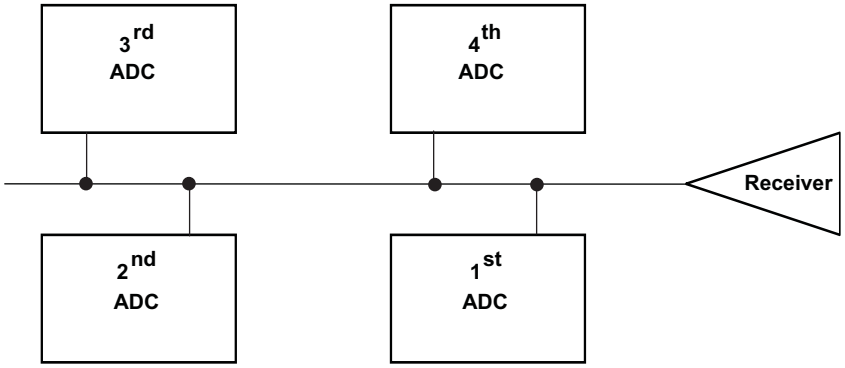
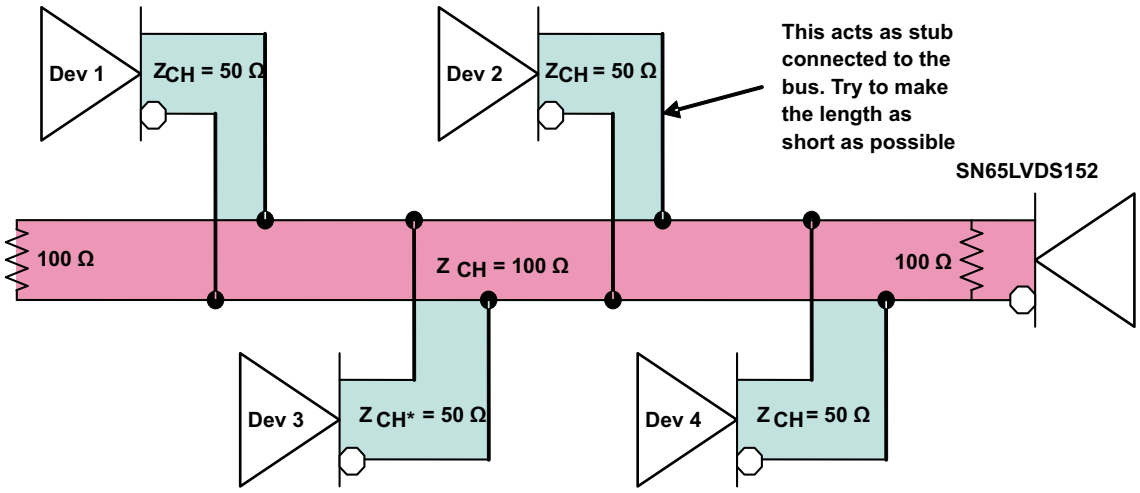


Figure 13. Four ADCs Placed in Two Rows

Either layout can be chosen depending on the area and shape of the printed-circuit board.

7.2 Signal Integrity

The ADC offers high-speed LVDS CLK_O, SDO, and SYNC_O signals which have a typical rise time of only 700 ps. According to the LVDS standard, the receiver termination needs to be 100 Ω (shunt resistance between +ve and –ve terminal of each LVDS signals) to have proper voltage swing (see Figure 14). To avoid reflection, the differential characteristic impedance needs to match with the 100-Ω termination. The resistor is placed at the receiver end. This termination technique is followed in point-to-point connection. However, in cascade mode, multiple transmitters connect to a common bus with only one receiver. To avoid reflection, two 100-Ω termination resistors are put at both ends of the bus. The differential characteristic impedance of the bus is matched with termination resistors and is 100 Ω. The trace connected from each ADC to the bus should have a differential characteristic impedance of 50 Ω in order to drive each end of the bus. This ensures that there is no reflection from either side of the bus. The parallel combination of two 100-Ω resistors makes the effective load to be 50 Ω. So, signal swing becomes half. To increase the signal swing back to its original value, M2 is made logic 1 so that the LVDS current doubles.



*Z_{CH} is the differential characteristic impedance between positive and negative terminal of LVDS signal

Figure 14. Terminating Four ADCs in Cascade

7.3 Proper Routing of Clock, Data, and Frame Sync

The reference board is designed as is shown in Figure 13. Figure 15 shows a block diagram of the clock layout. In this board, the clock can be either external or internal. An external 25-MHz clock is generated from a pattern generator. This clock is multiplied by a clock multiplier (Texas Instruments CDCF5801). This IC multiplies the clock to 200 MHz, and the output clock is an LVDS clock. In internal clock mode, ADC 3 generates the clock. The external or internal clock is chosen by installing appropriate resistors on the board. The internal clock is selected by installing R357 and R358 as 0 Ω and not installing R353 and R354. The external clock is selected by installing R353 and R354 as 0 Ω and not installing R357 and R358 (see the schematics in the appendix). This clock is used as a master clock for all the ADCs and is distributed by a clock distributor (Texas Instruments SN65LVDS104). The skew, between the output clocks from the clock distributor, should be lower than 100 ps. To meet setup and hold time, the length of the clock traces should be matched (within the tolerance of 100 mils) as:

(AA') + (A''R) = (CC') + (C''R) = (DD') + (D''R)

Also for each ADC, length of CLK_O, SDO, and SYNC_O traces should be matched within the tolerance of 100 mils. See the layout diagram in the appendix for actual layout.

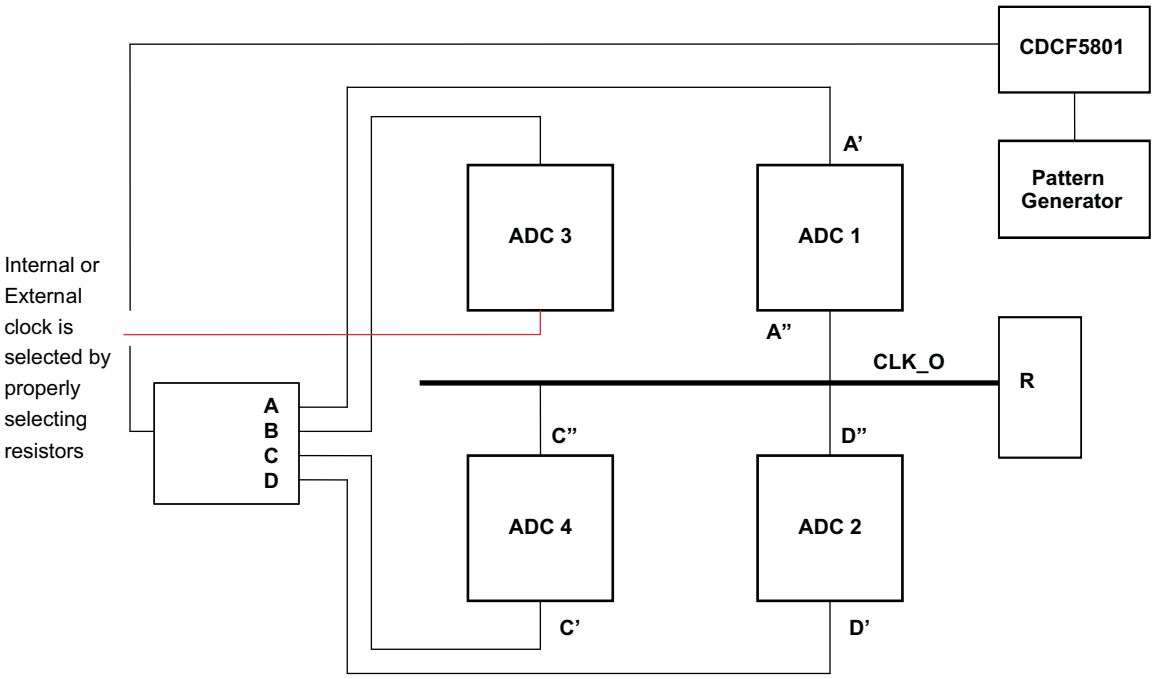


Figure 15. Block Diagram of Clock-In and Clock-Out Routing

7.4 Proper Layout for Analog and Digital

Because the ADC offers high-speed digital interface, analog and digital layout should not be mixed up. Analog placement and routing should be separated as far as possible from the digital placement and routing. See the reference schematics and layout at the end of this application report.

7.5 System Block Diagram

Figure 16 and Figure 17 show how four ADCs in cascade are tested. Figure 16 shows how first and second ADCs are connected when external clock mode is used. Connect ADC 3 and ADC 4 the same as ADC 2. A pattern generator is used to generate necessary control signals and clock. A 25-MHz clock is generated from the pattern generator and is multiplied by a clock multiplier (CDCF5801) to get a 200-MHz LVDS clock. CMOS to LVDS drivers (SN75LVDS389) are used to convert from CMOS/ TTL to LVDS.

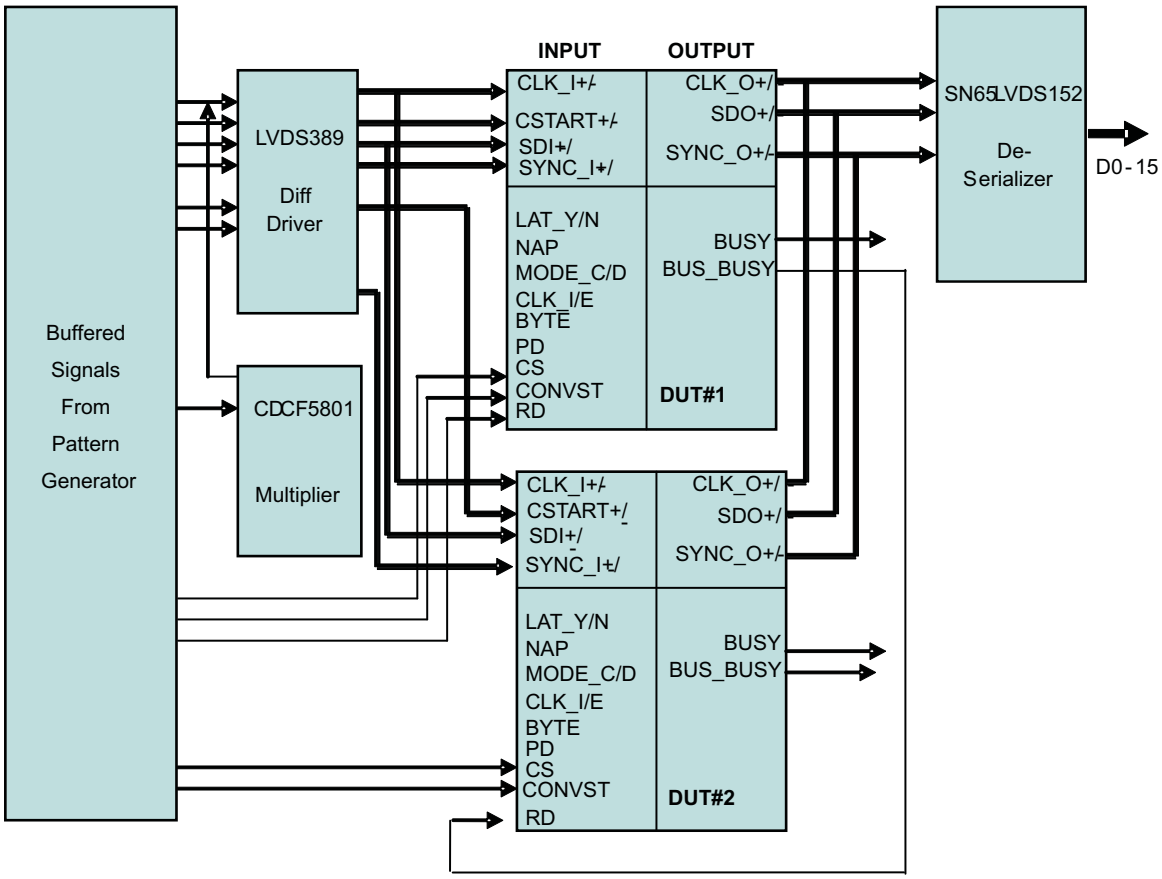


Figure 16. First and Second ADC in Cascade Mode

Figure 17 shows how first and third ADCs are connected when an internal clock is used. In this case, ADC 3 is used to generate the internal clock. LVDS serial data are converted to parallel by two cascaded SN65LVDS152.

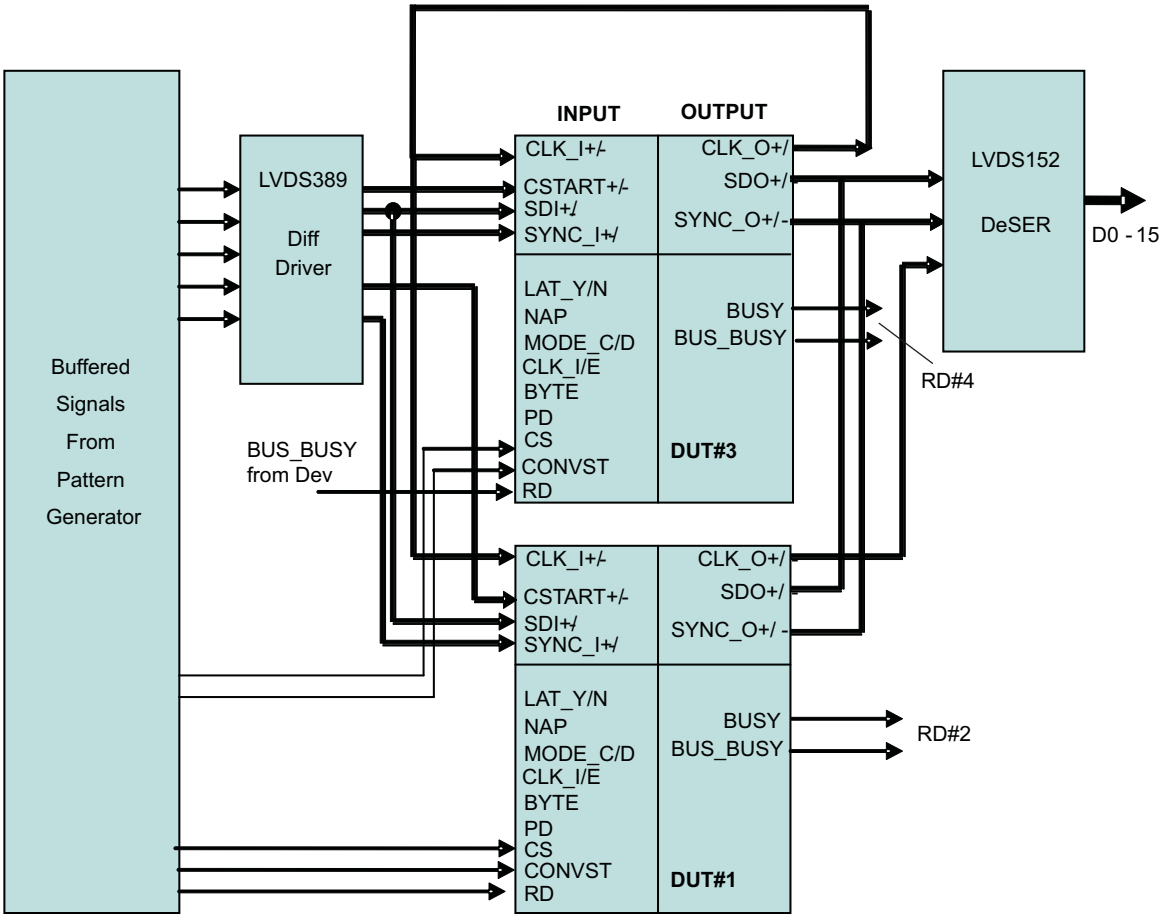


Figure 17. Third and First ADC in Cascade

7.6 De-Serialization

The interface is compatible with TI de-serializer SN65LVDS152. SN65LVDS152 is a 10-bit de-serializer. Two such de-serializers are cascaded to get 16-bit parallel data output. Figure 18 shows the connection of the de-serializer with CLK_O, SYNC_O, and SDO bus with the necessary terminations.

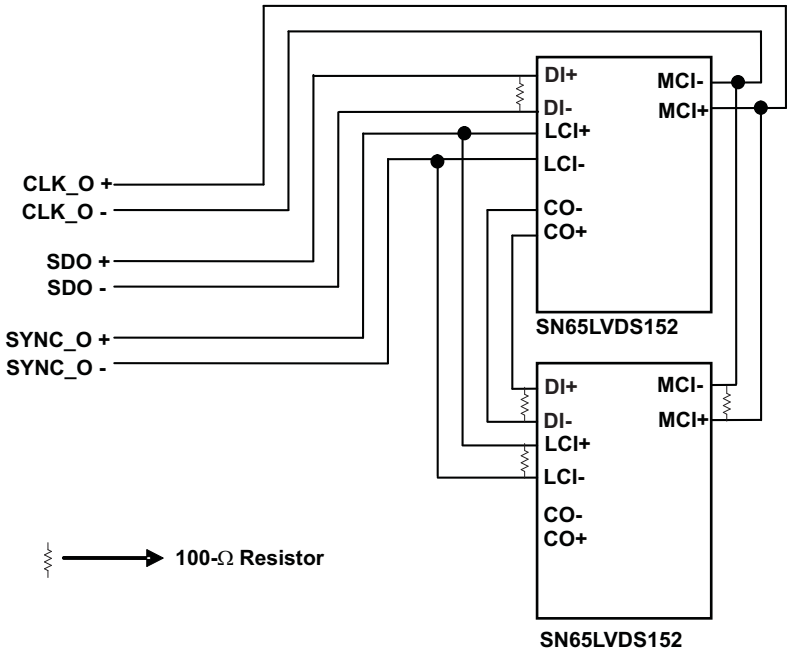


Figure 18. CLK_O, SYNC_O and SDO Bus and De-Serializers

7.7 Limitation on Number of ADCs in Cascade Mode

The cascade mode is designed for a maximum of three ADCs at a throughput of 2 MSPS and at an interface speed of 200 Mbps. However, a maximum of four ADCs can be used at 1.9 MSPS. See the timing section for the relation between sampling rate and the number of ADCs in the cascade mode. When more than four ADCs are used, the output load for CLK_O, SYNC_O, and SDO increases, which causes timing violation.

8 Results

8.1 Linearity Across ADCs

Table 2 shows DNL and INL of ADS8413 versus the ADC number in cascade mode. The data has been captured for four ADCs in the chain at 200-MHz external clock and 1.9 MSPS throughput

Table 2. Linearity of Four ADCs in Cascade Mode

ADC NO.	DNL		INL	
	MAX	MIN	MAX	MIN
1	0.8	–0.6	1.2	–1.3
2	0.7	–0.6	1.2	–1.3
3	0.9	–0.6	1.0	–1.1
4	0.6	–0.5	1.0	–1.4

8.2 SNR and THD Across ADCs

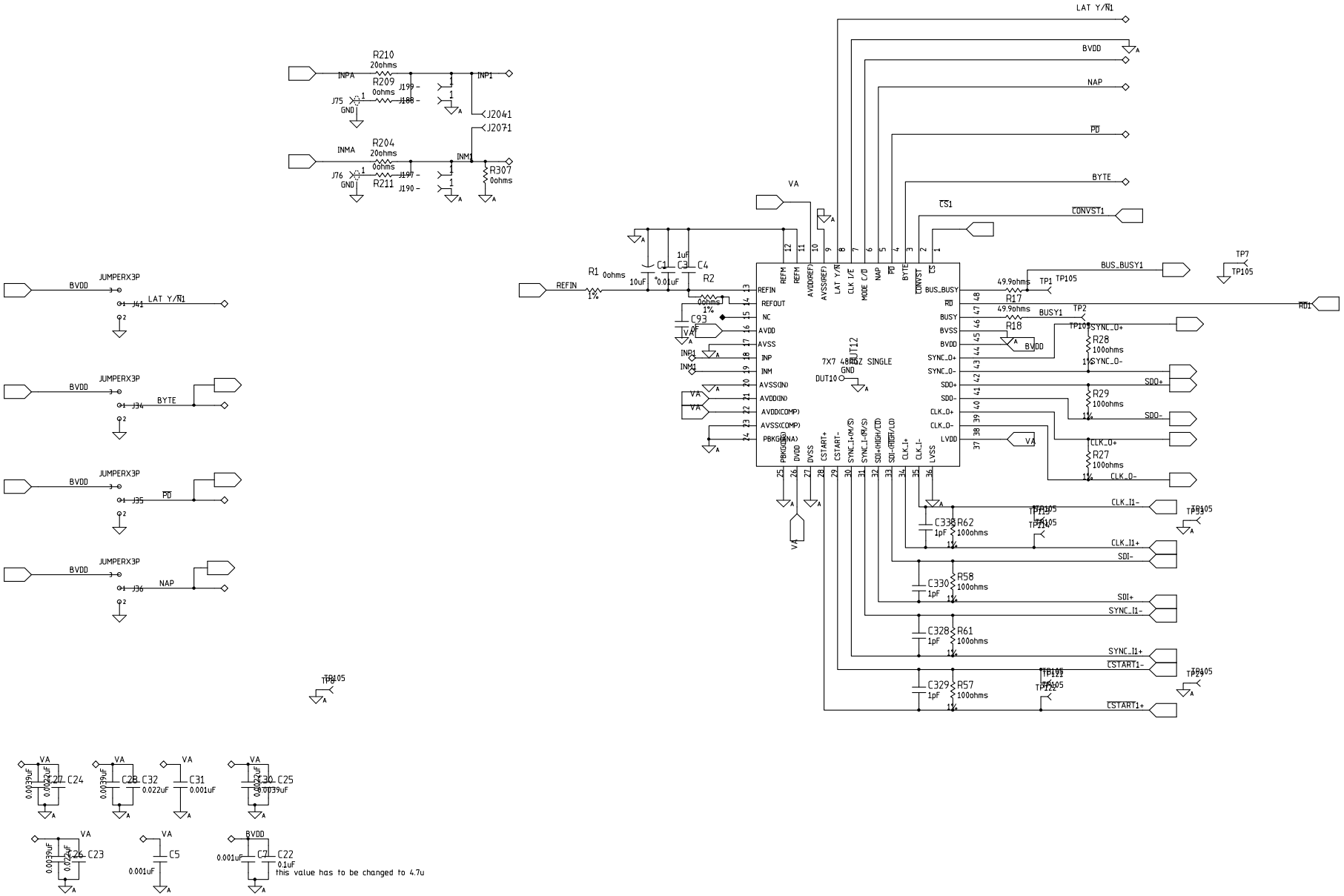
AC performance of ADS8413 is checked in cascade mode. No degradation is seen with cascading.

9 Conclusion

Cascade mode offers the ability to use each ADC in the system independently. One or more idle ADCs can be powered down or driven to low-power mode (NAP = 1) to save overall system power. Malfunctioning of one ADC in the system does not interfere with the functionality of the other ADCs. This system can run with its own internal clock (clock is generated from one of the ADCs) or an external clock. The full frame (conversion and acquisition) of the sampling time of the ADC is available for data transfer. This allows using four ADCs with a throughput of 1.9 MSPS. No performance degradation was seen with four ADCs in a cascade configuration.

Appendix A Schematics

The relevant schematics are appended on the following pages.



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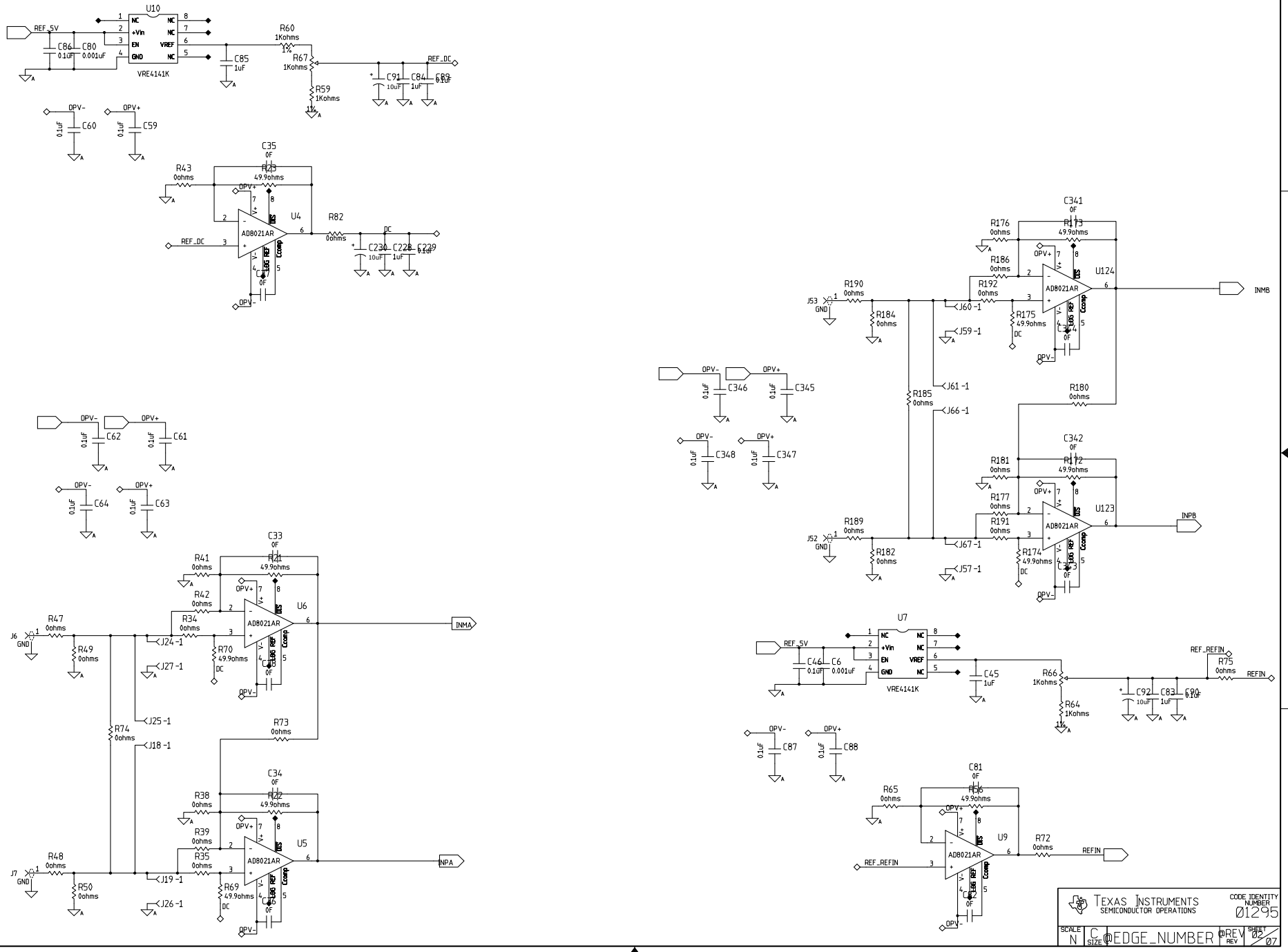
			SHEET Ø1 Ø7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REF_5V
C86 0.1uF
C80 0.001uF
VRE4141K
C85 1uF
R60 1Kohms 1%
R67 1Kohms
R59 1Kohms 1%
REF_DC
C91 10uF
C84 1uF
C89 0.1uF
OPV-
C60 0.1uF
OPV+
C59 0.1uF
C35 0F
R43 0ohms
R23 49.9ohms
U4
AD8021AR
R82 0ohms
C230 10uF
C228 1uF
C229 0.1uF
C62 0.1uF
C61 0.1uF
C64 0.1uF
C63 0.1uF
C33 0F
R41 0ohms
R21 49.9ohms
R42 0ohms
R34 0ohms
U6
R47 0ohms
J6
GND
R49 0ohms
J24 -1
J27 -1
R70 49.9ohms DC
INMA
R74 0ohms
J25 -1
J18 -1
R73 0ohms
C34 0F
R38 0ohms
R22 49.9ohms
R39 0ohms
R35 0ohms
U5
R48 0ohms
J7
R50 0ohms
J19 -1
J26 -1
R69 49.9ohms DC
INPA
C341 0F
R176 0ohms
R173 49.9ohms
R186 0ohms
R192 0ohms
U124
R190 0ohms
J53
R184 0ohms
J60 -1
J59 -1
R175 49.9ohms DC
INMB
C346 0.1uF
C345 0.1uF
C348 0.1uF
C347 0.1uF
R185 0ohms
J61 -1
J66 -1
R180 0ohms
C342 0F
R181 0ohms
R172 49.9ohms
R177 0ohms
R191 0ohms
U123
R189 0ohms
J52
R182 0ohms
J67 -1
J57 -1
R174 49.9ohms DC
INPB
U7
REF_5V
C46 0.1uF
C6 0.001uF
VRE4141K
C45 1uF
R66 1Kohms 1%
R64 1Kohms
C92 10uF
C83 1uF
C90 0.1uF
REF_REFIN
R75 0ohms
REFIN
C87 0.1uF
C88 0.1uF
C81 0F
R65 0ohms
R56 49.9ohms
U9
R72 0ohms
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REFIN
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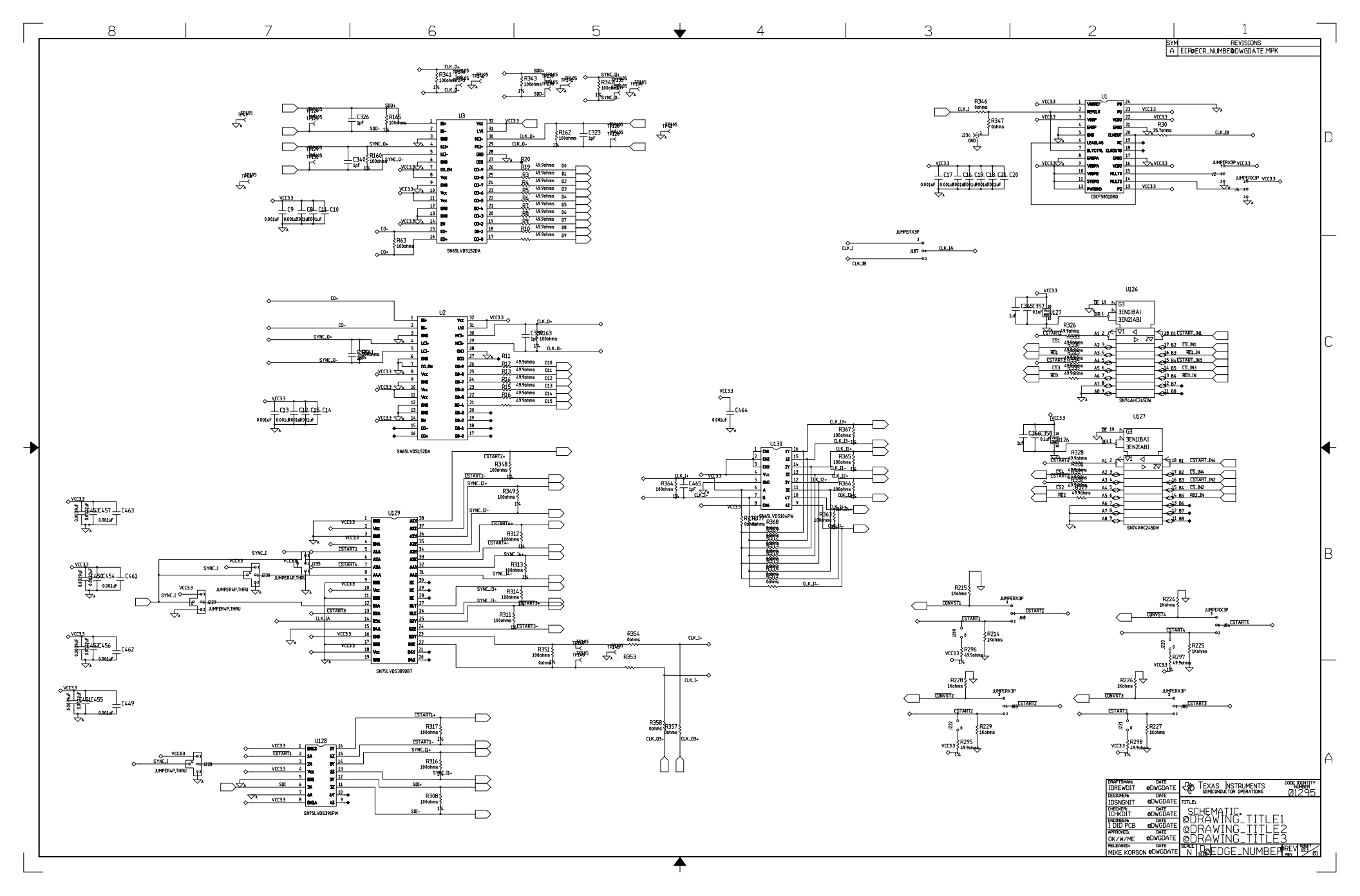
@EDGE_NUMBER
@REV REV
SHEET 02 07


REVISIONS
SYM
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U2
SN65LVDS152DA
U1
CDCF5801DBQ
U126
SN74AHC245DW
U127
SN74AHC245DW
U130
SN65LVDS104PW
U129
SN75LVDS3890BT
U128
SN75LVDS391PW
JUMPER4P,THRU
JUMPERX3P
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SEMICONDUCTOR OPERATIONS
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01295
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DESIGNER: IDSNGNIT DATE @DWGDATE
CHECKER: ICHKDIT DATE @DWGDATE
ENGINEER: I DID PCB DATE @DWGDATE
APPROVED: OK/W/ME DATE @DWGDATE
RELEASED: MIKE KORSON @DWGDATE DATE
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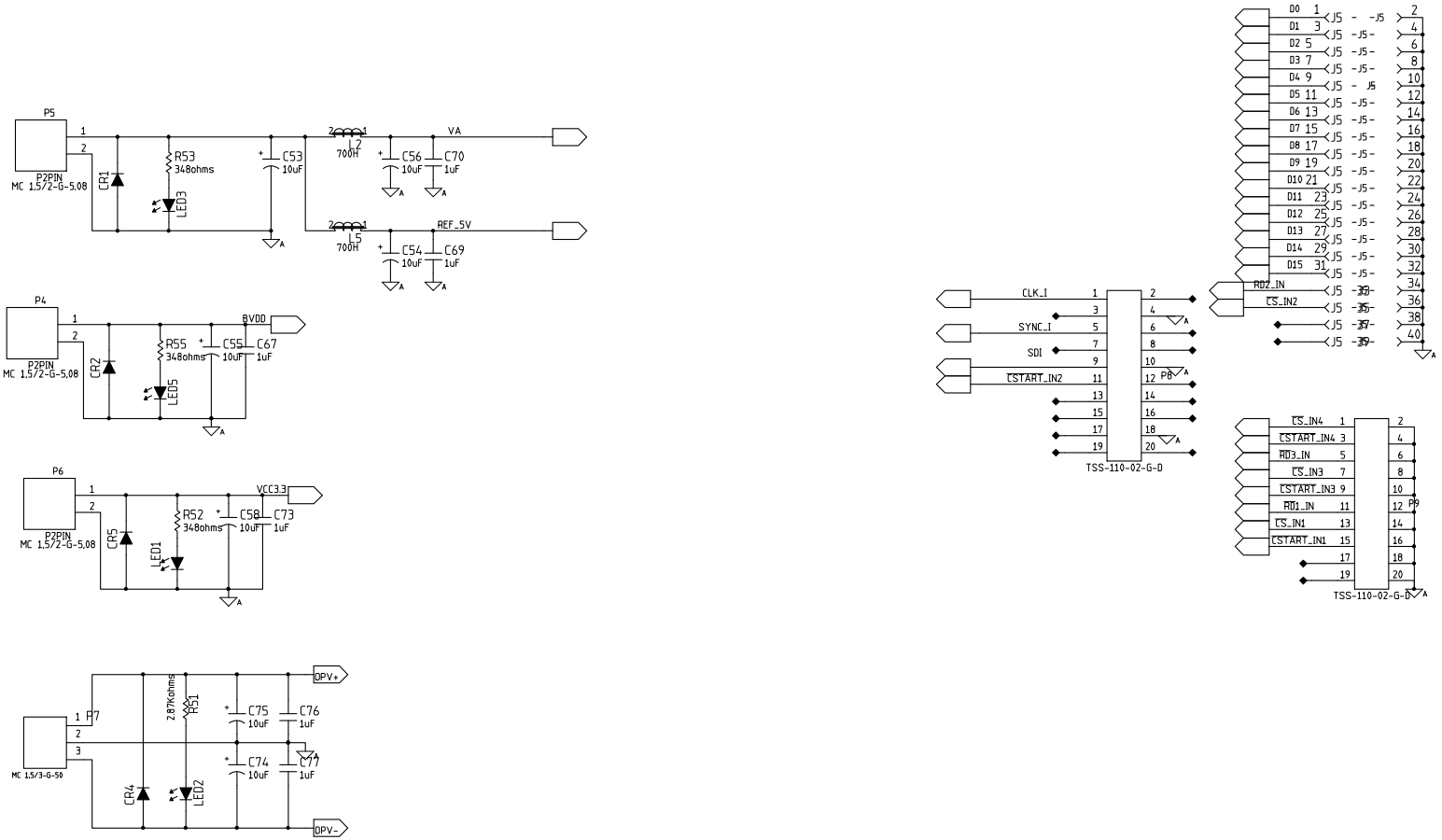
SHT: 01



TEXAS INSTRUMENTS
SEMICONDUCTOR OPERATIONS

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Ø1295

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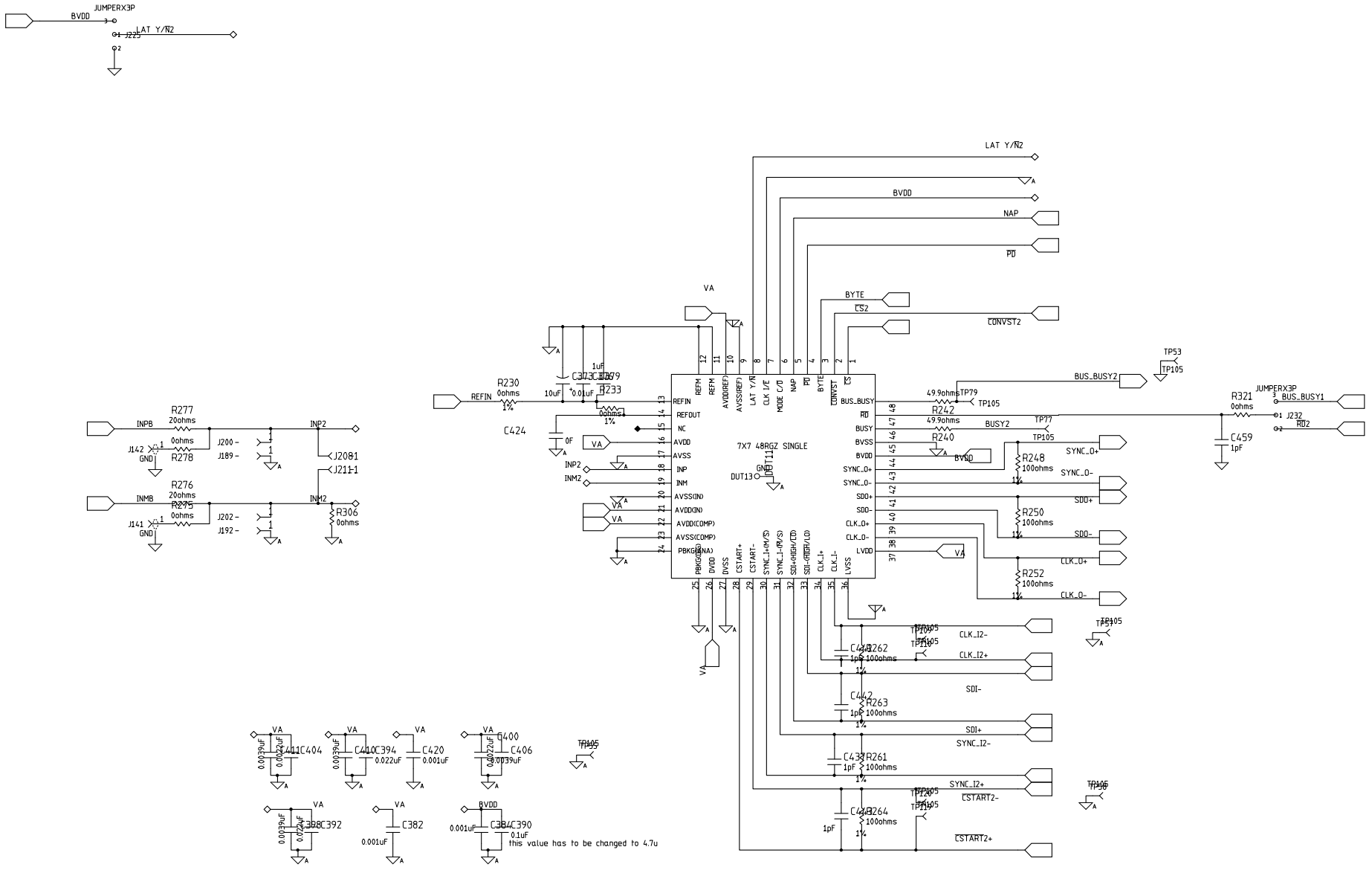

TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS			CODE IDENTITY NUMBER 01295
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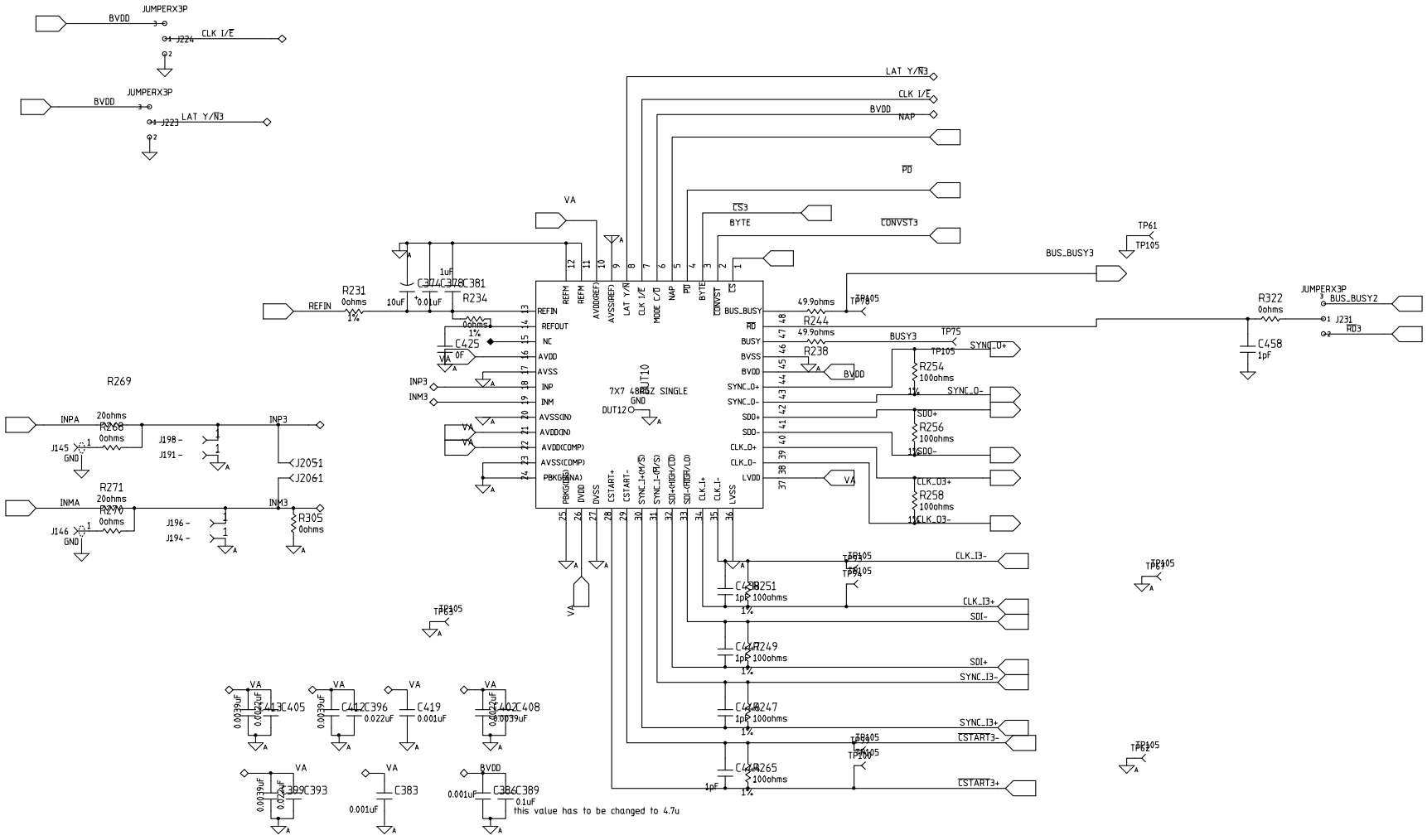

Texas Instruments Semiconductor Operations		CODE IDENTITY NUMBER	Ø1295
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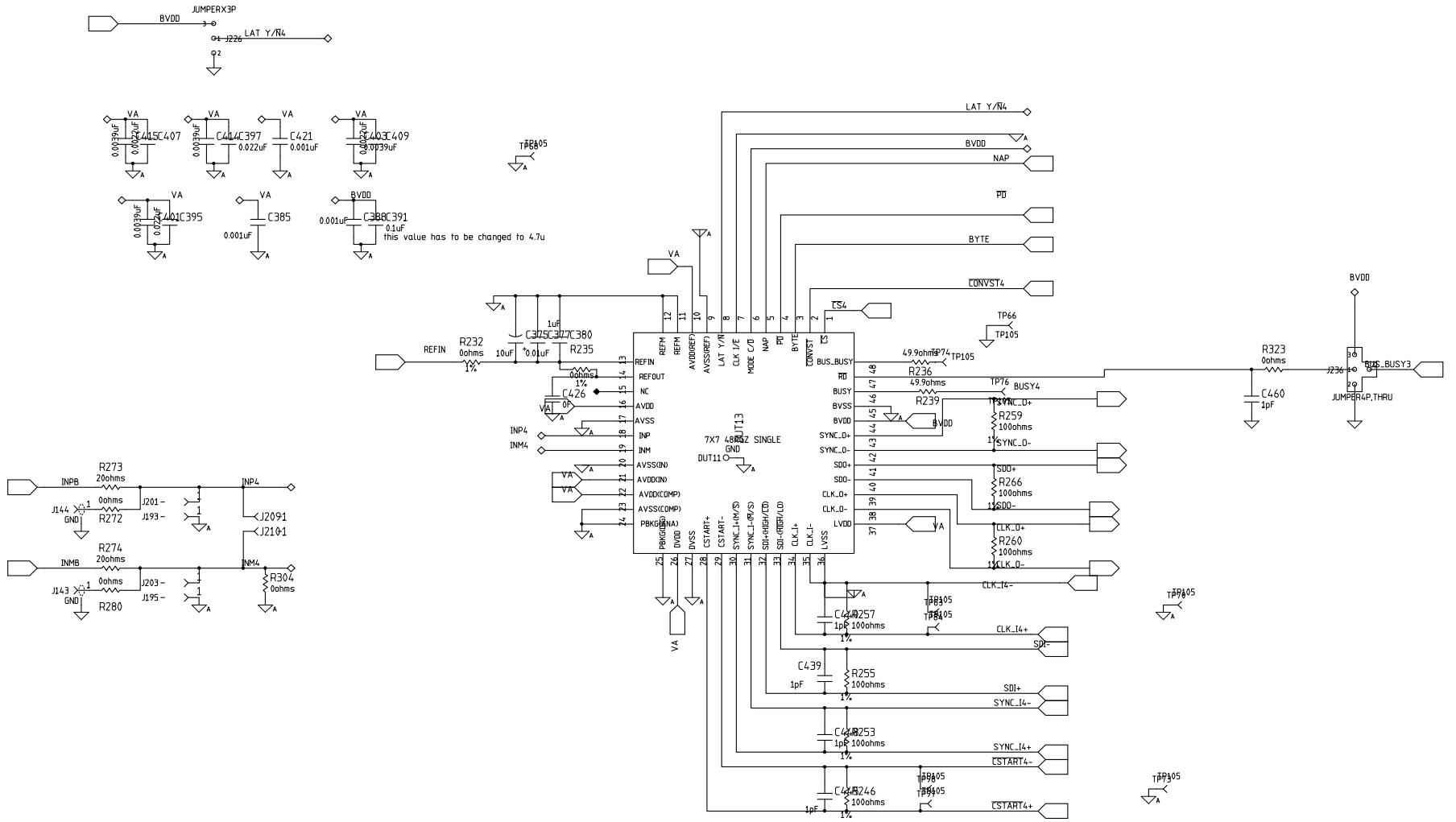
SHEET Ø6 Ø7			



TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS			CODE IDENTITY NUMBER Ø1295
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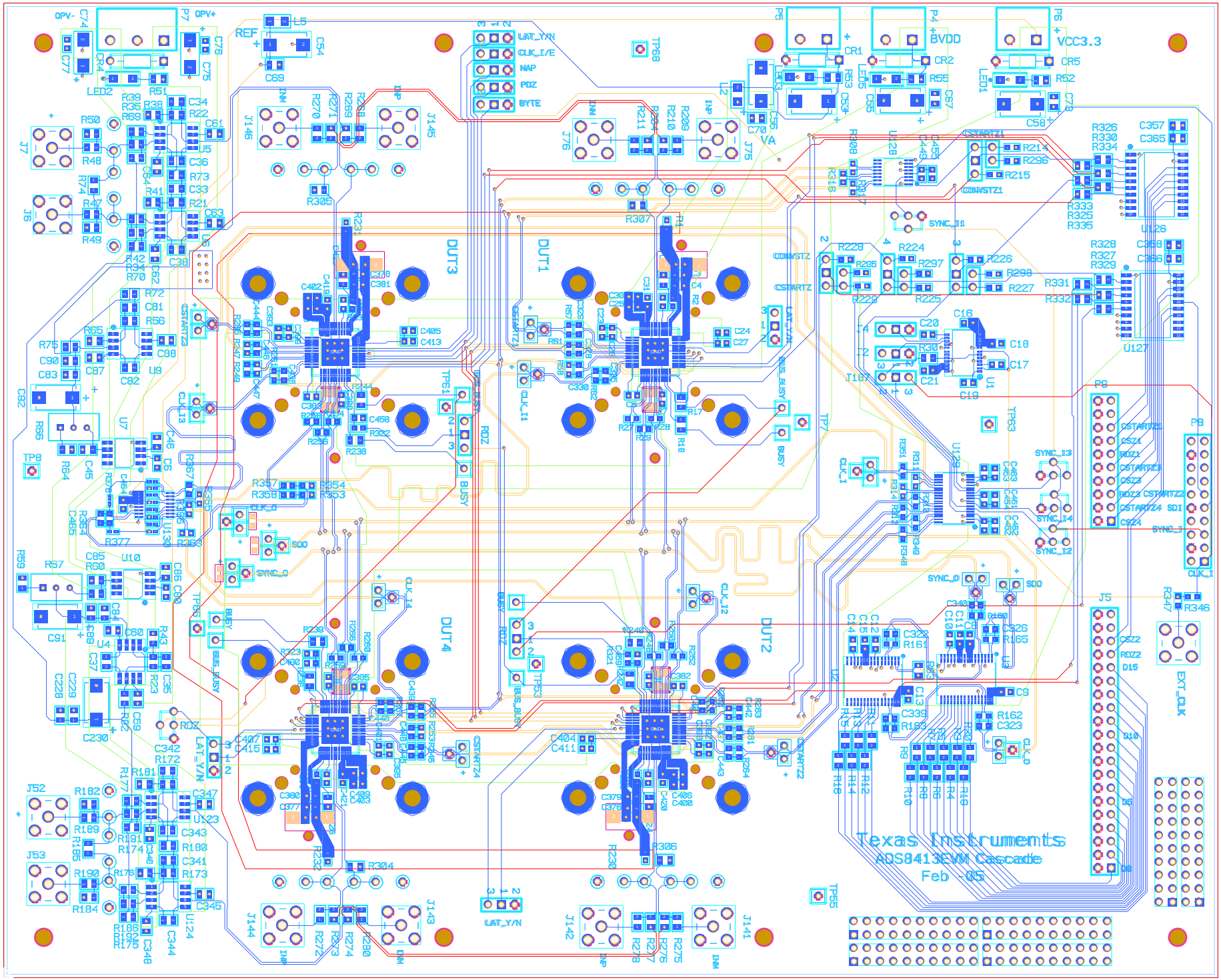
			SHEET Ø7/Ø7

Appendix B Layout

The ADS8413EVM Cascade layout is appended on the following page.


DUT3
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DUT4
DUT2
REF
BVDD
VCC3.3
VA
Texas Instruments
ADS8413EVM Cascade
Feb 05

Appendix C Picture of the Evaluation Board

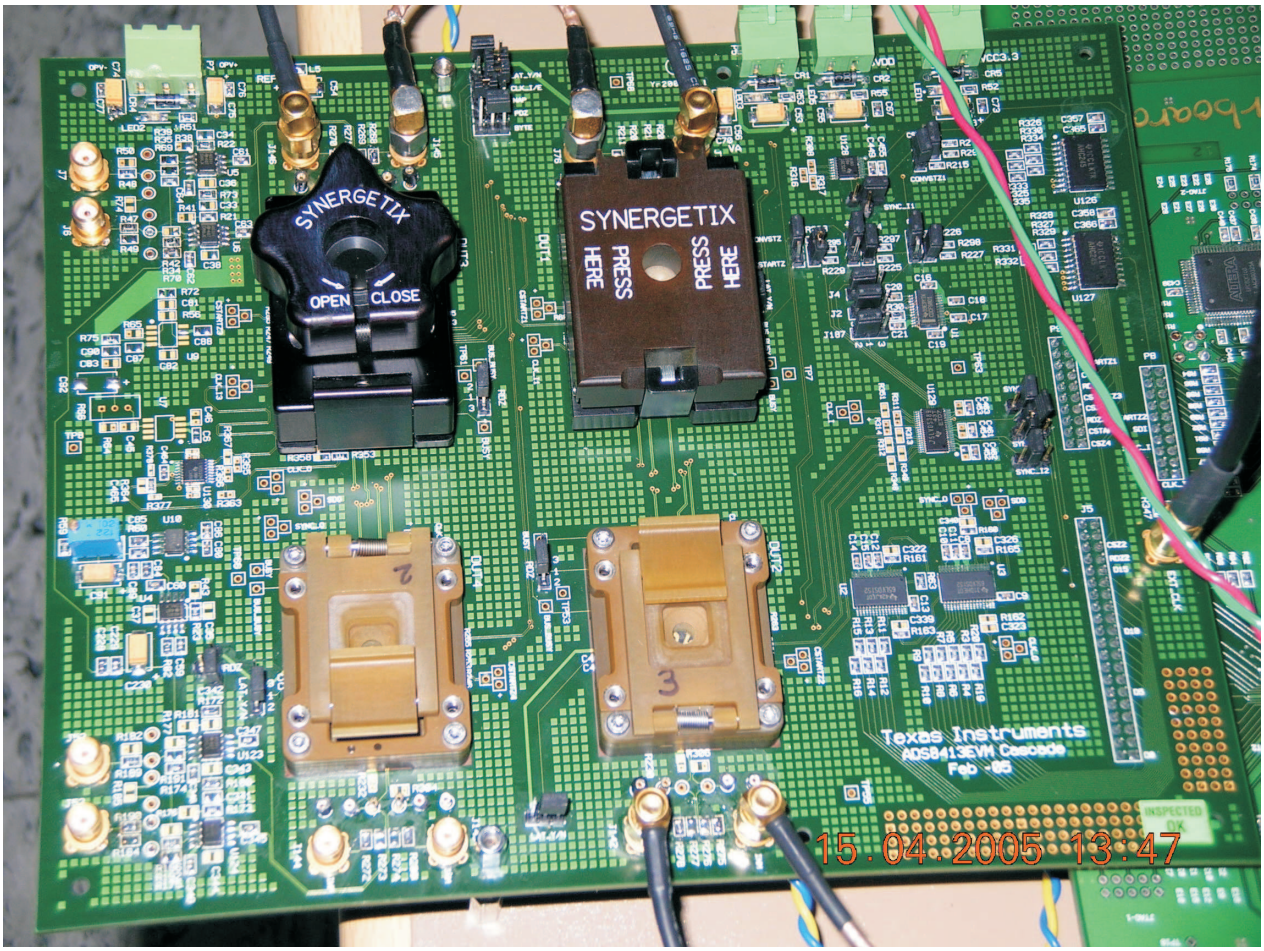

Figure C-1. ADS8413EVM Cascade PCB

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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