# Simple Power Solution Using LDOs for the DM365

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**ABSTRACT**

This reference design is intended for users designing with TMS320DM365 Processor. This design is ideal for achieving the requirement of a input voltage of 5V, and uses LDOs for a simple, small configuration.

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## 1 Introduction

In dual voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

## 2 Power Requirements

The power specifications and sequencing requirements for TMS320DM365 Processor is shown in the table below.

**Table 1. TMS320DM365 Power Specs**

| | Pin Name | Voltage (V) | Imax (mA) | Tolerance | Sequencing Order |
|---|---|---|---|---|---|
| Core | CVDD, VDD12_PRTCSS, VDDA12_DAC, VPP | 1.2 * | 650 | ±5% | 1 |
| I/O | VDDS18, VDD18_PRTCSS, VDDMXI, VDD18_SLDO, VDD18_DDR, VDDA18_PLL, VDDA18_USB, VDDA18_VC, VDDA18_ADC, VDDA18_DAC | 1.8 | 95 | ±5% | 2 |
| I/O | VDDS33, VDDA33_USB, VDDA33_VC | 3.3 | 51 | ±5% | 3 |
| I/O | VDD_AEMIF1_18_3 3, VDD_AEMIF2_18_3 3, VDD_ISIF18_33 | 1.8 / 3.3 | 65 | ±5% | Ramp with appropriate voltage |

**Note:**

- If running DM365 @ 300MHz, then CVDD, VDD12_PRTCSS, VDDA12_DAC and VPP = 1.35V and Imax = 800mA.
- If using PRTCSS, power-up sequencing changes to:
  1. Power on PRTCSS core (1.2-V) while RESET is low
  2. Power on PRTCSS I/O (1.8-V)
  3. Power on Main core (1.2-V)
  4. Power on Main I/O (1.8-V)
  5. Power on Main/Analog I/O (3.3-V)

## 3 Features

The design uses the following LDSOs.

| Devices: | TPS74701(3.3V),TPS74801(1.2V),TPS74701(1.8V) |
|---|---|
| Power supply specs: | |
| Vin | 5 V ± 10% |
| Vout1 | 1.2 V ± 5% at 800 mA |
| Vout2 | 1.8 V ± 5% at 200 mA |
| Vout3 | 3.3 V ± 5% at 200 mA |
| Sequencing | 1) Vout1<br>2) Vout2<br>3) Vout3 |

### TPS74801 and TPS74701

- VOUT Range: 0.8V to 3.6V
- 2% Accuracy Over Line/Load/Temperature
- Programmable Soft-Start Provides Linear Voltage Startup
- Stable with Any Output Capacitor ≥ 2.2µF
- Available in a Small 3mm × 3mm × 1mm SON-10 and 5 × 5 QFN-20 Packages

More information on the Devices can be found from the datasheets.

TPS74801 –SBVS074F

TPS74701 –SBVS099D

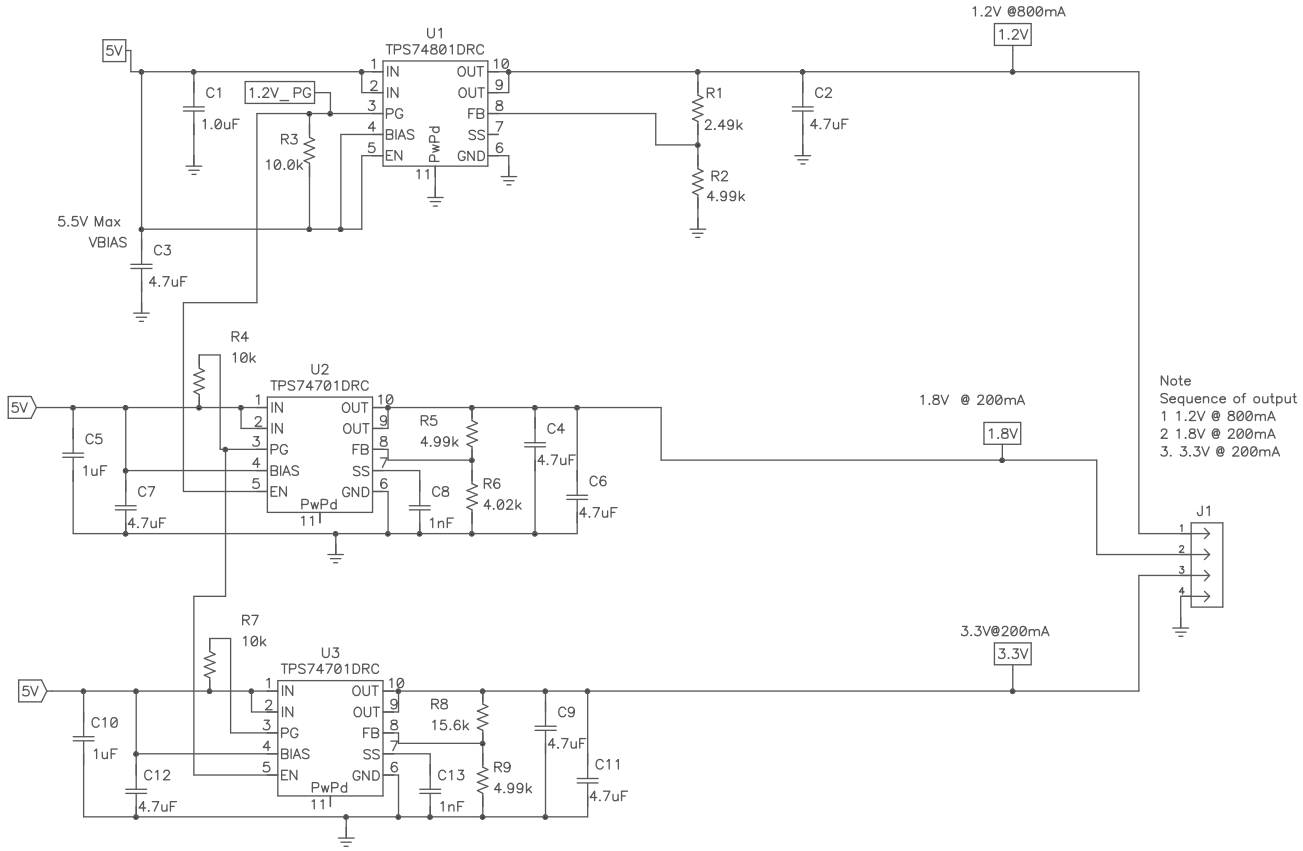


**Figure 1. PMP5048 Reference Design Schematic**

Proper sequencing is achieved in the design with the use of enable pins. The Core 1.2V at 800mA (TPS74801) comes first, PG output of the device then enable the TPS74701 (1.8V) device which in turn enable second TPS74701 (3.3V) device thus, follwoing the required sequence.

# 4 List of Material

**Table 2. PMP5048 List of Materials**

| Count | RefDes | Value | Description | Size | Part Number | MFR | Area |
|---|---|---|---|---|---|---|---|
| 1 | C1 | 1.0 µF | Capacitor, Ceramic, 25V, X5R, 10% | 0603 | C1608X5R1E105K | TDK | 5650 |
| 1 | C2 | 4.7 µF | Capacitor, Ceramic, 6.3V, X5R, 10% | 0603 | C1608X5R0J106M | TDK | 5650 |
| 1 | C3 | 4.7 µF | Capacitor, Ceramic, 6.3V, X5R, 10% | 0603 | C1608X5R0J475K | TDK | 5650 |
| 6 | C4 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| 2 | C5 | 1 µF | Capacitor, Ceramic,1 µF, 16V, X5R | 0603 | C1608X5R1C105K | TDK | 5650 |
| | C6 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| | C7 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| 2 | C8 | 1 nF | Capacitor, Ceramic, 1000 pF, 50V, X7R, 10% | 0603 | C1608X7R1H102K | TDK | 5650 |
| | C9 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| | C10 | 1 µF | Capacitor, Ceramic,1 µF, 16V, X5R | 0603 | C1608X5R1C105K | TDK | 5650 |
| | C11 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| | C12 | 4.7 µF | Capacitor, Ceramic,4.7 µF, 6.3V, X5R | 0603 | C1608X5R0J475M | TDK | 5650 |
| | C13 | 1 nF | Capacitor, Ceramic, 1000 pF, 50V, X7R, 10% | 0603 | C1608X7R1H102K | TDK | 5650 |
| 1 | J1 | PEC36SAAN | Header, Male 4-pin, 100mil spacing, (36-pin strip) | 0.100 inch x 4 | PEC36SAAN | Sullins | 50000 |
| 1 | R1 | 2.49k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std | 5650 |
| 1 | R2 | 4.99k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std | 5650 |
| 1 | R3 | 10.0k | Resistor, Chip, 1/16W, 1% | 0603 | Std | Std | 5650 |
| 2 | R4 | 10k | Resistor, Chip, 10kΩ 1/16W, 5% | 0603 | Std | Std | 5,650 |
| 1 | R5 | 4.99k | Resistor, Chip, 2k49Ω, 1/16W, 5% | 0603 | Std | Std | 5,650 |
| 1 | R6 | 4.02k | Resistor, Chip, 4k99Ω, 1/16W, 5% | 0603 | Std | Std | 5,650 |
| | R7 | 10k | Resistor, Chip, 10kΩ 1/16W, 5% | 0603 | Std | Std | 5,650 |
| 1 | R8 | 15.6k | Resistor, Chip, 2k49Ω, 1/16W, 5% | 0603 | Std | Std | 5,650 |
| 1 | R9 | 4.99k | Resistor, Chip, 4k99Ω, 1/16W, 5% | 0603 | Std | Std | 5,650 |
| 1 | U1 | TPS74801DRC | IC, 1.5A LDO Regulator with Soft-Start | SON-10 | TPS74801DRC | TI | 30400 |
| 2 | U2 | TPS74701DRC | IC, 1.5A LDO Regulator with Soft-Start | SON-10 | TPS74701DRC | TI | 30400 |
| | U3 | TPS74701DRC | IC, 1.5A LDO Regulator with Soft-Start | SON-10 | TPS74701DRC | TI | 30400 |

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

## 5 Test Result

The startup waveform, shown in Figure 2 , demonstrates that the required sequencing order is followed.

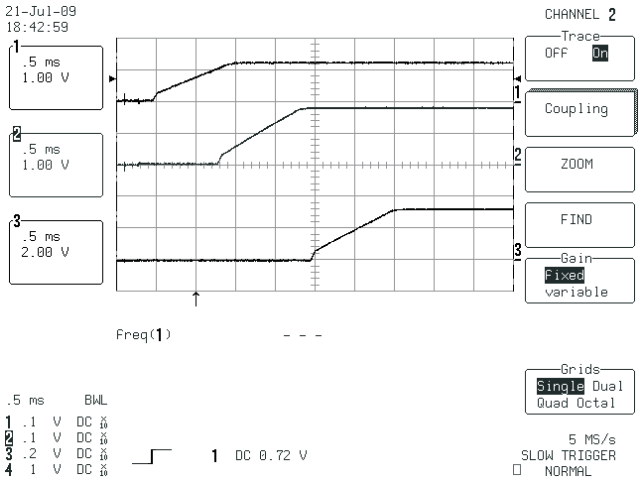


**Figure 2. Shows Sequencing in Start up Waveform**

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