Application Note

Sitara™ Processor Power Distribution Networks: Implementation and Analysis

Dave King

ABSTRACT

The purpose of a power distribution network (PDN) is primarily to provide clean and reliable power to the active devices on the system. The printed circuit board (PCB) is a critical component of the system-level PDN delivery network. As such, optimal design of the PCB power distribution network is of utmost importance for high performance microprocessors. This application report provides implementation guidelines and recommendations for designing printed circuit board (PCB) power delivery networks (PDN) for the Texas Instruments Sitara™ family of microprocessors.

Table of Contents

List of Figures

List of Tables

Trademarks

Sitara™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

This application report provides implementation guidelines and recommendations for designing printed circuit board (PCB) power delivery networks (PDN) for the Texas Instruments Sitara family of microprocessors. This application report will:

- Discuss PCB PDN design methodology
- Provide general PCB PDN design recommendations and requirements
- Discuss the rationale behind these design requirements
- Provide suggestions and methods that PCB designers can implement to ensure that the PDN requirements for a specific processor are met.
- Provide PDN targets for Sitara-class microprocessors

1.1 Acronyms Used in This Document

Table 1-1. Acronyms

Acronym	Description
AC	Alternating current
BGA	Ball grid array
DC	Direct current (static)
Df	Loss tangent
Dk	Dielectric constant
EDA	Electronic design automation
EM	Electromigration
ESL	Effective series inductance
ESR	Effective series resistance
FDTIM	Frequency domain target impedance method
HDI	High density interconnect (for example, buried/blind via)
IR	Product of current (I) x resistance (R)
PCB	Printed circuit board
PDN	Power distribution network
PM-IC/PMIC	Power management integrated circuit
PTH	Plated through hole
RLC	Resistance, inductance, and capacitance
SMPS	Switch mode power supply
SMT	Surface mount technology
SRF	Self resonant frequency
VIP	Via in pad
VRM	Voltage regulator module

Note

Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, for customer boards. The data described in this document are intended as guidelines only.

2 Guidelines for PCB Stack-Up

The PCB stack-up (or layer assignment) is an important factor in ensuring optimal performance of a power distribution scheme. An optimized PCB stack-up for improved power integrity performance can be achieved by following these recommendations:

- Power and ground plane pairs/”islands” should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply. Whenever possible the power and ground planes should be solid to provide a continuous return path for return current.
- Use a thin dielectric between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair so minimizing the separation distance (the dielectric thickness) will help to maximize the capacitance.
- Keep the power and ground plane pair as close to the PCB top and bottom surfaces as possible (see Figure 2-1). This will help to minimize the associated loop inductance of the decoupling capacitors, vias, and the power/ground plane pair spreading loop inductance.

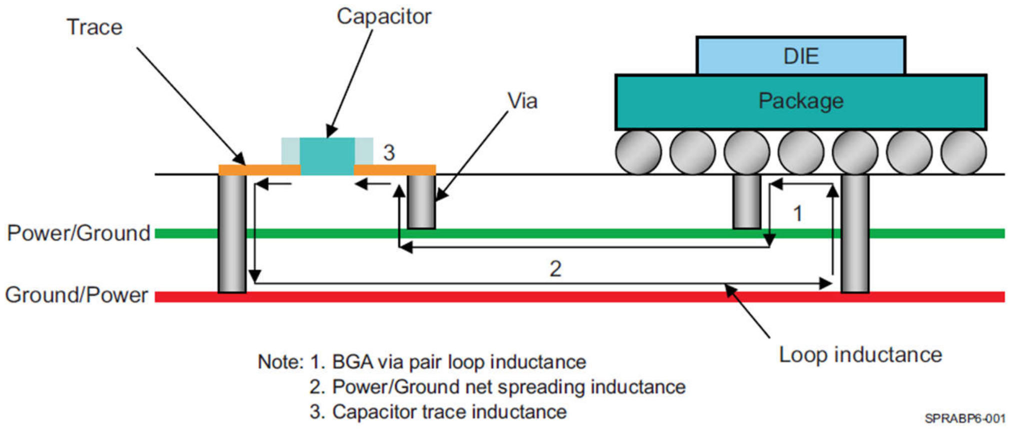


Figure 2-1. Minimize Loop Inductance by Optimizing Layer Assignments in the PCB

The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductance of the power current path as shown above. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, putting high priority supplies in the top half of the stack-up and low-priority supplies in the bottom half of the stack-up as shown in the examples below. Figure 2-2 and Figure 2-3 show examples of typical PCB stack-ups designed with power distribution performance in mind. Device-specific stack-up examples can be found in Section 8.

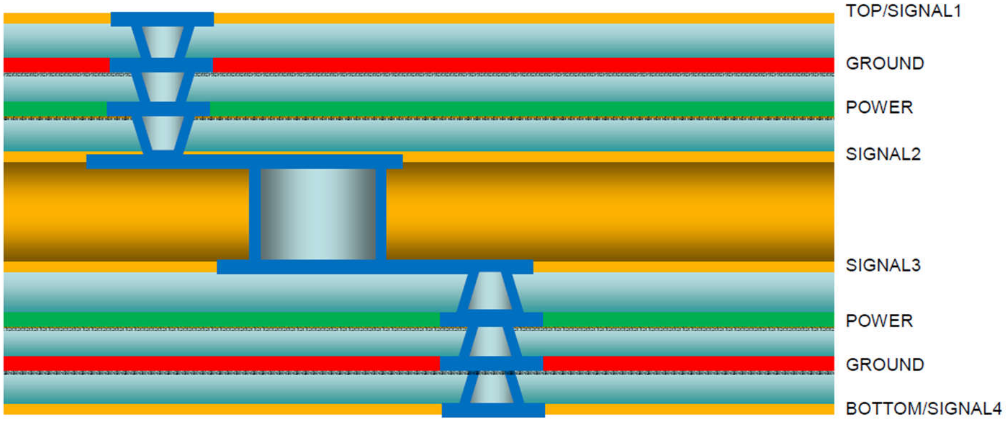


Figure 2-2. Example Stack-Up Utilizing High-Density Interconnect Vias

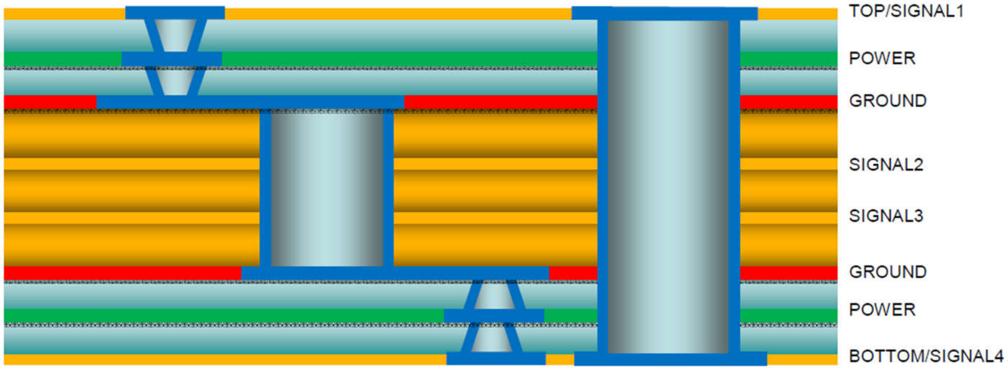


Figure 2-3. Example Stack-Up Utilizing Plated-Through-Hole (PTH) Vias

3 Physical Layout Optimization of the PDN

The following are important requirements that need to be implemented in the PCB PDN design:

- External power trace routing between components should be as wide as possible as wider traces result in reduced DC resistance and consequently a lower static IR drop. They also provide for lower loop inductance and higher capacitance.
- Whenever possible, attempt to achieve a ratio of 1:1 (or better) for component pins and associated vias. Do not share vias among multiple capacitors.
- Placement of decoupling capacitors and associated vias should be as close to the processor ball as possible.
- The maximum current-carrying capacity of each transitional via should be evaluated through simulation to determine the appropriate number of vias required to connect components. This ensures that the current-carrying ability of a via interconnect network is sufficient for the needs of each particular component. When a via interconnect, or a network of same, is unable to supply sufficient current, this is referred to as “via starvation”.
- TI highly recommends that both static and dynamic IR drop analysis (discussed in Section 4 and Section 5) be performed on any new PCB design prior to fabrication. These analyses should be used to assess the appropriate number of vias and geometrical trace width dimensions required to meet the IR drop requirements of system components.
- Whenever possible for the internal layers (both signal routing and power plane), wide traces and copper area fills are recommended for PDN layout. As discussed in previous sections of this document, routing power nets in planes provides for more inter-plane capacitance and improves high frequency performance of the PDN.
- Decoupling capacitors should be mounted with minimum impact to inductance. A capacitor has characteristics not only of capacitance but also inductance and resistance. Figure 3-1 shows the parasitic model of a real capacitor. A real capacitor should be treated as an RLC circuit with effective series resistance (ESR) and effective series inductance (ESL).

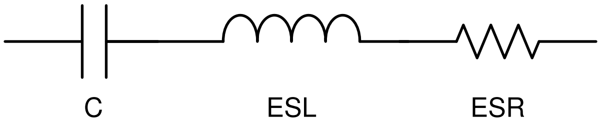


Figure 3-1. Characteristics of a “Real” Capacitor With ESL and ESR

The magnitude of the impedance of this series model is given in Equation 1.

$$|Z| = \sqrt{ESR^2 + \left(wESL - \frac{1}{wC} \right)^2}$$

where

$$w = 2\pi f \quad (1)$$

Figure 3-2 shows the resonant frequency response of a typical capacitor with self-resonant frequency of 55 MHz. The impedance of the capacitor is a combination of its series resistance and reactive capacitance and inductance as shown per Equation 1.

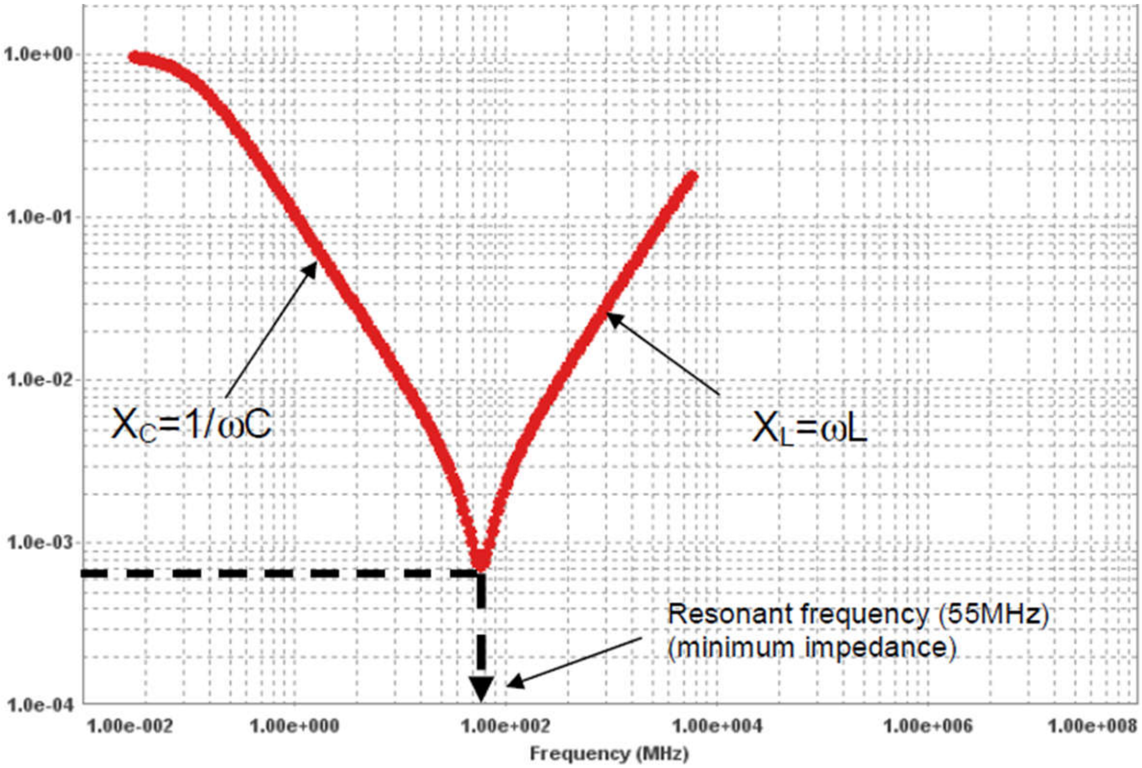


Figure 3-2. Typical Impedance Profile of a Capacitor

- Try to avoid different power nets coupling on the PCB by using "co-planar" shielding whenever appropriate. Figure 3-3 depicts an example of co-planar shielding for two different power nets (VDD_MPU_IVA and VDD_CORE).

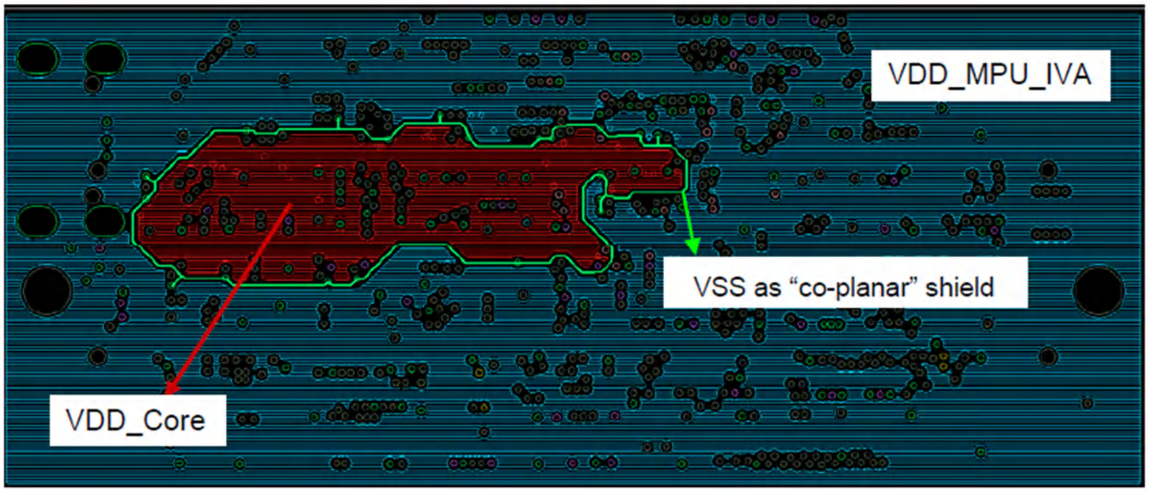


Figure 3-3. Example of "Co-Planar' Shielding of Power Net Using Ground Guard-Band

As the capacitors have both series inductance and resistance that will impact their effectiveness, it is critical that the following recommendations are adopted in placing them on the power distribution network. Whenever possible make sure to mount the capacitor with the geometry that will minimize the mounting inductance and resistance. The capacitor mounting inductance and resistance includes the inductance and resistance of the pads, the trace, and the associated vias.

The length of a trace used to connect a capacitor has a significant impact on the parasitic inductance and resistance of the mounting. This trace should be as short and wide as possible. Wherever possible, minimize the trace by locating vias near the solder pad landing. Further improvements can be made to the mounting by placing vias to the side of capacitor lands or by doubling the number of vias. If the PCB manufacturing process allows, and if cost-effective, via-in-pad (VIP) geometries are strongly recommended.

The most common via placement geometries are proved below, in order of preference for reducing parasitic impact:

1. Via-In-Pad (VIP)
2. Dual Offset Via
3. Single Offset Via
4. Pad to Via Trace (short)
5. Pad to Via Trace (long)

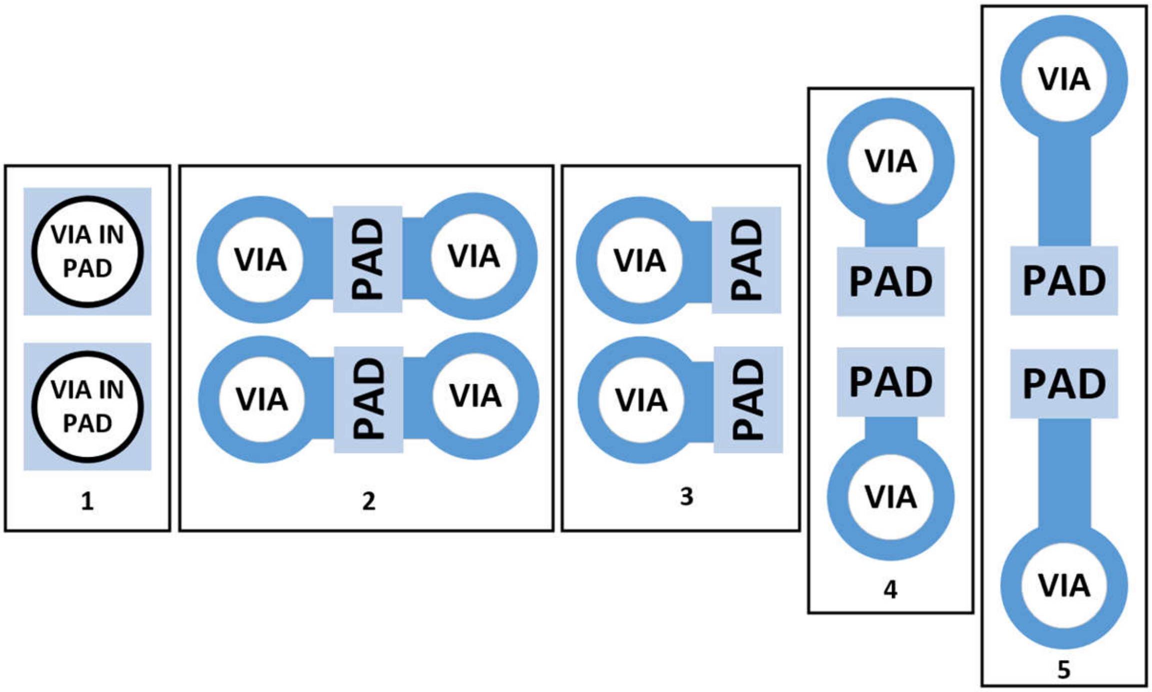
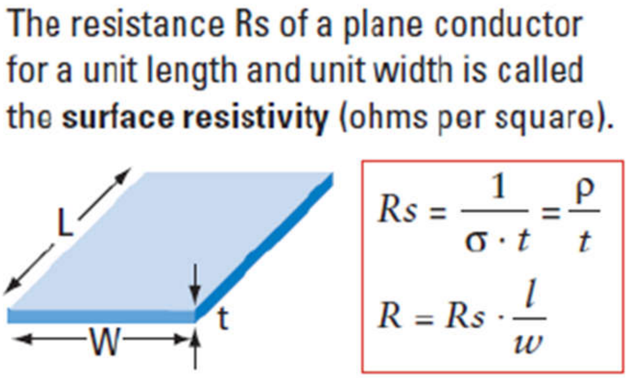


Figure 3-4. Capacitor Mounting Geometries

In addition to mounting inductance and resistance associated with placing a capacitor on the PCB, the effectiveness of a decoupling capacitor also depends on the spreading inductance and resistance that the capacitor sees with respect to the load. The spreading inductance and resistance is strongly dependent on the layer assignment in the PCB stack-up (see Figure 2-1).

4 Static PDN Analysis (IR Drop Optimization)

Delivering reliable power to circuits is always of critical importance as IR drops can occur at every level in a chip, package, and board system. Components that are distant from their associated power source are particularly susceptible to IR drop, and designs that rely on battery power must further minimize voltage drop to avoid unacceptable power loss. Early DC assessments made through simulation help to determine power distribution basics such as the best available entry point for power, layer stack-up choices, and estimates for the amount of copper needed to carry the required current.



The resistance Rs of a plane conductor for a unit length and unit width is called the **surface resistivity** (ohms per square).

$$Rs = \frac{1}{\sigma \cdot t} = \frac{\rho}{t}$$

$$R = Rs \cdot \frac{l}{w}$$

Figure 4-1. Depiction of Sheet Resistivity and Resistance

Ohm’s Law (V=IR) relates conduction current to voltage drop, and at DC, the relation coefficient is a constant representing the resistance of the conductor. Conductors also dissipate power due to their resistance. Both voltage drop and power dissipation are proportional to the resistance of the conductor. Static IR or DC analysis/ design methodology consists of designing the power distribution network such that the voltage drop (under DC operating conditions) across the power and ground pads of the application processor device is within a specified value of the nominal voltage to ensure proper functionality of the device. The PCB-level static IR drop budget is defined between the *pins/pads* of the power management device (PMIC/VRM/SMPS) and the *BGA balls* on the application processor device to which the power management device is supplying power (see Figure 4-2).

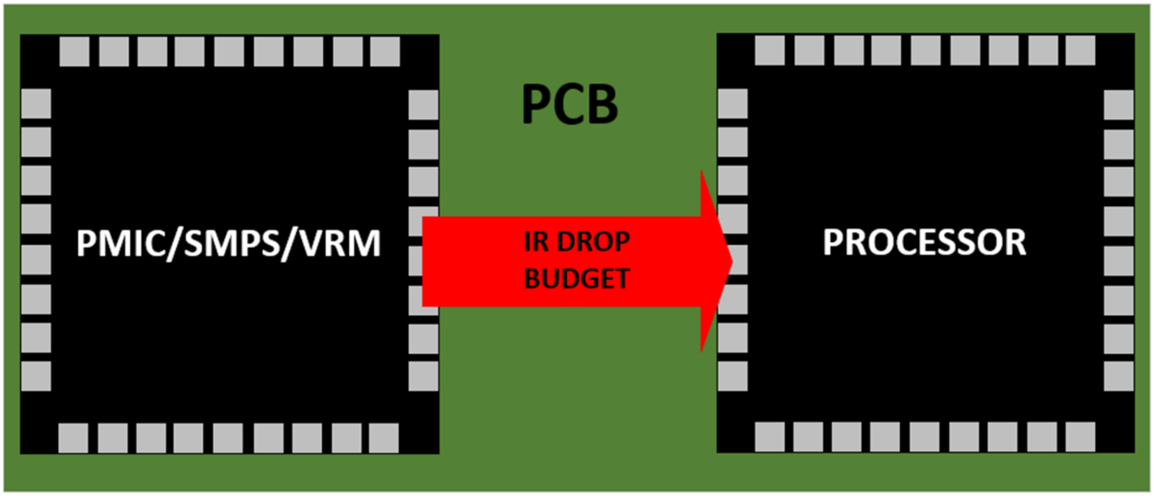


Figure 4-2. PCB IR Drop Budget

Given the total system-level margin allowed for proper device functionality, allowable voltage variation at the BGA of the device is typically specified at 2.5% of the nominal voltage. [1] [1]For devices implementing remote-sense functionality, it is a requirement that the power management device feedback/sense line(s) be placed as close to the relevant processor power balls as physically possible (see Figure 4-3) and that a supply input voltage difference of ≤5 mV under maximum current loading is maintained across all balls connected to a common power rail. This 5 mV maximum represents any voltage difference that may exist between a remote sense point and any associated power input (see Figure 4-4).

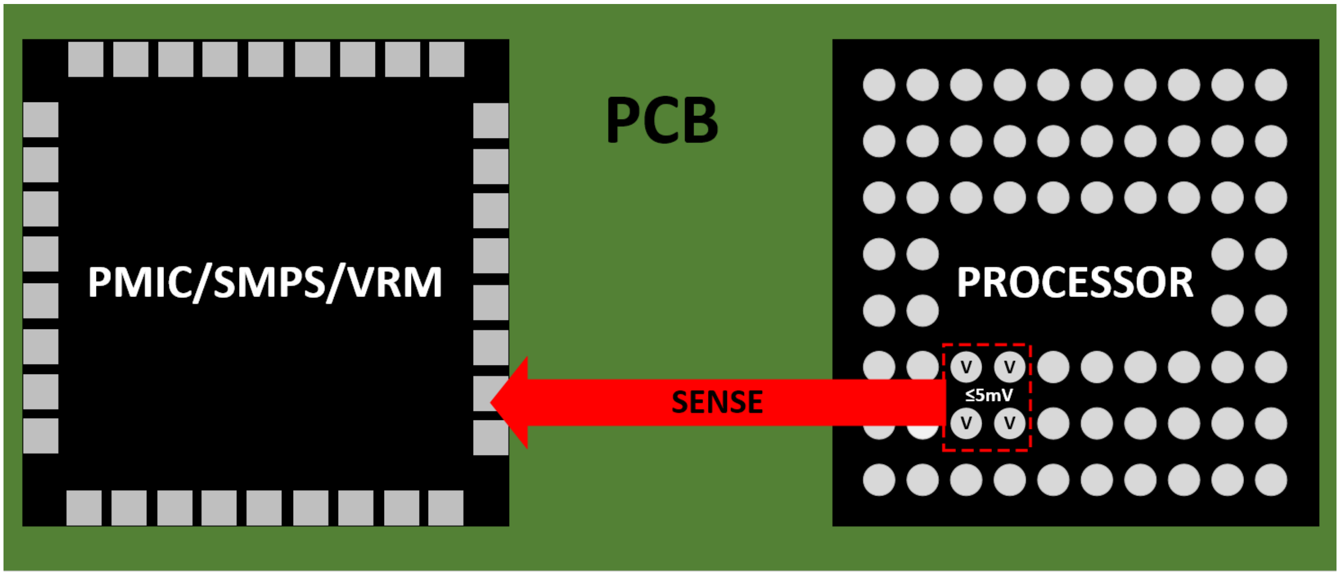


Figure 4-3. Sense Line Placement

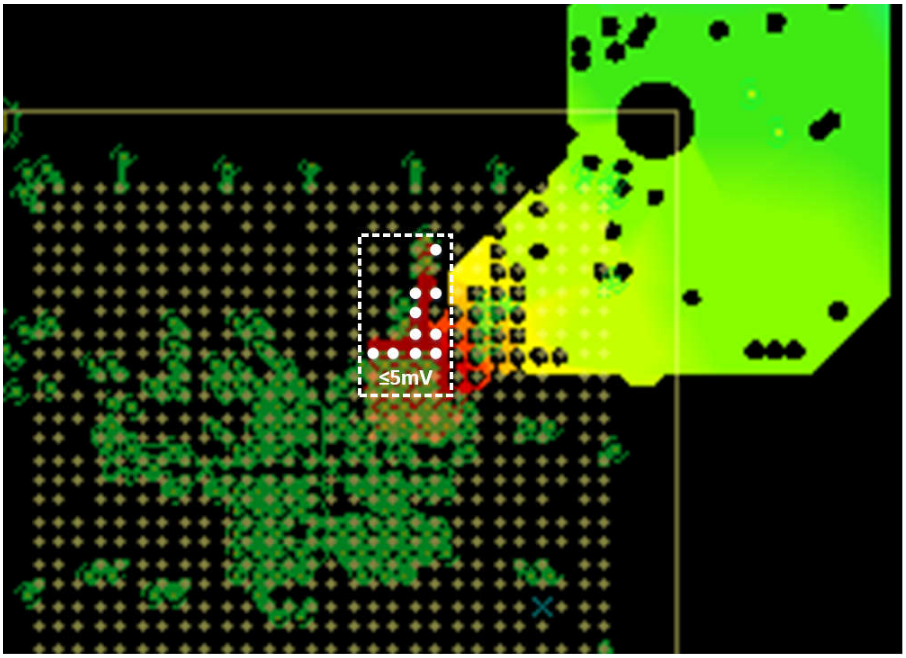


Figure 4-4. Allowable Power Input Voltage Difference

---

[1] This is a generic recommendation and may not apply to your specific processor. For processor requirements, see the device-specific data sheet.

5 Dynamic Analysis of PCB PDN

The typical elements of the PDN are shown in Figure 5-1; which includes the chip-level power distribution with thin-oxide decoupling capacitors. The package-level power distribution with planes and mid-frequency decoupling capacitors; and the board-level (for example, PCB) power distribution with planes, low-frequency ceramic and bulk decoupling capacitors, and the voltage regulator module (VRM).

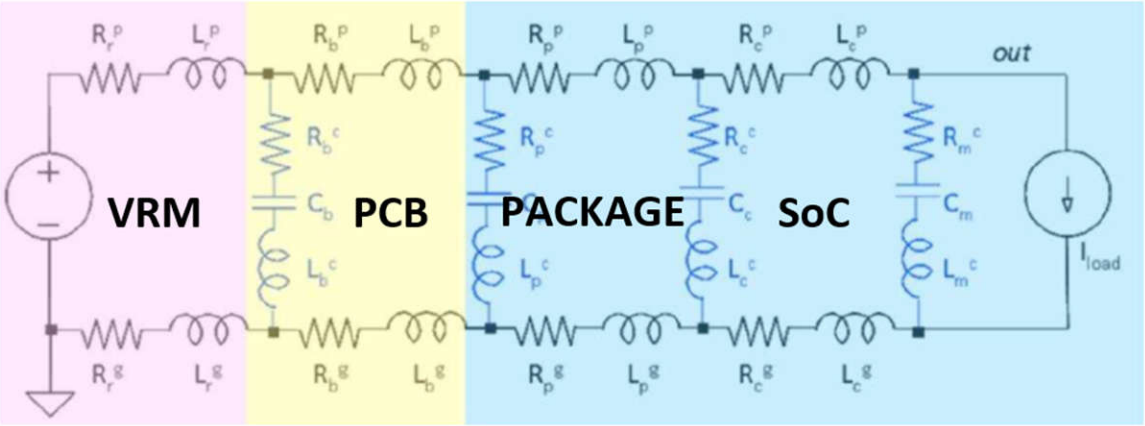


Figure 5-1. Components of a Typical Power Distribution Network (PDN)

The frequency ranges covered by these elements are shown in Figure 5-2. As the primary focus is on optimizing the PCB PDN for high performance, the methodology is developed around the areas over which the PCB designer has control over and can influence early in the design phase.

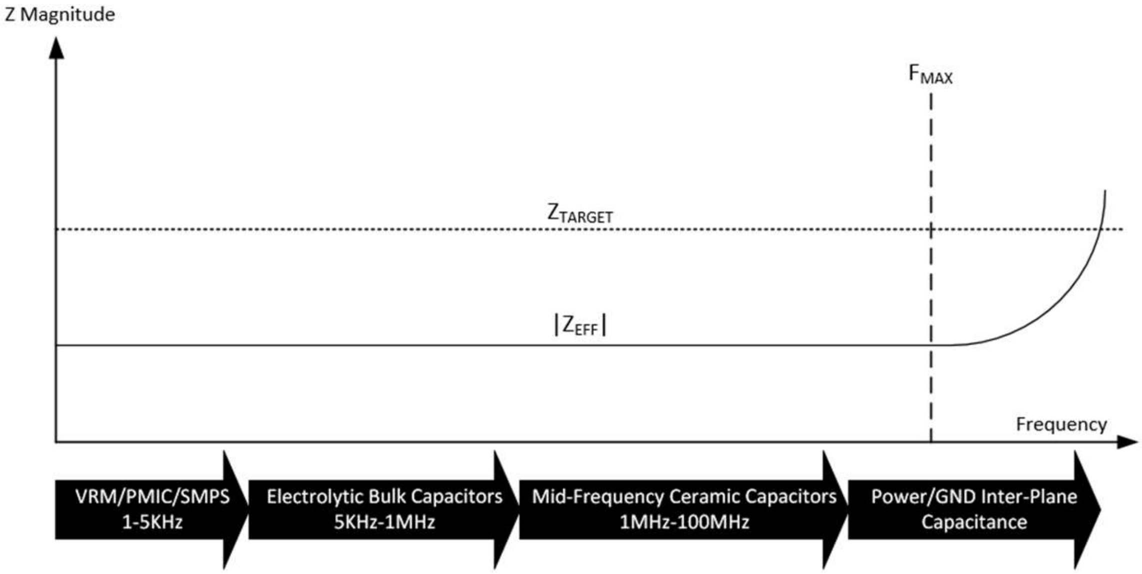


Figure 5-2. Decoupling Frequency Range of PCB Components

The VRM/PMIC/SMPS (or simply voltage regulator device) is the first major component of the PDN. It observes its output voltage and adjusts the amount of current being supplied to keep the voltage constant. Most common voltage regulators make this adjustment on the order of milliseconds to microseconds. They are effective at maintaining output voltage for events at all frequencies from DC to a few kilohertz (depending on the regulator dynamic response time). For all transient events that occur at frequencies above this range, there is a time delay before the voltage regulator can respond to the new level of demand. During this time delay the rail suffers from voltage droop. A power delivery network has an impedance (Z_{PDN}) associated with the path from the voltage regulator module to the processor. The magnitude of noise (voltage ripple) seen on a given power rail is proportional to the impedance (Z_{PDN}) and the transient current ($I_{TRANSIENT}$) draw associated with that rail.

Based on Ohm's Law,

$$V_{RIPPLE} = I_{TRANSIENT} \times Z_{PDN} \tag{2}$$

Typically the transient current is application-specific and is determined by a particular switching scenario. As a board designer, you have the ability to minimize the voltage ripple by reducing Z_{PDN} either by reducing the inductance, or by maximizing the capacitance. To ensure that the voltage ripple noise is within the processor's specification, the Z_{PDN} must be designed to meet a certain impedance, referred to as the target impedance (Z_{TARGET}). Using frequency domain target impedance method (FDTIM) to describe the behavior of a power delivery system has been widely accepted.

The key concept of the FDTIM is the determination of the target impedance Z_{TARGET} (see Equation 3) for the power rail under consideration. For reliable operation of a power delivery system, its impedance spectrum needs to be maintained below the target value at the frequencies from DC to FMAX (see Figure 5-2). FMAX is the point in frequency after which adding a reasonable number of decoupling capacitors does not bring the power rail impedance |ZEFF| below the target impedance (Z_{TARGET}) due to the dominance of the parasitic planar spreading inductance and package inductances.

$$Z_{TARGET} = \frac{\text{Voltage Rail} \times \%\text{Ripple}}{0.5 \times \text{IMax}} \tag{3}$$

5.1 Selecting Decoupling Capacitors to Meet Z_{TARGET}

To maintain power integrity throughout the entire frequency range of interest, the power distribution network relies on the voltage regulator module (VRM/SMPS), the on-board discrete bulk electrolytic and ceramic decoupling capacitors, and the inter-plane capacitances (capacitance from the power-ground sandwich in the board stack-up). For a first-order analysis, the VRM of the power management integrated circuit (PMIC) can be modeled as a series-connected resistor and inductor. A PMIC, at low frequencies (up to 500 KHz-1 MHz), typically has low impedance and is capable of responding to the instantaneous requirements of the processor. The ESR and ESL values for the VRM are therefore very low. Beyond lower frequencies, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement of the device. The bulk and ceramic discrete decoupling capacitors must provide the required low impedance from the point at which the VRM becomes inductive. The effectiveness of the bulk and mid-frequency decoupling capacitors (1 MHz-70 MHz, depending on the capacitor's ESL and ESR) is limited by its placement (due to loop inductance), value, and type. Refer to Figure 5-3 for a capacitor placement example. Note that in order to minimize the loop inductance, the mid-frequency capacitors have been placed directly underneath the processor (on the bottom side of the PCB).

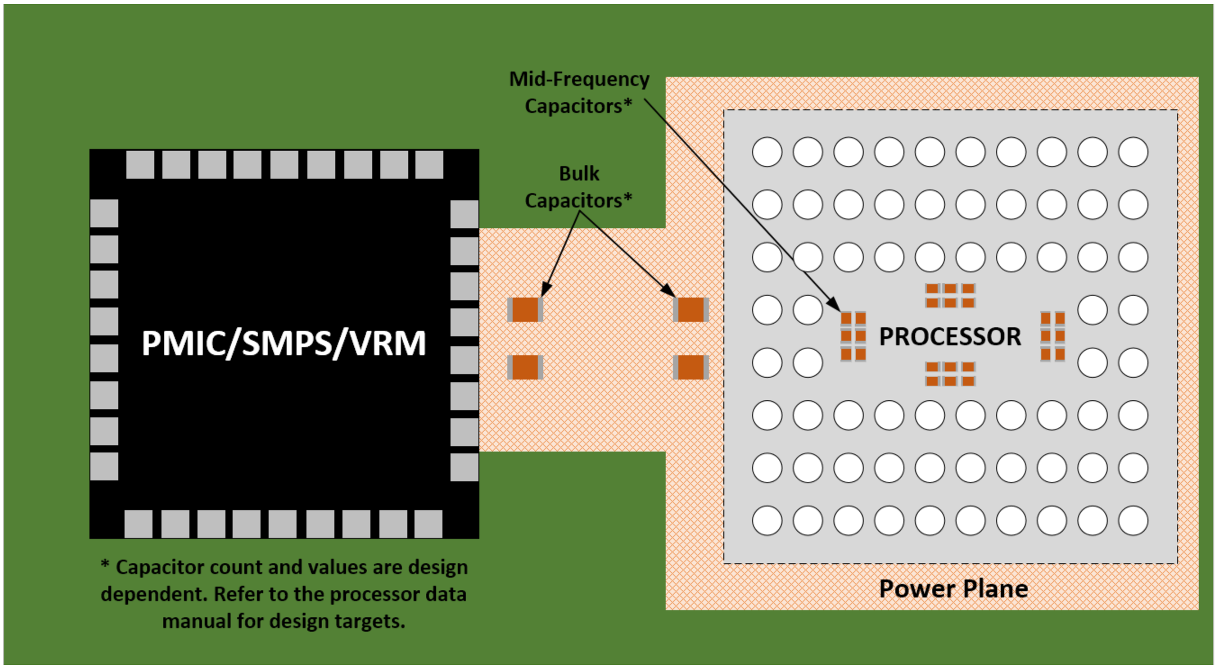


Figure 5-3. Example Capacitor Placement

The bulk capacitors should be located near the point of entry of the supply entrance to the board. The decoupling capacitors maintain the PDN impedance at the required value beyond the VRM frequency and until the frequency at which mid-frequency capacitors become useful. The mid-frequency SMT capacitors are useful in the 10 to 150 MHz range and higher. These capacitors are primarily ceramic capacitors that come in several dielectric types (NPO, X7R, X5R, and Y5V) and several sizes (1206, 0805, 0603, 0402, and so forth). The mid-frequency capacitors are much smaller than the bulk capacitors and can be placed closer to the transistor circuit. Since the ceramic capacitors are smaller, they have lower ESR and ESL and lower capacitance than bulk capacitors, leading to a higher resonance frequency with smaller impedance at resonance. Therefore, ceramic capacitors can be used at higher frequencies. Typical mid-frequency capacitors have capacitance in the range of 1 nF –100 nF, ESR in the range of 10-100 mΩ, and ESL in the range of 0.5 nH – 1 nH.

The concept of “loop inductance” is a useful metric for quantifying the effectiveness of the decoupling capacitors of a power distribution network. To calculate the “loop inductance” associated with decoupling capacitor placement, Equation 4 can be used:

$$L_{eff} = \frac{\text{Imaginary}\left(Z\left(\text{Power,GND pads of decap}\right)\right)}{2 \times \pi \times \text{Frequency}} \tag{4}$$

Where L_{eff} is the effective loop inductance, Z (power, GND pads of decap) represents the Z-parameters of the port defined across the power and ground pads of the corresponding decap. The frequency should be chosen in the “flat” region of the Z-parameter response, typically in the 50 MHz – 70 MHz range.

6 Checklist for PDN

Although this list is not inclusive of every parameter and variable that must be considered when designing a PCB, a PDN-optimized PCB design will implement these guidelines:

- Power and ground plane pairs (or “islands”) should be closely coupled together. The capacitance formed between the planes can be used to decouple the power supply at high frequencies.
- Whenever possible, the power and ground planes should be solid as this provides a continuous return path for return current.
- Use a thin dielectric thickness between the power and ground plane pair. Capacitance is inversely proportional to the separation of the plane pair so minimizing the separation distance (such as, the dielectric thickness) will maximize the resulting capacitance.
- The placement of power and ground planes in the PCB stack-up (determined by layer assignment) has a significant impact on the parasitic inductances of power current path. For this reason, it is recommended to consider layer order in the early stages of the PCB PDN design cycle, placing high priority supplies in the upper-half of the stack-up and low priority supplies in the lower half of the stack-up. This helps to minimize the loop inductance caused by decoupling capacitors and their associated vias.
- External power trace routing between components should be as wide as possible as wider traces result in reduced DC resistance and consequently a lower static IR drop.
- Whenever possible, attempt to achieve a ratio of 1:1 (or better) for component pins and associated vias. Do not share vias among multiple capacitors.
- Placement of decoupling capacitors and their associated vias should be as close to the processor ball as possible. Reserve the space directly underneath the processor for this purpose.
- Use of short and wide surface traces to connect capacitor pads to the vias connected to the planes below is preferred.
- Use of large diameter vias is preferred for reduced inductance/resistance.
- 1 oz – 2 oz Cu weight for power / ground plane is preferred to enable better PCB heat spreading, which helps to reduce processor junction temperatures. In addition, it is preferable to have the power / ground planes be located adjacent to the PCB surface on which the processor is mounted.
- Place the VRM as close as possible to the processor and on the same side of the PCB. In cases where a power management IC (PMIC) is implemented as the VRM, it should be aligned to minimize distance for the highest current rail.

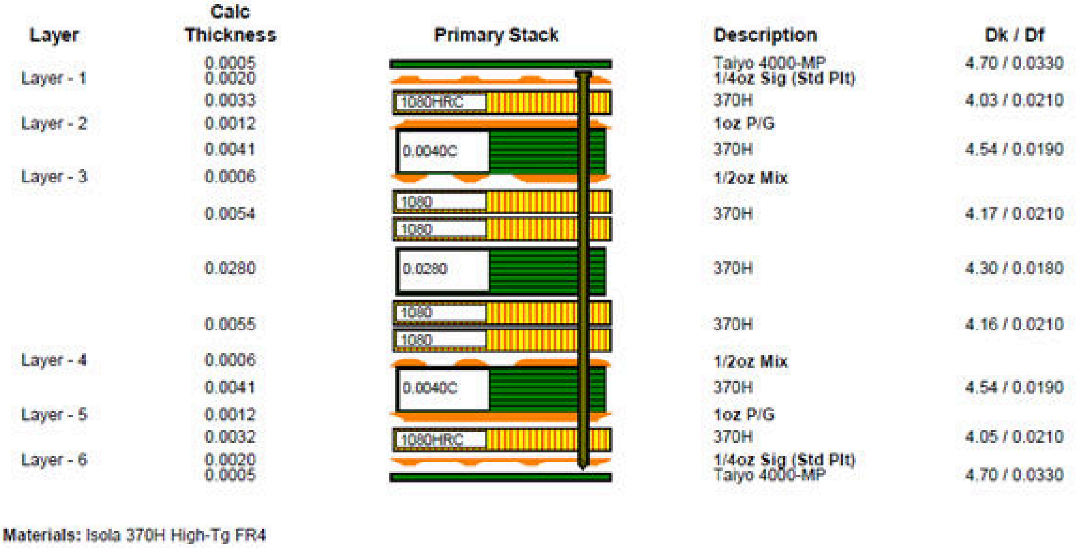
7 Implementation Examples and PDN Targets

This section provides device-specific PDN targets and implementation examples that meet these targets.

Note

The decoupling capacitor counts and/or capacitor values presented in this document are PCB design-specific and should not be used in lieu of PCB simulations. It is the responsibility of the PCB designer to ensure that any design meets the provided PDN targets.

7.1 AM570x

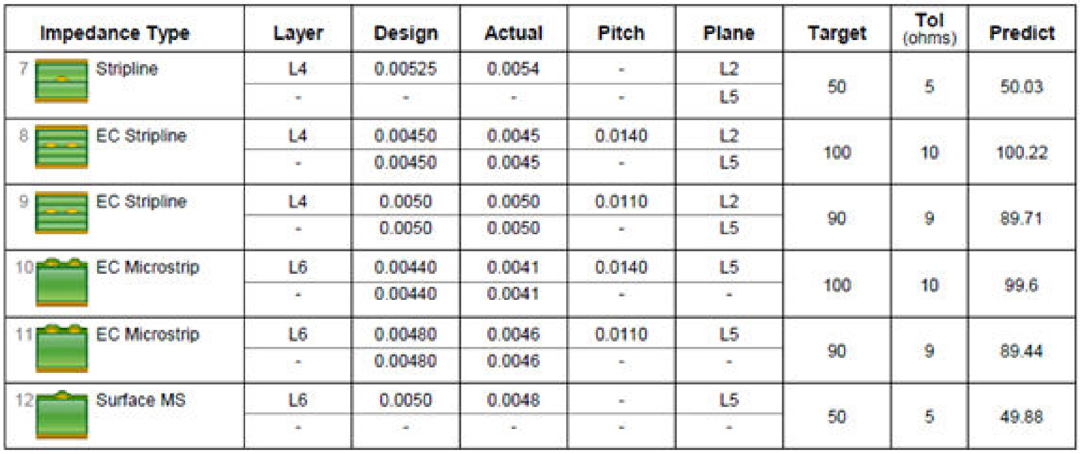


Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0005		Taiyo 4000-MP	4.70 / 0.0330
Layer - 1	0.0020		1/4oz Sig (Std Plt)	
	0.0033	1080HRC	370H	4.03 / 0.0210
Layer - 2	0.0012		1oz P/G	
	0.0041	0.0040C	370H	4.54 / 0.0190
Layer - 3	0.0006		1/2oz Mix	
	0.0054	1080 1080	370H	4.17 / 0.0210
	0.0280	0.0280	370H	4.30 / 0.0180
	0.0055	1080 1080	370H	4.16 / 0.0210
Layer - 4	0.0006		1/2oz Mix	
	0.0041	0.0040C	370H	4.54 / 0.0190
Layer - 5	0.0012		1oz P/G	
	0.0032	1080HRC	370H	4.05 / 0.0210
Layer - 6	0.0020		1/4oz Sig (Std Plt)	
	0.0005		Taiyo 4000-MP	4.70 / 0.0330

Materials: Isola 370H High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0620	0.0062	0.0062	0.0622
Incl. Mask over Laminate	0.0580	0.0058	0.0058	0.0582
Incl. Plating	0.0610	0.0061	0.0061	0.0612
After Lamination	0.0576	0.0029	0.0029	0.0578
Over Laminate	0.0570	0.0057	0.0057	0.0572

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1 Surface MS	L1	0.0050	0.0050	-	-	50	5	49.89
	-	-	-	-	L2			
2 EC Microstrip	L1	0.00480	0.0046	0.0110	-	90	9	90.71
	-	0.00480	0.0046	-	L2			
3 EC Microstrip	L1	0.00440	0.0042	0.0140	-	100	10	100.04
	-	0.00440	0.0042	-	L2			
4 Stripline	L3	0.00525	0.0054	-	L2	50	5	50.01
	-	-	-	-	L5			
5 EC Stripline	L3	0.00450	0.0045	0.0140	L2	100	10	100.18
	-	0.00450	0.0045	-	L5			
6 EC Stripline	L3	0.0050	0.0050	0.0110	L2	90	9.0	89.67
	-	0.0050	0.0050	-	L5			



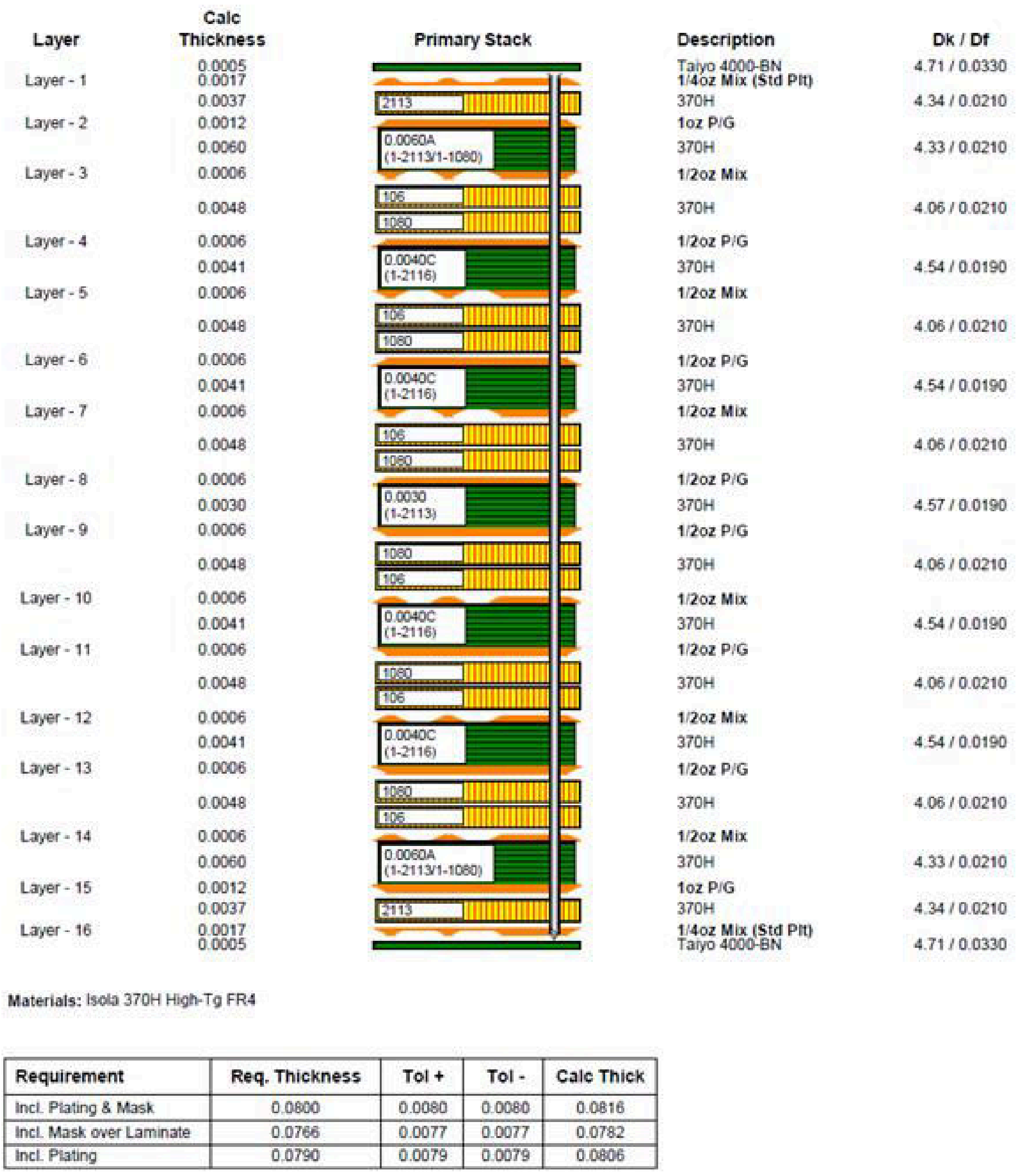
Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
7 Stripline	L4	0.00525	0.0054	-	L2	50	5	50.03
	-	-	-	-	L5			
8 EC Stripline	L4	0.00450	0.0045	0.0140	L2	100	10	100.22
	-	0.00450	0.0045	-	L5			
9 EC Stripline	L4	0.0050	0.0050	0.0110	L2	90	9	89.71
	-	0.0050	0.0050	-	L5			
10 EC Microstrip	L6	0.00440	0.0041	0.0140	L5	100	10	99.6
	-	0.00440	0.0041	-	-			
11 EC Microstrip	L6	0.00480	0.0046	0.0110	L5	90	9	89.44
	-	0.00480	0.0046	-	-			
12 Surface MS	L6	0.0050	0.0048	-	L5	50	5	49.88
	-	-	-	-	-			

Table 7-1. AM570x PDN Targets and Decoupling Example

	Static PDN Target	Dynamic PDN Targets			Number of Decoupling Capacitors Per Supply (1) (2) (3) (4) (5) (6) (9)							
Supply Name(10)	Max R_{eff} (mΩ) (7)	Dec Cap Max LL (nH) (6) (8)	Max Impedance (mΩ)	Frequency of Interest (MHz)	100 nF	220 nF	470 nF	1 µF	2.2 µF	4.7 µF	10 µF	22 µF
VDD_CORE	18	2	57	≤20			5	4			1	
VDD_DSP	22	2.5	54	≤20			6	5			2	
VDDS_DDR1	10	2.5	200	≤100			12	1			1	
CAP_VBBLDO_DSP	N/A	6	N/A	N/A				1				
CAP_VBBLDO_GPU	N/A	6	N/A	N/A				1				
CAP_VBBDLO_IVA	N/A	6	N/A	N/A				1				
CAP_VBBLD0_MPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE2	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE3	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE4	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSP	N/A	6	N/A	N/A				1				
CAP_VDDRAM_GPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_IVA	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU	N/A	6	N/A	N/A				1				

(1) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
(2) ESL must be as low as possible and not exceed 0.5 nH.
(3) The power delivery network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table in the *Specifications* chapter of the device-specific data manual.
(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
(6) High-frequency (30 MHz – 70 MHz) PCB decoupling capacitors.
(7) Maximum R_{eff} from VRM/SMPS/PMIC to processor.
(8) Maximum loop inductance for decoupling capacitor.
(9) Decoupling capacitor counts and values are provided as a baseline recommendation only. TI recommends that all PCB designs be simulated prior fabrication to ensure that the processor PDN requirements are met.
(10) Ganged rails must meet all requirements of each member rail.

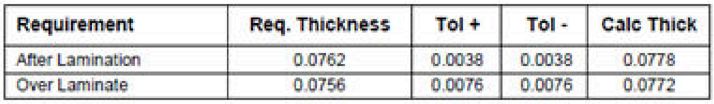
7.2 AM571x



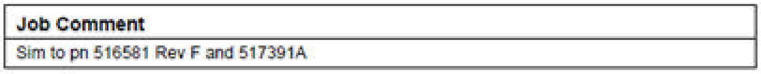
Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0005		Taiyo 4000-BN	4.71 / 0.0330
Layer - 1	0.0017		1/4oz Mix (Std Plt)	
	0.0037	2113	370H	4.34 / 0.0210
Layer - 2	0.0012		1oz P/G	
	0.0060	0.0060A (1-2113/1-1080)	370H	4.33 / 0.0210
Layer - 3	0.0006		1/2oz Mix	
	0.0048	106 1080	370H	4.06 / 0.0210
Layer - 4	0.0006		1/2oz P/G	
	0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 5	0.0006		1/2oz Mix	
	0.0048	106 1080	370H	4.06 / 0.0210
Layer - 6	0.0006		1/2oz P/G	
	0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 7	0.0006		1/2oz Mix	
	0.0048	106 1080	370H	4.06 / 0.0210
Layer - 8	0.0006		1/2oz P/G	
	0.0030	0.0030 (1-2113)	370H	4.57 / 0.0190
Layer - 9	0.0006		1/2oz P/G	
	0.0048	1080 106	370H	4.06 / 0.0210
Layer - 10	0.0006		1/2oz Mix	
	0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 11	0.0006		1/2oz P/G	
	0.0048	1080 106	370H	4.06 / 0.0210
Layer - 12	0.0006		1/2oz Mix	
	0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 13	0.0006		1/2oz P/G	
	0.0048	1080 106	370H	4.06 / 0.0210
Layer - 14	0.0006		1/2oz Mix	
	0.0060	0.0060A (1-2113/1-1080)	370H	4.33 / 0.0210
Layer - 15	0.0012		1oz P/G	
	0.0037	2113	370H	4.34 / 0.0210
Layer - 16	0.0017		1/4oz Mix (Std Plt)	
	0.0005		Taiyo 4000-BN	4.71 / 0.0330

Materials: Isola 370H High-Tg FR4

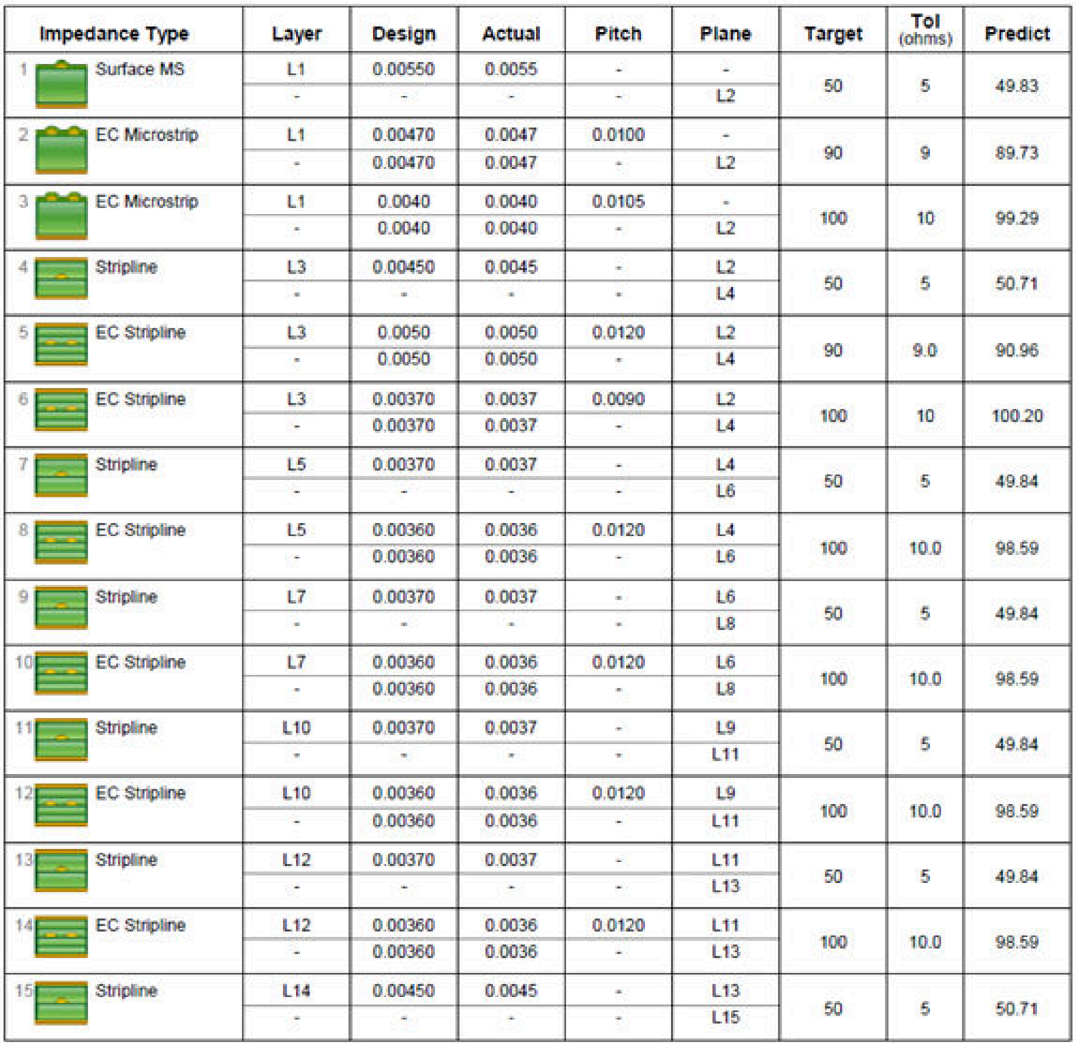
Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0800	0.0080	0.0080	0.0816
Incl. Mask over Laminate	0.0766	0.0077	0.0077	0.0782
Incl. Plating	0.0790	0.0079	0.0079	0.0806



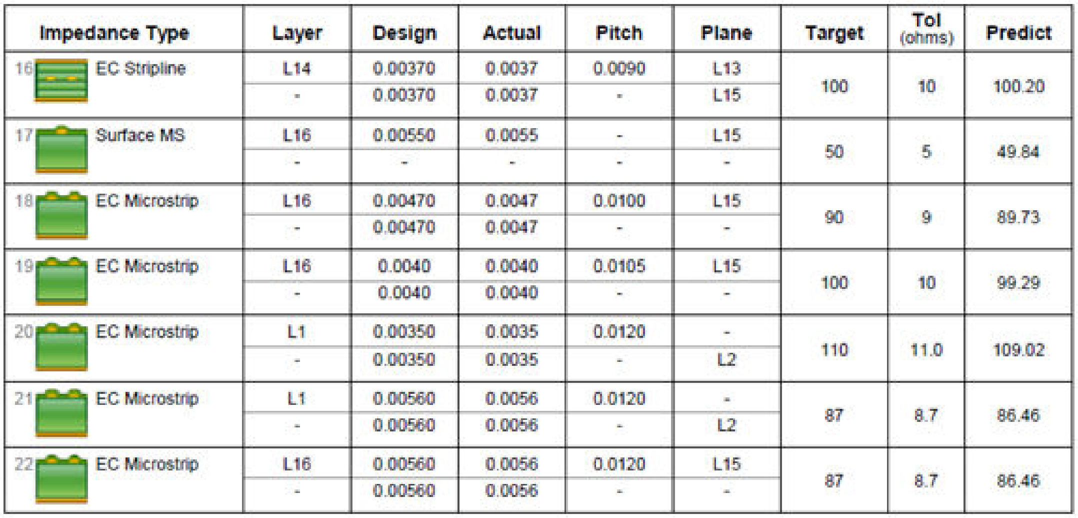
Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
After Lamination	0.0762	0.0038	0.0038	0.0778
Over Laminate	0.0756	0.0076	0.0076	0.0772



Job Comment
Sim to pn 516581 Rev F and 517391A



Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1 Surface MS	L1	0.00550	0.0055	-	-	50	5	49.83
	-	-	-	-	L2			
2 EC Microstrip	L1	0.00470	0.0047	0.0100	-	90	9	89.73
	-	0.00470	0.0047	-	L2			
3 EC Microstrip	L1	0.0040	0.0040	0.0105	-	100	10	99.29
	-	0.0040	0.0040	-	L2			
4 Stripline	L3	0.00450	0.0045	-	L2	50	5	50.71
	-	-	-	-	L4			
5 EC Stripline	L3	0.0050	0.0050	0.0120	L2	90	9.0	90.96
	-	0.0050	0.0050	-	L4			
6 EC Stripline	L3	0.00370	0.0037	0.0090	L2	100	10	100.20
	-	0.00370	0.0037	-	L4			
7 Stripline	L5	0.00370	0.0037	-	L4	50	5	49.84
	-	-	-	-	L6			
8 EC Stripline	L5	0.00360	0.0036	0.0120	L4	100	10.0	98.59
	-	0.00360	0.0036	-	L6			
9 Stripline	L7	0.00370	0.0037	-	L6	50	5	49.84
	-	-	-	-	L8			
10 EC Stripline	L7	0.00360	0.0036	0.0120	L6	100	10.0	98.59
	-	0.00360	0.0036	-	L8			
11 Stripline	L10	0.00370	0.0037	-	L9	50	5	49.84
	-	-	-	-	L11			
12 EC Stripline	L10	0.00360	0.0036	0.0120	L9	100	10.0	98.59
	-	0.00360	0.0036	-	L11			
13 Stripline	L12	0.00370	0.0037	-	L11	50	5	49.84
	-	-	-	-	L13			
14 EC Stripline	L12	0.00360	0.0036	0.0120	L11	100	10.0	98.59
	-	0.00360	0.0036	-	L13			
15 Stripline	L14	0.00450	0.0045	-	L13	50	5	50.71
	-	-	-	-	L15			



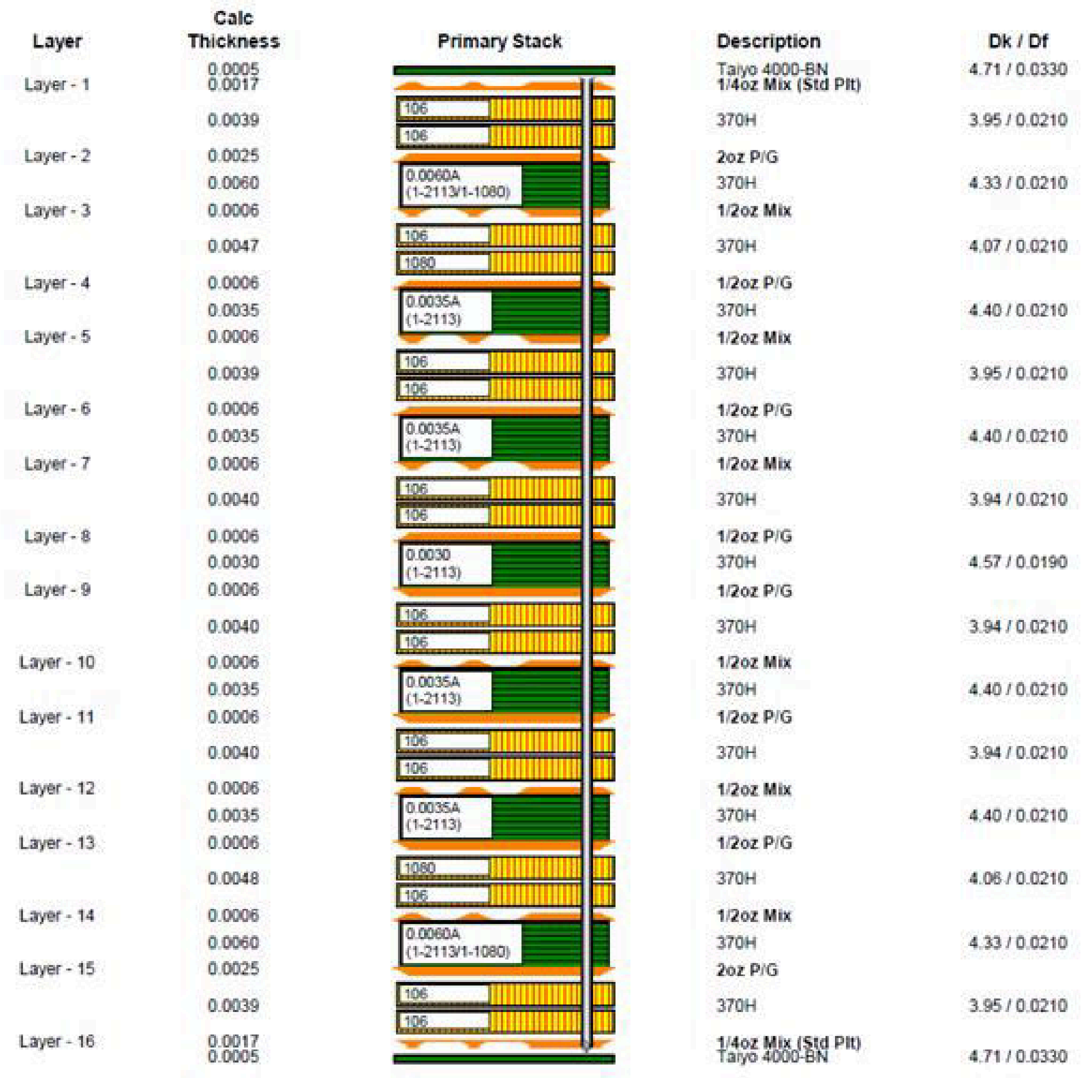
Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
16 EC Stripline	L14	0.00370	0.0037	0.0090	L13	100	10	100.20
	-	0.00370	0.0037	-	L15			
17 Surface MS	L16	0.00550	0.0055	-	L15	50	5	49.84
	-	-	-	-	-			
18 EC Microstrip	L16	0.00470	0.0047	0.0100	L15	90	9	89.73
	-	0.00470	0.0047	-	-			
19 EC Microstrip	L16	0.0040	0.0040	0.0105	L15	100	10	99.29
	-	0.0040	0.0040	-	-			
20 EC Microstrip	L1	0.00350	0.0035	0.0120	-	110	11.0	109.02
	-	0.00350	0.0035	-	L2			
21 EC Microstrip	L1	0.00560	0.0056	0.0120	-	87	8.7	86.46
	-	0.00560	0.0056	-	L2			
22 EC Microstrip	L16	0.00560	0.0056	0.0120	L15	87	8.7	86.46
	-	0.00560	0.0056	-	-			

Table 7-2. AM571x PDN Targets and Decoupling Example

	Static PDN Target	**Dynamic PDN Targets**			**Number of Decoupling Capacitors Per Supply** (1) (2) (3) (4) (5) (6) (9)							
Supply Name(10)	**Max R_{eff} (mΩ)** (7)	**Dec Cap Max LL (nH)** (6) (8)	**Max Impedance (mΩ)**	**Frequency of Interest (MHz)**	**100 nF**	**220 nF**	**470 nF**	**1 µF**	**2.2 µF**	**4.7 µF**	**10 µF**	**22 µF**
VDD_CORE	27	2	87	≤50	6	1	1	1	1	1		
VDD_MPU	10	2	57	≤20	8	1	1	1	1	1		1
VDD_DSP VDD_GPU VDD_IVA	13	2.5	54	≤20	8	1	1	1	1	1	1	1
VDDS_DDR1	10	2.5	200	≤100	8	4		2		2		1
CAP_VBBLDO_DSP	N/A	6	N/A	N/A				1				
CAP_VBBLDO_GPU	N/A	6	N/A	N/A				1				
CAP_VBBDLO_IVA	N/A	6	N/A	N/A				1				
CAP_VBBLD0_MPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE3	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE4	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSP	N/A	6	N/A	N/A				1				
CAP_VDDRAM_GPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_IVA	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU	N/A	6	N/A	N/A				1				

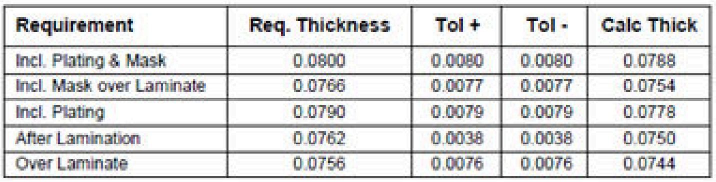
(1) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
(2) ESL must be as low as possible and not exceed 0.5 nH.
(3) The power delivery network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table in the *Specifications* chapter of the device-specific data manual.
(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
(6) High-frequency (30 MHz – 70 MHz) PCB decoupling capacitors.
(7) Maximum R_{eff} from VRM/SMPS/PMIC to processor.
(8) Maximum loop inductance for decoupling capacitor.
(9) Decoupling capacitor counts and values are provided as a baseline recommendation only. TI recommends that all PCB designs be simulated prior fabrication to ensure that the processor PDN requirements are met.
(10) Ganged rails must meet all requirements of each member rail.

7.3 AM572x

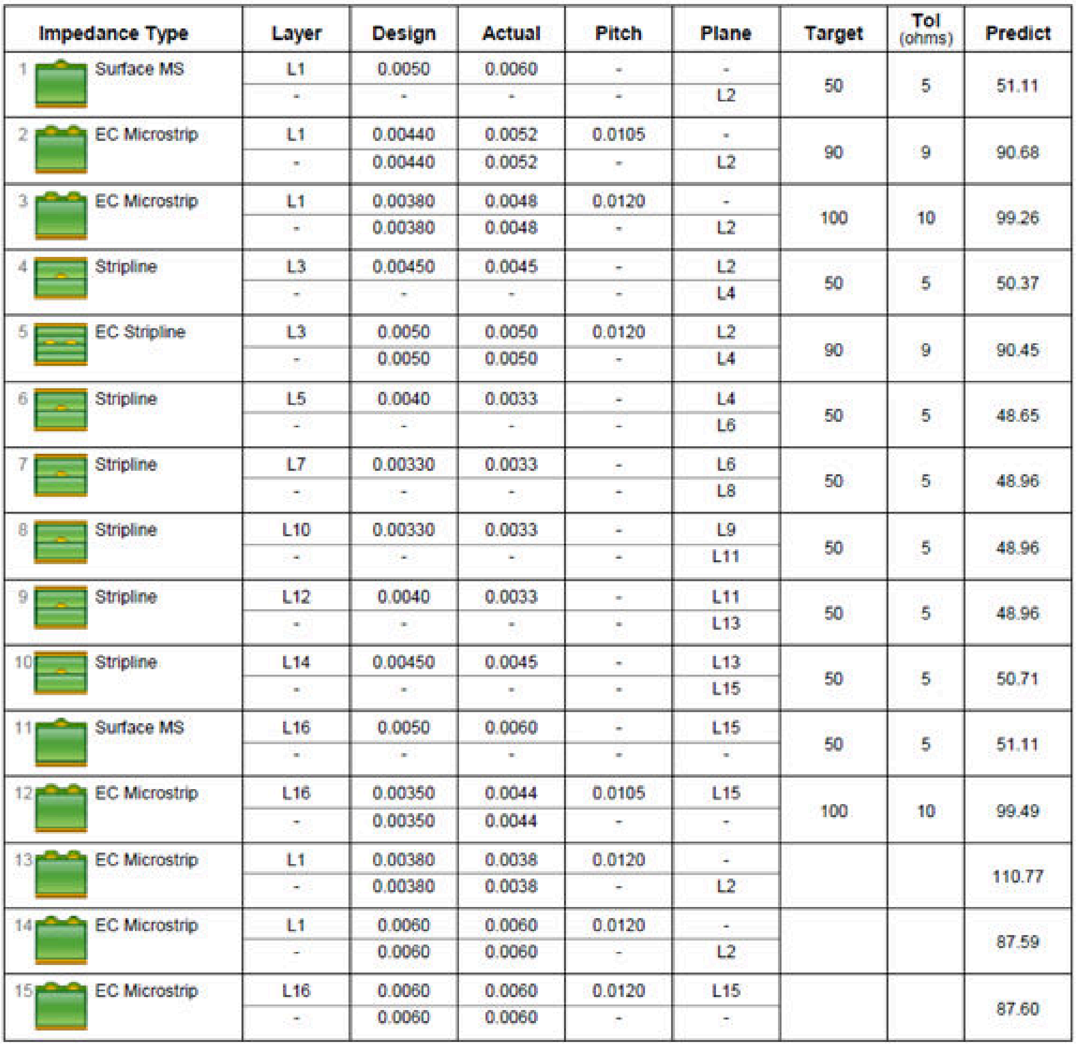


Layer	Calc Thickness	Primary Stack	Description	Dk / Df
	0.0005		Taiyo 4000-BN	4.71 / 0.0330
Layer - 1	0.0017		1/4oz Mix (Std Plt)	
	0.0039	106 106	370H	3.95 / 0.0210
Layer - 2	0.0025		2oz P/G	
	0.0060	0.0060A (1-2113/1-1080)	370H	4.33 / 0.0210
Layer - 3	0.0006		1/2oz Mix	
	0.0047	106 1080	370H	4.07 / 0.0210
Layer - 4	0.0006		1/2oz P/G	
	0.0035	0.0035A (1-2113)	370H	4.40 / 0.0210
Layer - 5	0.0006		1/2oz Mix	
	0.0039	106 106	370H	3.95 / 0.0210
Layer - 6	0.0006		1/2oz P/G	
	0.0035	0.0035A (1-2113)	370H	4.40 / 0.0210
Layer - 7	0.0006		1/2oz Mix	
	0.0040	106 106	370H	3.94 / 0.0210
Layer - 8	0.0006		1/2oz P/G	
	0.0030	0.0030 (1-2113)	370H	4.57 / 0.0190
Layer - 9	0.0006		1/2oz P/G	
	0.0040	106 106	370H	3.94 / 0.0210
Layer - 10	0.0006		1/2oz Mix	
	0.0035	0.0035A (1-2113)	370H	4.40 / 0.0210
Layer - 11	0.0006		1/2oz P/G	
	0.0040	106 106	370H	3.94 / 0.0210
Layer - 12	0.0006		1/2oz Mix	
	0.0035	0.0035A (1-2113)	370H	4.40 / 0.0210
Layer - 13	0.0006		1/2oz P/G	
	0.0048	1080 106	370H	4.06 / 0.0210
Layer - 14	0.0006		1/2oz Mix	
	0.0060	0.0060A (1-2113/1-1080)	370H	4.33 / 0.0210
Layer - 15	0.0025		2oz P/G	
	0.0039	106 106	370H	3.95 / 0.0210
Layer - 16	0.0017		1/4oz Mix (Std Plt)	
	0.0005		Taiyo 4000-BN	4.71 / 0.0330

Materials: Isola 370H High-Tg FR4



Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0800	0.0080	0.0080	0.0788
Incl. Mask over Laminate	0.0766	0.0077	0.0077	0.0754
Incl. Plating	0.0790	0.0079	0.0079	0.0778
After Lamination	0.0762	0.0038	0.0038	0.0750
Over Laminate	0.0756	0.0076	0.0076	0.0744



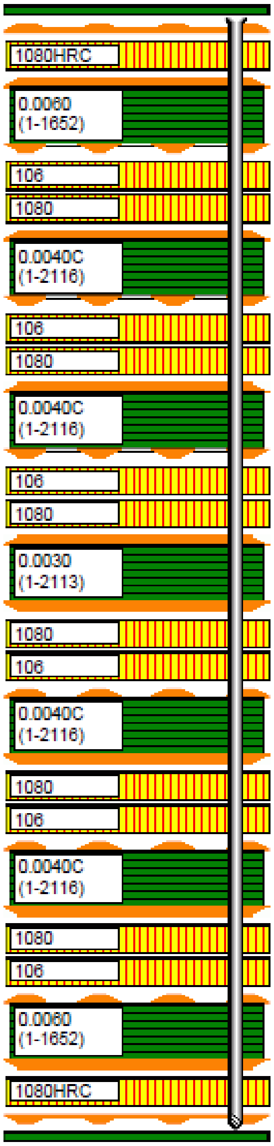
Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1 Surface MS	L1	0.0050	0.0060	-	-	50	5	51.11
	-	-	-	-	L2			
2 EC Microstrip	L1	0.00440	0.0052	0.0105	-	90	9	90.68
	-	0.00440	0.0052	-	L2			
3 EC Microstrip	L1	0.00380	0.0048	0.0120	-	100	10	99.26
	-	0.00380	0.0048	-	L2			
4 Stripline	L3	0.00450	0.0045	-	L2	50	5	50.37
	-	-	-	-	L4			
5 EC Stripline	L3	0.0050	0.0050	0.0120	L2	90	9	90.45
	-	0.0050	0.0050	-	L4			
6 Stripline	L5	0.0040	0.0033	-	L4	50	5	48.65
	-	-	-	-	L6			
7 Stripline	L7	0.00330	0.0033	-	L6	50	5	48.96
	-	-	-	-	L8			
8 Stripline	L10	0.00330	0.0033	-	L9	50	5	48.96
	-	-	-	-	L11			
9 Stripline	L12	0.0040	0.0033	-	L11	50	5	48.96
	-	-	-	-	L13			
10 Stripline	L14	0.00450	0.0045	-	L13	50	5	50.71
	-	-	-	-	L15			
11 Surface MS	L16	0.0050	0.0060	-	L15	50	5	51.11
	-	-	-	-	-			
12 EC Microstrip	L16	0.00350	0.0044	0.0105	L15	100	10	99.49
	-	0.00350	0.0044	-	-			
13 EC Microstrip	L1	0.00380	0.0038	0.0120	-			110.77
	-	0.00380	0.0038	-	L2			
14 EC Microstrip	L1	0.0060	0.0060	0.0120	-			87.59
	-	0.0060	0.0060	-	L2			
15 EC Microstrip	L16	0.0060	0.0060	0.0120	L15			87.60
	-	0.0060	0.0060	-	-			

Table 7-3. AM572x PDN Targets and Decoupling Example

Supply Name(10)	**Static PDN Target**	**Dynamic PDN Targets**			**Number of Decoupling Capacitors Per Supply** (1) (2) (3) (4) (5) (6) (9)							
	Max R_{eff} (mΩ) (7)	**Dec Cap Max LL (nH)** (6) (8)	**Max Impedance (mΩ)**	**Frequency of Interest (MHz)**	**100 nF**	**220 nF**	**470 nF**	**1 µF**	**2.2 µF**	**4.7 µF**	**10 µF**	**22 µF**
VDD_CORE	27	2	87	≤50	6	1	1	1	1	1		
VDD_MPU	10	2	57	≤20	12	2	2	3	1	1		1
VDD_DSPEVE	13	2.5	54	≤20	8	1	1	2	1	1	1	
VDD_IVA	48	2	800	≤100	5		1			1		
VDD_GPU	18	2.5	207	≤50	6	1	1	1	1	1		
VDDS_DDR1	10	2.5	200	≤100	8	4		2		2		1
VDDS_DDR2	10	2.5	200	≤100	8	4		2		2		1
CAP_VBBLDO_DSPEVE	N/A	6	N/A	N/A				1				
CAP_VBBLDO_GPU	N/A	6	N/A	N/A				1				
CAP_VBBDLO_IVA	N/A	6	N/A	N/A				1				
CAP_VBBLD0_MPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE2	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE3	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE4	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE5	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSPEVE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSPEVE2	N/A	6	N/A	N/A				1				
CAP_VDDRAM_GPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_IVA	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU2	N/A	6	N/A	N/A								

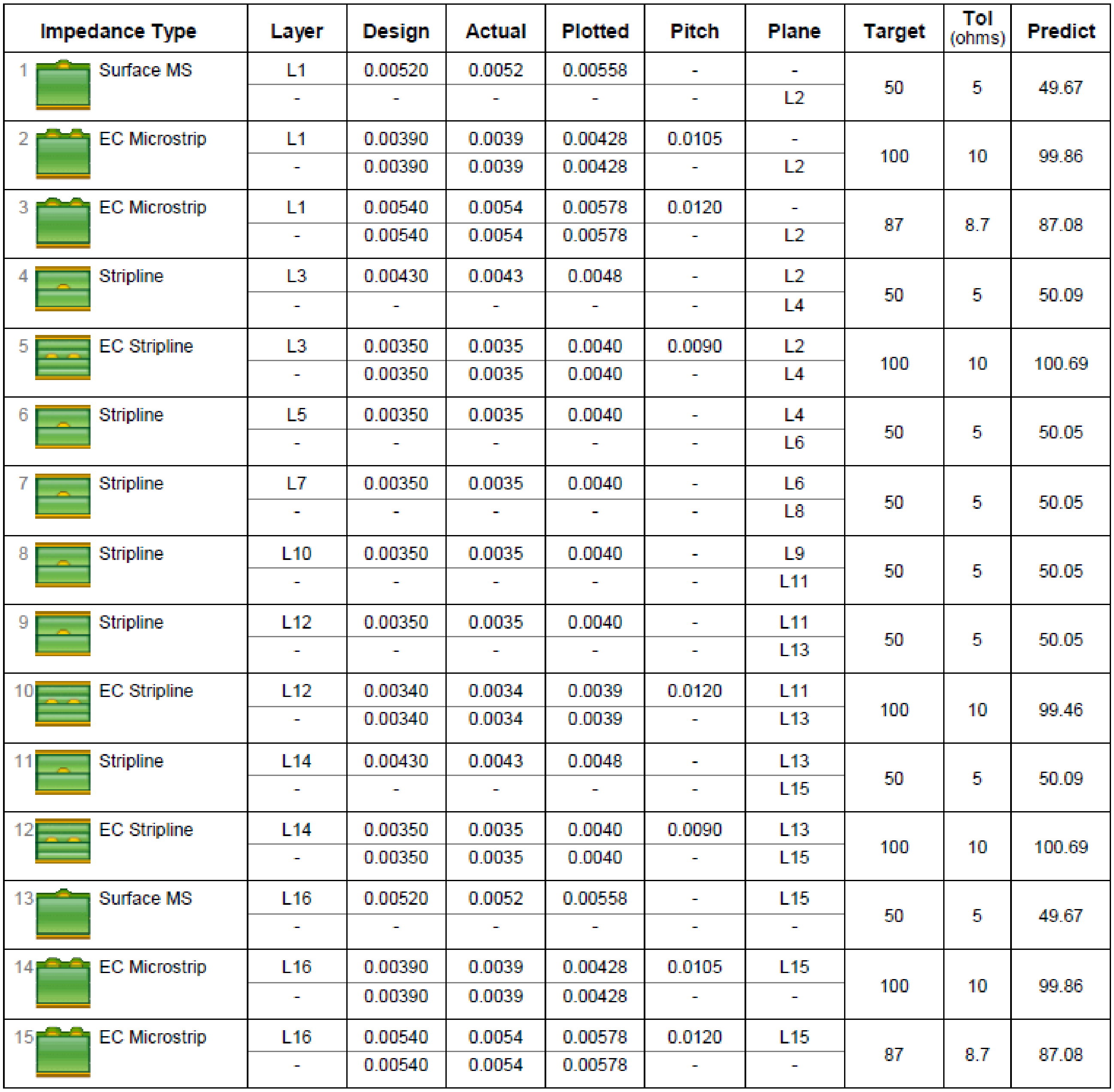
(1) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
(2) ESL must be as low as possible and not exceed 0.5 nH.
(3) The power delivery network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table in the *Specifications* chapter of the device-specific data manual.
(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
(6) High-frequency (30 MHz – 70 MHz) PCB decoupling capacitors.
(7) Maximum R_{eff} from VRM/SMPS/PMIC to processor.
(8) Maximum loop inductance for decoupling capacitor.
(9) Decoupling capacitor counts and values are provided as a baseline recommendation only. TI recommends that all PCB designs be simulated prior fabrication to ensure that the processor PDN requirements are met.
(10) Ganged rails must meet all requirements of each member rail.

7.4 AM574x



Layer	Cust Thickness	Calc Thickness	Primary Stack	Description	Dk / Df
		0.0005		Taiyo 4000 LDI	3.50 / 0.0019
Layer - 1		0.0017		**1/4oz Sig (Std Plt)**	
		0.0033	1080HRC	370H	4.03 / 0.0210
Layer - 2		0.0012		**1oz P/G**	
		0.0060	0.0060 (1-1652)	370H	4.43 / 0.0200
Layer - 3		0.0006		**1/2oz Sig**	
		0.0044	106 1080	370H	4.12 / 0.0210
Layer - 4		0.0006		**1/2oz P/G**	
		0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 5		0.0006		**1/2oz Sig**	
		0.0044	106 1080	370H	4.12 / 0.0210
Layer - 6		0.0006		**1/2oz P/G**	
		0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 7		0.0006		**1/2oz Sig**	
		0.0044	106 1080	370H	4.12 / 0.0210
Layer - 8		0.0006		**1/2oz P/G**	
		0.0030	0.0030 (1-2113)	370H	4.57 / 0.0190
Layer - 9		0.0006		**1/2oz P/G**	
		0.0044	1080 106	370H	4.12 / 0.0210
Layer - 10		0.0006		**1/2oz Sig**	
		0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 11		0.0006		**1/2oz P/G**	
		0.0044	1080 106	370H	4.12 / 0.0210
Layer - 12		0.0006		**1/2oz Sig**	
		0.0041	0.0040C (1-2116)	370H	4.54 / 0.0190
Layer - 13		0.0006		**1/2oz P/G**	
		0.0044	1080 106	370H	4.12 / 0.0210
Layer - 14		0.0006		**1/2oz Sig**	
		0.0060	0.0060 (1-1652)	370H	4.43 / 0.0200
Layer - 15		0.0012		**1oz P/G**	
		0.0033	1080HRC	370H	4.03 / 0.0210
Layer - 16		0.0017		**1/4oz Sig (Std Plt)**	
		0.0005		Taiyo 4000 LDI	3.50 / 0.0019

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0800	0.0080	0.0080	0.0784
Incl. Mask over Laminate	0.0766	0.0077	0.0077	0.0750
Incl. Plating	0.0790	0.0079	0.0079	0.0774
After Lamination	0.0762	0.0038	0.0038	0.0746



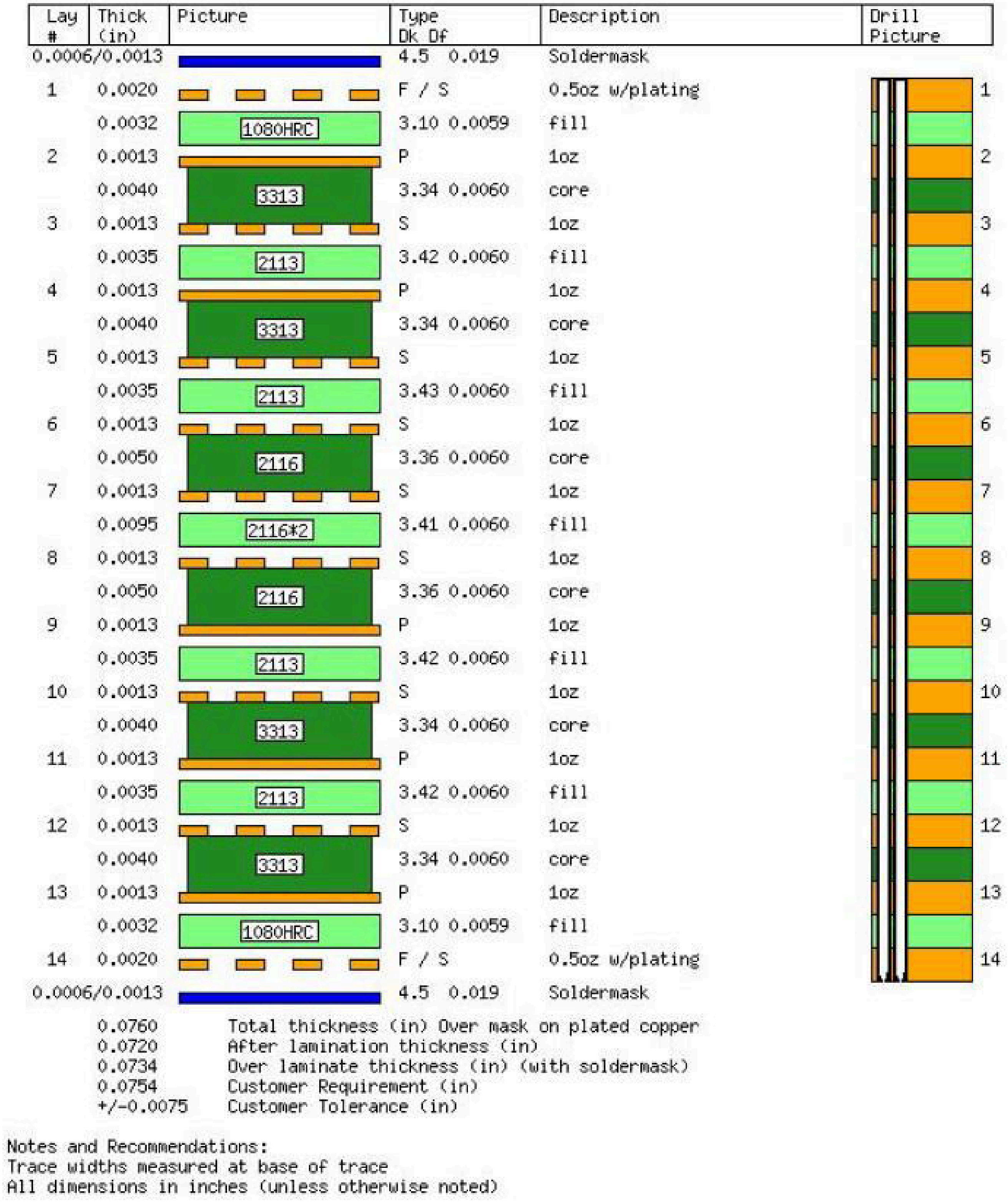
Impedance Type	Layer	Design	Actual	Plotted	Pitch	Plane	Target	Tol (ohms)	Predict
1 Surface MS	L1	0.00520	0.0052	0.00558	-	-	50	5	49.67
	-	-	-	-	-	L2			
2 EC Microstrip	L1	0.00390	0.0039	0.00428	0.0105	-	100	10	99.86
	-	0.00390	0.0039	0.00428	-	L2			
3 EC Microstrip	L1	0.00540	0.0054	0.00578	0.0120	-	87	8.7	87.08
	-	0.00540	0.0054	0.00578	-	L2			
4 Stripline	L3	0.00430	0.0043	0.0048	-	L2	50	5	50.09
	-	-	-	-	-	L4			
5 EC Stripline	L3	0.00350	0.0035	0.0040	0.0090	L2	100	10	100.69
	-	0.00350	0.0035	0.0040	-	L4			
6 Stripline	L5	0.00350	0.0035	0.0040	-	L4	50	5	50.05
	-	-	-	-	-	L6			
7 Stripline	L7	0.00350	0.0035	0.0040	-	L6	50	5	50.05
	-	-	-	-	-	L8			
8 Stripline	L10	0.00350	0.0035	0.0040	-	L9	50	5	50.05
	-	-	-	-	-	L11			
9 Stripline	L12	0.00350	0.0035	0.0040	-	L11	50	5	50.05
	-	-	-	-	-	L13			
10 EC Stripline	L12	0.00340	0.0034	0.0039	0.0120	L11	100	10	99.46
	-	0.00340	0.0034	0.0039	-	L13			
11 Stripline	L14	0.00430	0.0043	0.0048	-	L13	50	5	50.09
	-	-	-	-	-	L15			
12 EC Stripline	L14	0.00350	0.0035	0.0040	0.0090	L13	100	10	100.69
	-	0.00350	0.0035	0.0040	-	L15			
13 Surface MS	L16	0.00520	0.0052	0.00558	-	L15	50	5	49.67
	-	-	-	-	-	-			
14 EC Microstrip	L16	0.00390	0.0039	0.00428	0.0105	L15	100	10	99.86
	-	0.00390	0.0039	0.00428	-	-			
15 EC Microstrip	L16	0.00540	0.0054	0.00578	0.0120	L15	87	8.7	87.08
	-	0.00540	0.0054	0.00578	-	-			

Table 7-4. AM574x PDN Targets and Decoupling Example

	Static PDN Target	Dynamic PDN Targets			Number of Decoupling Capacitors Per Supply (1) (2) (3) (4) (5) (9)							
Supply Name(10)	Max R_{eff} (mΩ) (7)	Dec Cap Max LL (nH) (6) (8)	Max Impedance (mΩ)	Frequency of Interest (MHz)	100 nF	220 nF	470 nF	1 µF	2.2 µF	4.7 µF	10 µF	22 µF
VDD_MPU	18	2	57	≤20	2		4	5			2	
VDD_DSPEVE	22	1.6	40	≤30	2		4	5			2	
VDD_CORE	32	1.6	43	≤30			5	4			1	
VDD_GPU	22	2.1	48	≤30	2		4	3			1	
VDD_IVA	48	2.1	179	≤30	2		2	2			1	
VDDS_DDR1	18	1.5	130	≤100			8	1			1	
VDDS_DDR2	18	1.5	130	≤100			8	1			1	
CAP_VBBLDO_DSPEVE	N/A	6	N/A	N/A				1				
CAP_VBBLDO_GPU	N/A	6	N/A	N/A				1				
CAP_VBBDLO_IVA	N/A	6	N/A	N/A				1				
CAP_VBBLD0_MPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE2	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE3	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE4	N/A	6	N/A	N/A				1				
CAP_VDDRAM_CORE5	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSPEVE1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_DSPEVE2	N/A	6	N/A	N/A				1				
CAP_VDDRAM_GPU	N/A	6	N/A	N/A				1				
CAP_VDDRAM_IVA	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU1	N/A	6	N/A	N/A				1				
CAP_VDDRAM_MPU2	N/A	6	N/A	N/A				1				

(1) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
(2) ESL must be as low as possible and not exceed 0.5 nH.
(3) The power delivery network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table in the *Specifications* chapter of the device-specific data manual.
(4) The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
(5) Assuming that the external SMPS (power IC) feedback sense is taken close to processor power balls.
(6) High-frequency (30 MHz – 70 MHz) PCB decoupling capacitors.
(7) Maximum R_{eff} from SMPS/PMIC to processor.
(8) Maximum loop inductance for decoupling capacitor.
(9) Decoupling capacitor counts and values are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PCB designs be simulated prior fabrication to ensure that the processor PDN requirements are met.
(10) Ganged rails must meet all requirements of each member rail.

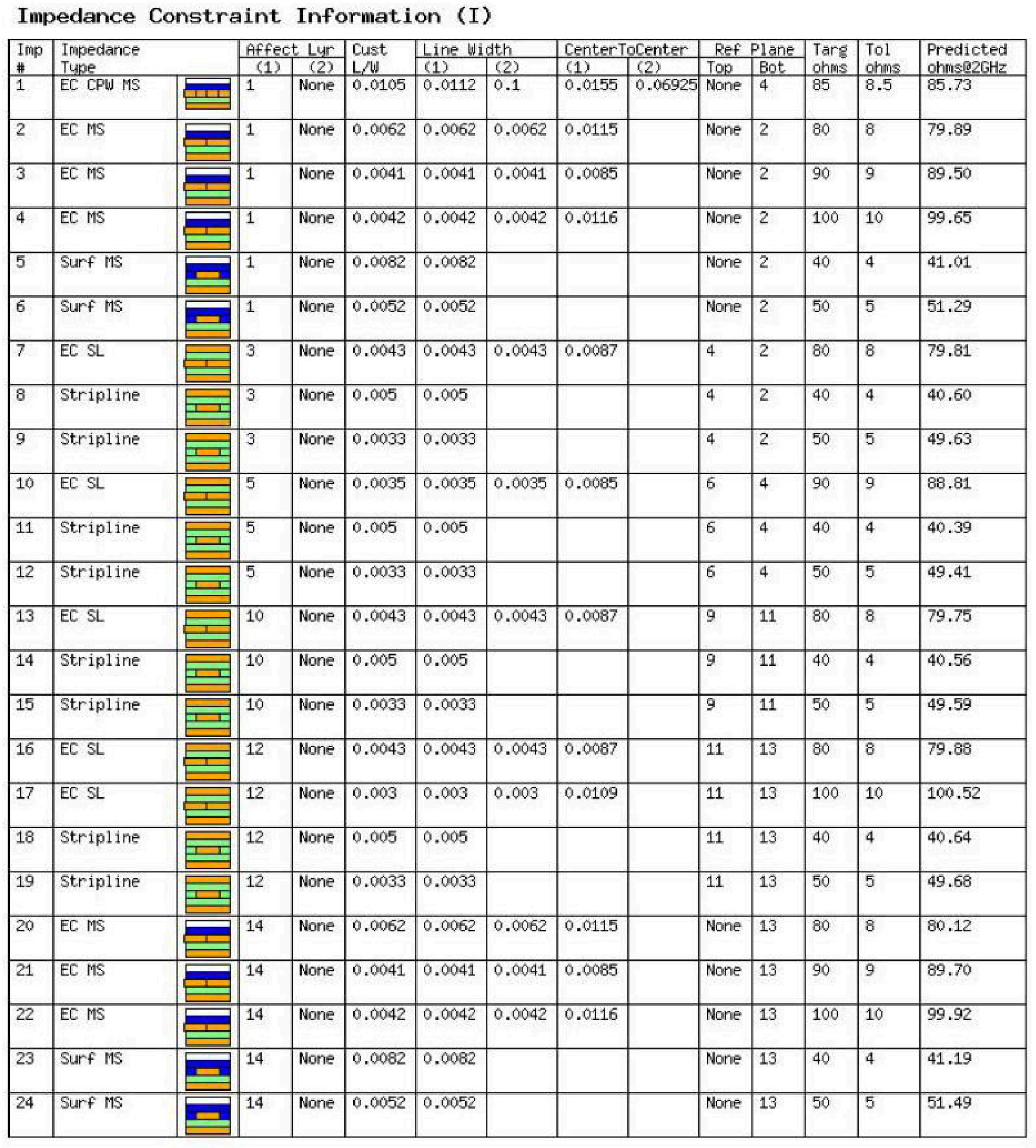
7.5 AM65xx/DRA80xM



Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
0.0006/0.0013			4.5 0.019	Soldermask	
1	0.0020		F / S	0.5oz w/plating	1
	0.0032	1080HRC	3.10 0.0059	fill	
2	0.0013		P	1oz	2
	0.0040	3313	3.34 0.0060	core	
3	0.0013		S	1oz	3
	0.0035	2113	3.42 0.0060	fill	
4	0.0013		P	1oz	4
	0.0040	3313	3.34 0.0060	core	
5	0.0013		S	1oz	5
	0.0035	2113	3.43 0.0060	fill	
6	0.0013		S	1oz	6
	0.0050	2116	3.36 0.0060	core	
7	0.0013		S	1oz	7
	0.0095	2116*2	3.41 0.0060	fill	
8	0.0013		S	1oz	8
	0.0050	2116	3.36 0.0060	core	
9	0.0013		P	1oz	9
	0.0035	2113	3.42 0.0060	fill	
10	0.0013		S	1oz	10
	0.0040	3313	3.34 0.0060	core	
11	0.0013		P	1oz	11
	0.0035	2113	3.42 0.0060	fill	
12	0.0013		S	1oz	12
	0.0040	3313	3.34 0.0060	core	
13	0.0013		P	1oz	13
	0.0032	1080HRC	3.10 0.0059	fill	
14	0.0020		F / S	0.5oz w/plating	14
0.0006/0.0013			4.5 0.019	Soldermask	

0.0760	Total thickness (in) Over mask on plated copper
0.0720	After lamination thickness (in)
0.0734	Over laminate thickness (in) (with soldermask)
0.0754	Customer Requirement (in)
+/-0.0075	Customer Tolerance (in)

Notes and Recommendations:
Trace widths measured at base of trace
All dimensions in inches (unless otherwise noted)



Impedance Constraint Information (I)

Imp #	Impedance Type	Affect Lyr		Cust L/W	Line Width		CenterToCenter		Ref Plane		Targ ohms	Tol ohms	Predicted ohms@2GHz
		(1)	(2)		(1)	(2)	(1)	(2)	Top	Bot			
1	EC CPW MS	1	None	0.0105	0.0112	0.1	0.0155	0.06925	None	4	85	8.5	85.73
2	EC MS	1	None	0.0062	0.0062	0.0062	0.0115		None	2	80	8	79.89
3	EC MS	1	None	0.0041	0.0041	0.0041	0.0085		None	2	90	9	89.50
4	EC MS	1	None	0.0042	0.0042	0.0042	0.0116		None	2	100	10	99.65
5	Surf MS	1	None	0.0082	0.0082				None	2	40	4	41.01
6	Surf MS	1	None	0.0052	0.0052				None	2	50	5	51.29
7	EC SL	3	None	0.0043	0.0043	0.0043	0.0087		4	2	80	8	79.81
8	Stripline	3	None	0.005	0.005				4	2	40	4	40.60
9	Stripline	3	None	0.0033	0.0033				4	2	50	5	49.63
10	EC SL	5	None	0.0035	0.0035	0.0035	0.0085		6	4	90	9	88.81
11	Stripline	5	None	0.005	0.005				6	4	40	4	40.39
12	Stripline	5	None	0.0033	0.0033				6	4	50	5	49.41
13	EC SL	10	None	0.0043	0.0043	0.0043	0.0087		9	11	80	8	79.75
14	Stripline	10	None	0.005	0.005				9	11	40	4	40.56
15	Stripline	10	None	0.0033	0.0033				9	11	50	5	49.59
16	EC SL	12	None	0.0043	0.0043	0.0043	0.0087		11	13	80	8	79.88
17	EC SL	12	None	0.003	0.003	0.003	0.0109		11	13	100	10	100.52
18	Stripline	12	None	0.005	0.005				11	13	40	4	40.64
19	Stripline	12	None	0.0033	0.0033				11	13	50	5	49.68
20	EC MS	14	None	0.0062	0.0062	0.0062	0.0115		None	13	80	8	80.12
21	EC MS	14	None	0.0041	0.0041	0.0041	0.0085		None	13	90	9	89.70
22	EC MS	14	None	0.0042	0.0042	0.0042	0.0116		None	13	100	10	99.92
23	Surf MS	14	None	0.0082	0.0082				None	13	40	4	41.19
24	Surf MS	14	None	0.0052	0.0052				None	13	50	5	51.49

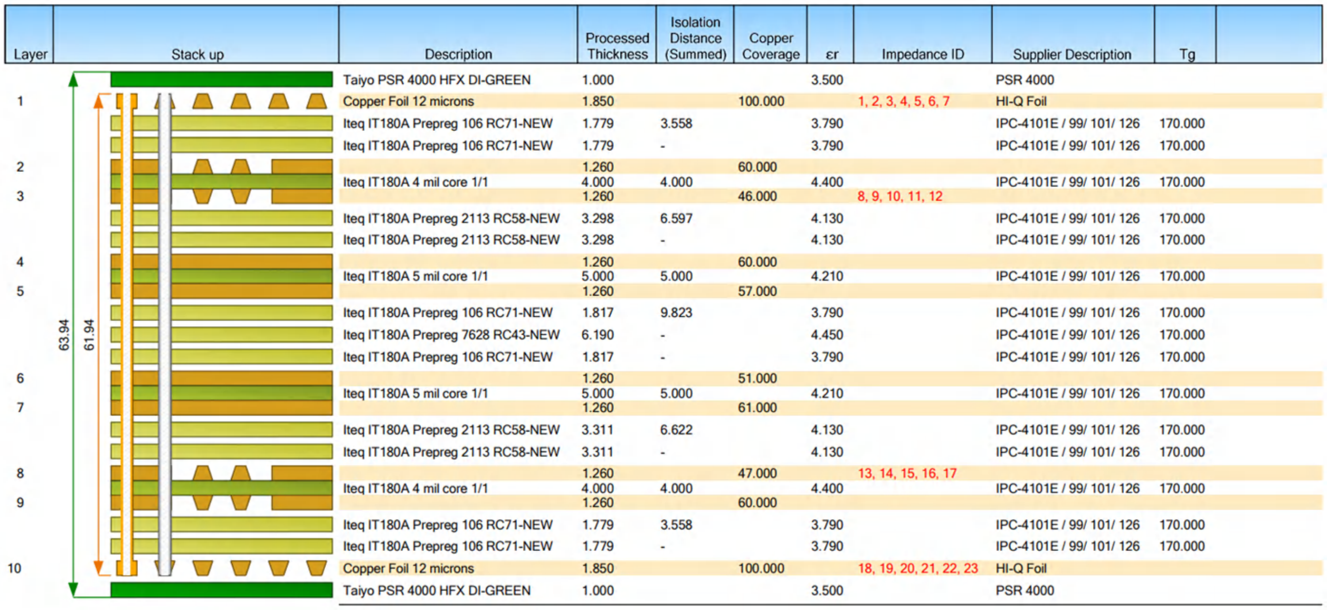
Trace widths measured at base of trace
All dimensions in inches (unless otherwise noted)

Table 7-5. AM65xx/DRA80xM PDN Targets and Decoupling Example

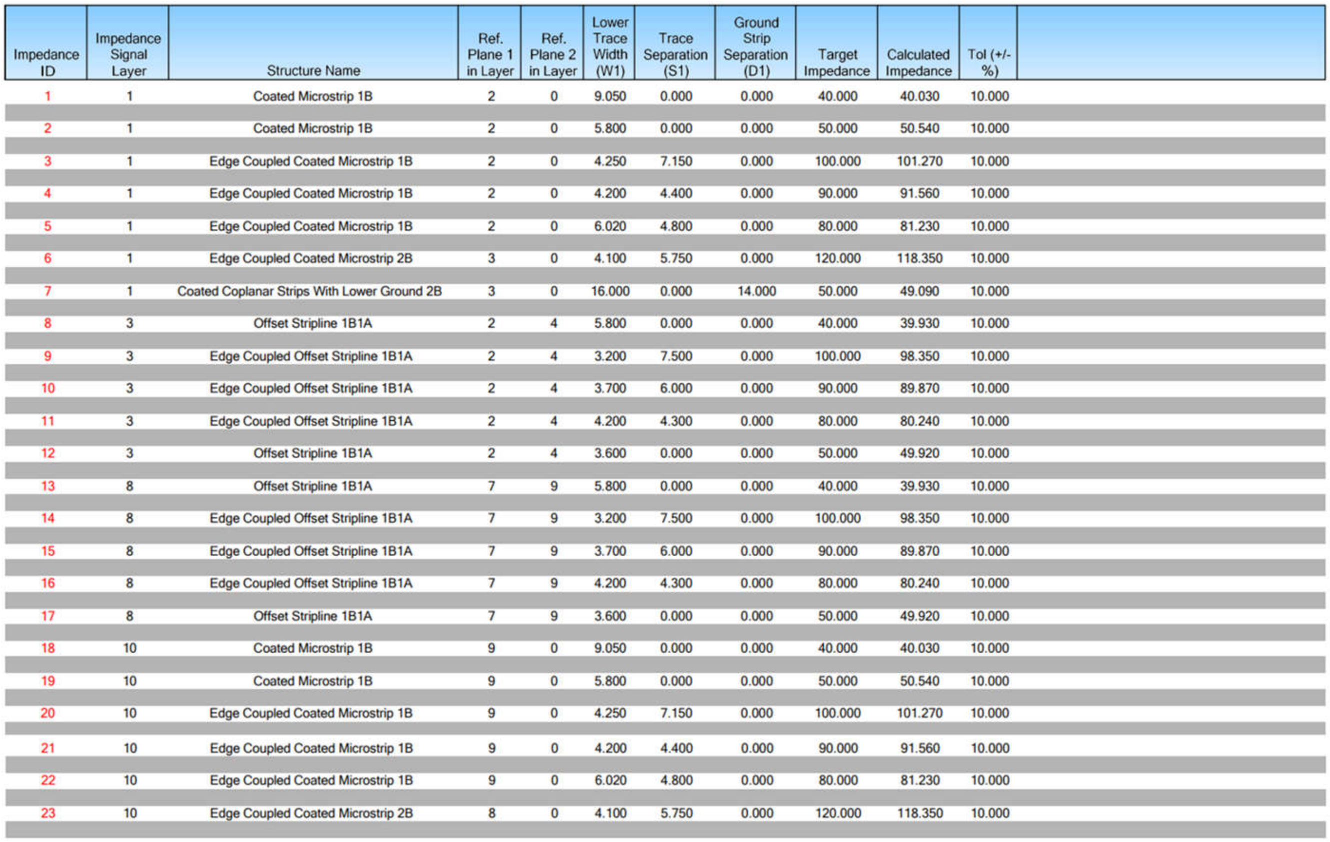
Supply Name (1)	**Frequency of Interest (MHz)**	**Number of Decoupling Capacitors Per Supply** (2) (3) (4)				
		0.01 µF	**0.1 µF**	**1 µF**	**2.2 µF**	**10 µF**
VDD_CORE	≤25		23	12		4
VDD_MPU0 VDD_MPU1	≤25		11	4		4
VDD_MCU	≤25		3	1		2
VDD_DLL_MMC0 VDD_DLL_MMC1	≤25		2			
VDD_WKUP0 VDD_WKUP1	≤25		4			
CAP_VDDAR_WKUP	N/A			1		
CAP_VDDAR_MPU1_1	N/A			1		
CAP_VDDAR_MPU1_0	N/A			1		
CAP_VDDAR_MPU0_1	N/A			1		
CAP_VDDAR_MPU0_0	N/A			1		
CAP_VDDAR_MCU	N/A			1		
CAP_VDDAR_CORE4	N/A			1		
CAP_VDDAR_CORE3	N/A			1		
CAP_VDDAR_CORE2	N/A			1		
CAP_VDDAR_CORE1	N/A			1		
CAP_VDDAR_CORE0	N/A			1		
CAP_VDDSHV_SDIO CAP_VDDA_1P8_SDIO CAP_VDDA_1P8_IOLDO1 CAP_VDDA_1P8_IOLDO0	N/A	Use-case dependent. Refer to the device-specific data sheet.				
CAP_VDDA_1P8_IOLDO_WKUP	N/A				1	
CAP_VDD_WKUP	N/A			1		

(1) Ganged rails must meet all requirements of each member rail.
(2) The decoupling capacitor counts and values presented here are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PCB designs be simulated prior to fabrication to ensure that all processor PDN requirements are met.
(3) For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data sheet.
(4) ESL must be as low as possible and not exceed 0.5 nH.

7.6 AM62xx



Layer	Stack up	Description	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID	Supplier Description	Tg	
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500		PSR 4000		
1		Copper Foil 12 microns	1.850		100.000		1, 2, 3, 4, 5, 6, 7	HI-Q Foil		
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790		IPC-4101E / 99/ 101/ 126	170.000	
2			1.260		60.000					
		Iteq IT180A 4 mil core 1/1	4.000	4.000		4.400		IPC-4101E / 99/ 101/ 126	170.000	
3			1.260		46.000		8, 9, 10, 11, 12			
		Iteq IT180A Prepreg 2113 RC58-NEW	3.298	6.597		4.130		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 2113 RC58-NEW	3.298	-		4.130		IPC-4101E / 99/ 101/ 126	170.000	
4			1.260		60.000					
		Iteq IT180A 5 mil core 1/1	5.000	5.000		4.210		IPC-4101E / 99/ 101/ 126	170.000	
5			1.260		57.000					
		Iteq IT180A Prepreg 106 RC71-NEW	1.817	9.823		3.790		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 7628 RC43-NEW	6.190	-		4.450		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 106 RC71-NEW	1.817	-		3.790		IPC-4101E / 99/ 101/ 126	170.000	
6			1.260		51.000					
		Iteq IT180A 5 mil core 1/1	5.000	5.000		4.210		IPC-4101E / 99/ 101/ 126	170.000	
7			1.260		61.000					
		Iteq IT180A Prepreg 2113 RC58-NEW	3.311	6.622		4.130		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 2113 RC58-NEW	3.311	-		4.130		IPC-4101E / 99/ 101/ 126	170.000	
8			1.260		47.000		13, 14, 15, 16, 17			
		Iteq IT180A 4 mil core 1/1	4.000	4.000		4.400		IPC-4101E / 99/ 101/ 126	170.000	
9			1.260		60.000					
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	3.558		3.790		IPC-4101E / 99/ 101/ 126	170.000	
		Iteq IT180A Prepreg 106 RC71-NEW	1.779	-		3.790		IPC-4101E / 99/ 101/ 126	170.000	
10		Copper Foil 12 microns	1.850		100.000		18, 19, 20, 21, 22, 23	HI-Q Foil		
		Taiyo PSR 4000 HFX DI-GREEN	1.000			3.500		PSR 4000		



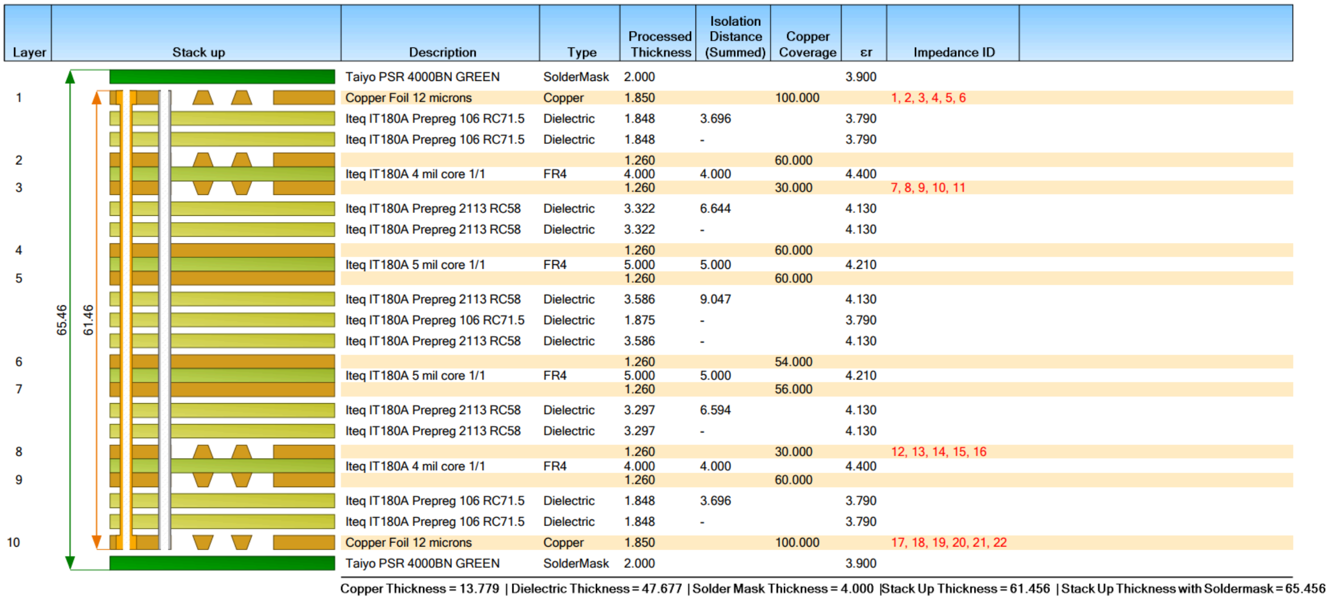
Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Target Impedance	Calculated Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	9.050	0.000	0.000	40.000	40.030	10.000
2	1	Coated Microstrip 1B	2	0	5.800	0.000	0.000	50.000	50.540	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	4.250	7.150	0.000	100.000	101.270	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	4.400	0.000	90.000	91.560	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	6.020	4.800	0.000	80.000	81.230	10.000
6	1	Edge Coupled Coated Microstrip 2B	3	0	4.100	5.750	0.000	120.000	118.350	10.000
7	1	Coated Coplanar Strips With Lower Ground 2B	3	0	16.000	0.000	14.000	50.000	49.090	10.000
8	3	Offset Stripline 1B1A	2	4	5.800	0.000	0.000	40.000	39.930	10.000
9	3	Edge Coupled Offset Stripline 1B1A	2	4	3.200	7.500	0.000	100.000	98.350	10.000
10	3	Edge Coupled Offset Stripline 1B1A	2	4	3.700	6.000	0.000	90.000	89.870	10.000
11	3	Edge Coupled Offset Stripline 1B1A	2	4	4.200	4.300	0.000	80.000	80.240	10.000
12	3	Offset Stripline 1B1A	2	4	3.600	0.000	0.000	50.000	49.920	10.000
13	8	Offset Stripline 1B1A	7	9	5.800	0.000	0.000	40.000	39.930	10.000
14	8	Edge Coupled Offset Stripline 1B1A	7	9	3.200	7.500	0.000	100.000	98.350	10.000
15	8	Edge Coupled Offset Stripline 1B1A	7	9	3.700	6.000	0.000	90.000	89.870	10.000
16	8	Edge Coupled Offset Stripline 1B1A	7	9	4.200	4.300	0.000	80.000	80.240	10.000
17	8	Offset Stripline 1B1A	7	9	3.600	0.000	0.000	50.000	49.920	10.000
18	10	Coated Microstrip 1B	9	0	9.050	0.000	0.000	40.000	40.030	10.000
19	10	Coated Microstrip 1B	9	0	5.800	0.000	0.000	50.000	50.540	10.000
20	10	Edge Coupled Coated Microstrip 1B	9	0	4.250	7.150	0.000	100.000	101.270	10.000
21	10	Edge Coupled Coated Microstrip 1B	9	0	4.200	4.400	0.000	90.000	91.560	10.000
22	10	Edge Coupled Coated Microstrip 1B	9	0	6.020	4.800	0.000	80.000	81.230	10.000
23	10	Edge Coupled Coated Microstrip 2B	8	0	4.100	5.750	0.000	120.000	118.350	10.000

Table 7-6. AM62xx PDN Targets and Decoupling Example

	Static PDN Target	Dynamic PDN Targets			Number of Decoupling Capacitors Per Supply (1) (2)(3) (4) (5) (6) (9)			
Supply Name (10) (11)	**Max R_{eff} (mΩ) (7)**	**Frequency of Interest (MHz)**	**Dec. Cap. Max LL (nH) (6) (8)**	**Z_{TARGET} (mΩ)**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**
VDD_CORE	23	≤1	1.5	23	17	1	1	1
		1-20		31				
		20-50		35				
VDDS_DDR	For more information, see AM62x DDR Board Design and Layout Guidelines.							

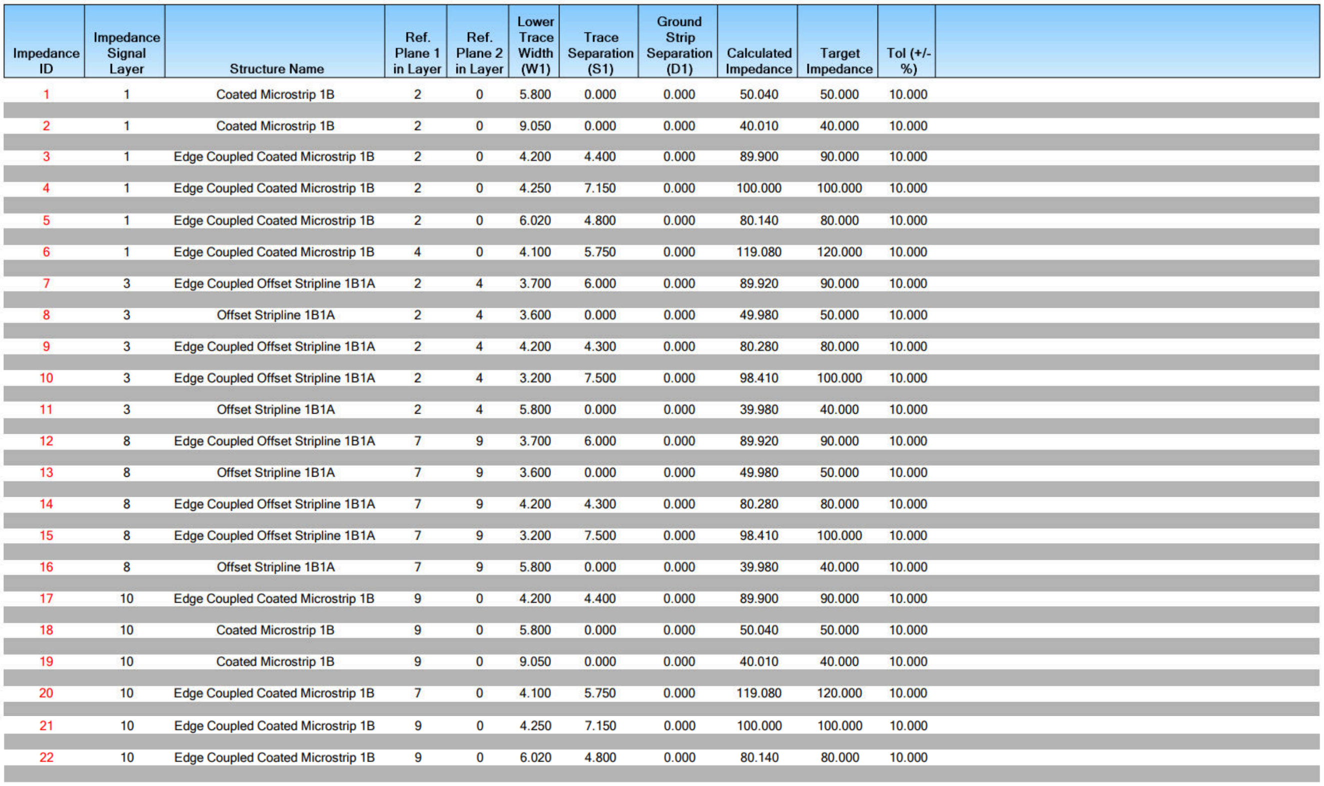
1. For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
2. Loop ESL (excluding the intrinsic decap ESL) from the capacitor pads to the SoC BGA must be as low as possible and not exceed 1.5 nH.
3. The Power Delivery Network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table of the *Specifications* chapter of the device-specific processor data manual.
4. The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
5. This assumes that the external SMPS (power IC) feedback sense is located very close to processor power balls.
6. High-frequency (30 MHz to 70 MHz) PCB decoupling capacitors.
7. Maximum R_{eff} from VRM/SMPS/PMIC to Processor.
8. Maximum Loop Inductance for decoupling capacitor when placed underneath processor BGA.
9. The decoupling capacitor counts and values presented here are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PCB designs be simulated prior to fabrication to ensure that all processor PDN requirements are met.
10. Ganged rails must meet all requirements of each member rail.
11. Rails not listed in this table are not simulated by TI due to low load transients. For more information, see the device-specific EVM layout for example implementation of these rails.

7.7 AM64xx



Layer	Stack up	Description	Type	Processed Thickness	Isolation Distance (Summed)	Copper Coverage	εr	Impedance ID
		Taiyo PSR 4000BN GREEN	SolderMask	2.000			3.900	
1		Copper Foil 12 microns	Copper	1.850		100.000		1, 2, 3, 4, 5, 6
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.848	3.696		3.790	
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.848	-		3.790	
2				1.260		60.000		
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
3				1.260		30.000		7, 8, 9, 10, 11
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.322	6.644		4.130	
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.322	-		4.130	
4				1.260		60.000		
		Iteq IT180A 5 mil core 1/1	FR4	5.000	5.000		4.210	
5				1.260		60.000		
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.586	9.047		4.130	
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.875	-		3.790	
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.586	-		4.130	
6				1.260		54.000		
		Iteq IT180A 5 mil core 1/1	FR4	5.000	5.000		4.210	
7				1.260		56.000		
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.297	6.594		4.130	
		Iteq IT180A Prepreg 2113 RC58	Dielectric	3.297	-		4.130	
8				1.260		30.000		12, 13, 14, 15, 16
		Iteq IT180A 4 mil core 1/1	FR4	4.000	4.000		4.400	
9				1.260		60.000		
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.848	3.696		3.790	
		Iteq IT180A Prepreg 106 RC71.5	Dielectric	1.848	-		3.790	
10		Copper Foil 12 microns	Copper	1.850		100.000		17, 18, 19, 20, 21, 22
		Taiyo PSR 4000BN GREEN	SolderMask	2.000			3.900	

Copper Thickness = 13.779 | Dielectric Thickness = 47.677 | Solder Mask Thickness = 4.000 |Stack Up Thickness = 61.456 | Stack Up Thickness with Soldermask = 65.456



Impedance ID	Impedance Signal Layer	Structure Name	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	1	Coated Microstrip 1B	2	0	5.800	0.000	0.000	50.040	50.000	10.000
2	1	Coated Microstrip 1B	2	0	9.050	0.000	0.000	40.010	40.000	10.000
3	1	Edge Coupled Coated Microstrip 1B	2	0	4.200	4.400	0.000	89.900	90.000	10.000
4	1	Edge Coupled Coated Microstrip 1B	2	0	4.250	7.150	0.000	100.000	100.000	10.000
5	1	Edge Coupled Coated Microstrip 1B	2	0	6.020	4.800	0.000	80.140	80.000	10.000
6	1	Edge Coupled Coated Microstrip 1B	4	0	4.100	5.750	0.000	119.080	120.000	10.000
7	3	Edge Coupled Offset Stripline 1B1A	2	4	3.700	6.000	0.000	89.920	90.000	10.000
8	3	Offset Stripline 1B1A	2	4	3.600	0.000	0.000	49.980	50.000	10.000
9	3	Edge Coupled Offset Stripline 1B1A	2	4	4.200	4.300	0.000	80.280	80.000	10.000
10	3	Edge Coupled Offset Stripline 1B1A	2	4	3.200	7.500	0.000	98.410	100.000	10.000
11	3	Offset Stripline 1B1A	2	4	5.800	0.000	0.000	39.980	40.000	10.000
12	8	Edge Coupled Offset Stripline 1B1A	7	9	3.700	6.000	0.000	89.920	90.000	10.000
13	8	Offset Stripline 1B1A	7	9	3.600	0.000	0.000	49.980	50.000	10.000
14	8	Edge Coupled Offset Stripline 1B1A	7	9	4.200	4.300	0.000	80.280	80.000	10.000
15	8	Edge Coupled Offset Stripline 1B1A	7	9	3.200	7.500	0.000	98.410	100.000	10.000
16	8	Offset Stripline 1B1A	7	9	5.800	0.000	0.000	39.980	40.000	10.000
17	10	Edge Coupled Coated Microstrip 1B	9	0	4.200	4.400	0.000	89.900	90.000	10.000
18	10	Coated Microstrip 1B	9	0	5.800	0.000	0.000	50.040	50.000	10.000
19	10	Coated Microstrip 1B	9	0	9.050	0.000	0.000	40.010	40.000	10.000
20	10	Edge Coupled Coated Microstrip 1B	7	0	4.100	5.750	0.000	119.080	120.000	10.000
21	10	Edge Coupled Coated Microstrip 1B	9	0	4.250	7.150	0.000	100.000	100.000	10.000
22	10	Edge Coupled Coated Microstrip 1B	9	0	6.020	4.800	0.000	80.140	80.000	10.000

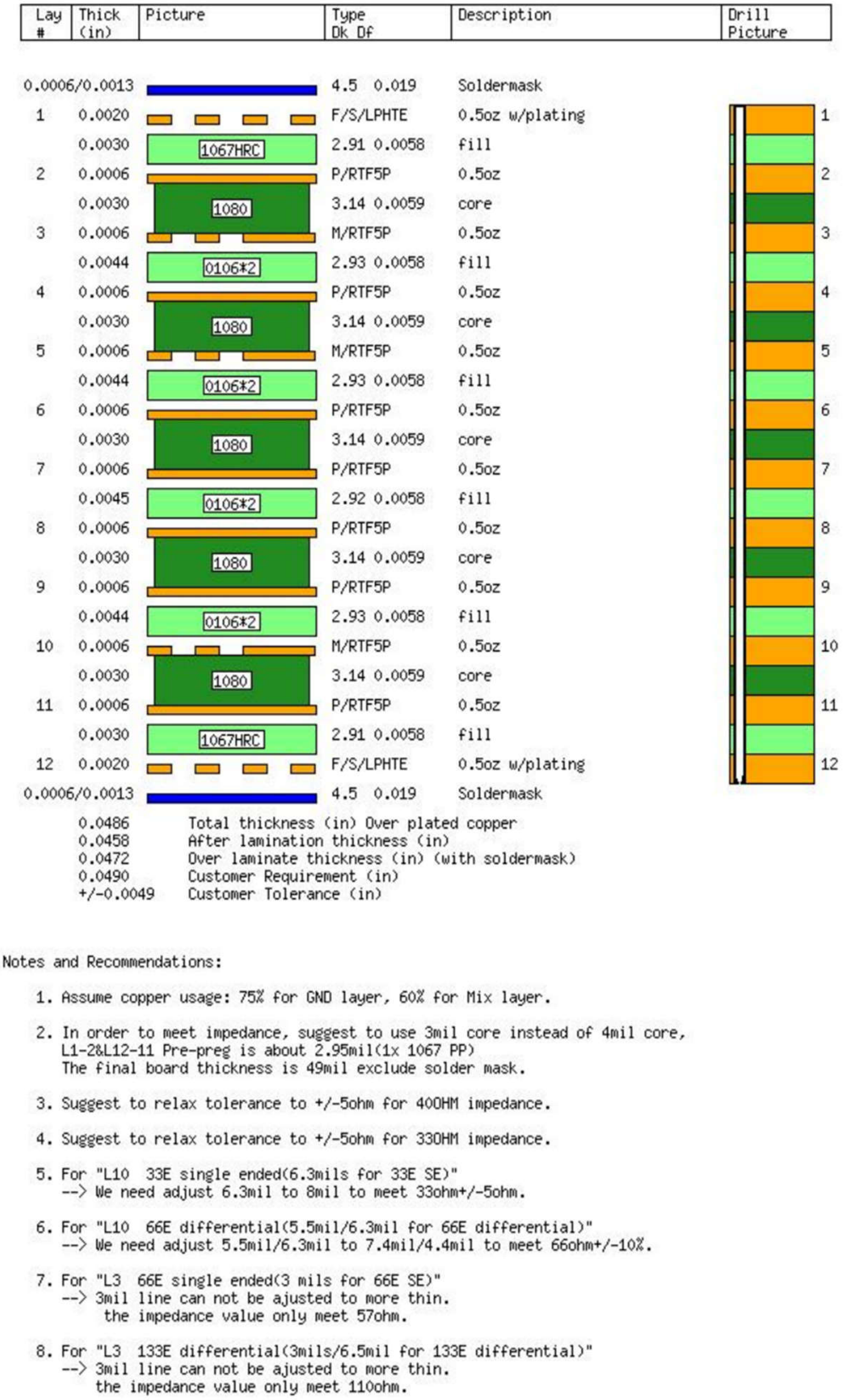
Table 7-7. AM64xx PDN Targets and Decoupling Example

	Static PDN Target	**Dynamic PDN Targets**			**Number of Decoupling Capacitors Per Supply (1) (2)(3) (4) (5) (6) (9)**			
Supply Name (10) (11)	**Max R_{eff} (mΩ) (7)**	**Frequency of Interest (MHz)**	**Dec. Cap. Max LL (nH) (6) (8)**	**Z_{TARGET} (mΩ)**	**0.1 µF**	**1 µF**	**4.7 µF**	**10 µF**
VDD_CORE	23	≤1	1.5	10	11	1	1	1
		1-20		34				
		20-50		35				
VDDS_DDR	For more information, see *AM64x/AM243x DDR Board Design and Layout Guidelines*.							

1. For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
2. Loop ESL (excluding the intrinsic decap ESL) from the capacitor pads to the SoC BGA must be as low as possible and not exceed 1.5 nH.
3. The Power Delivery Network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table of the *Specifications* chapter of the device-specific processor data manual.
4. The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
5. This assumes that the external SMPS (power IC) feedback sense is located very close to processor power balls.
6. High-frequency (30 MHz to 70 MHz) PCB decoupling capacitors.
7. Maximum R_{eff} from VRM/SMPS/PMIC to Processor.
8. Maximum Loop Inductance for decoupling capacitor when placed underneath processor BGA.
9. The decoupling capacitor counts and values presented here are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PCB designs be simulated prior to fabrication to ensure that all processor PDN requirements are met.
10. Ganged rails must meet all requirements of each member rail.

11. Rails not listed in this table are not simulated by TI due to low load transients. For more information, see the device-specific EVM layout for example implementation of these rails.

7.8 AM62Ax

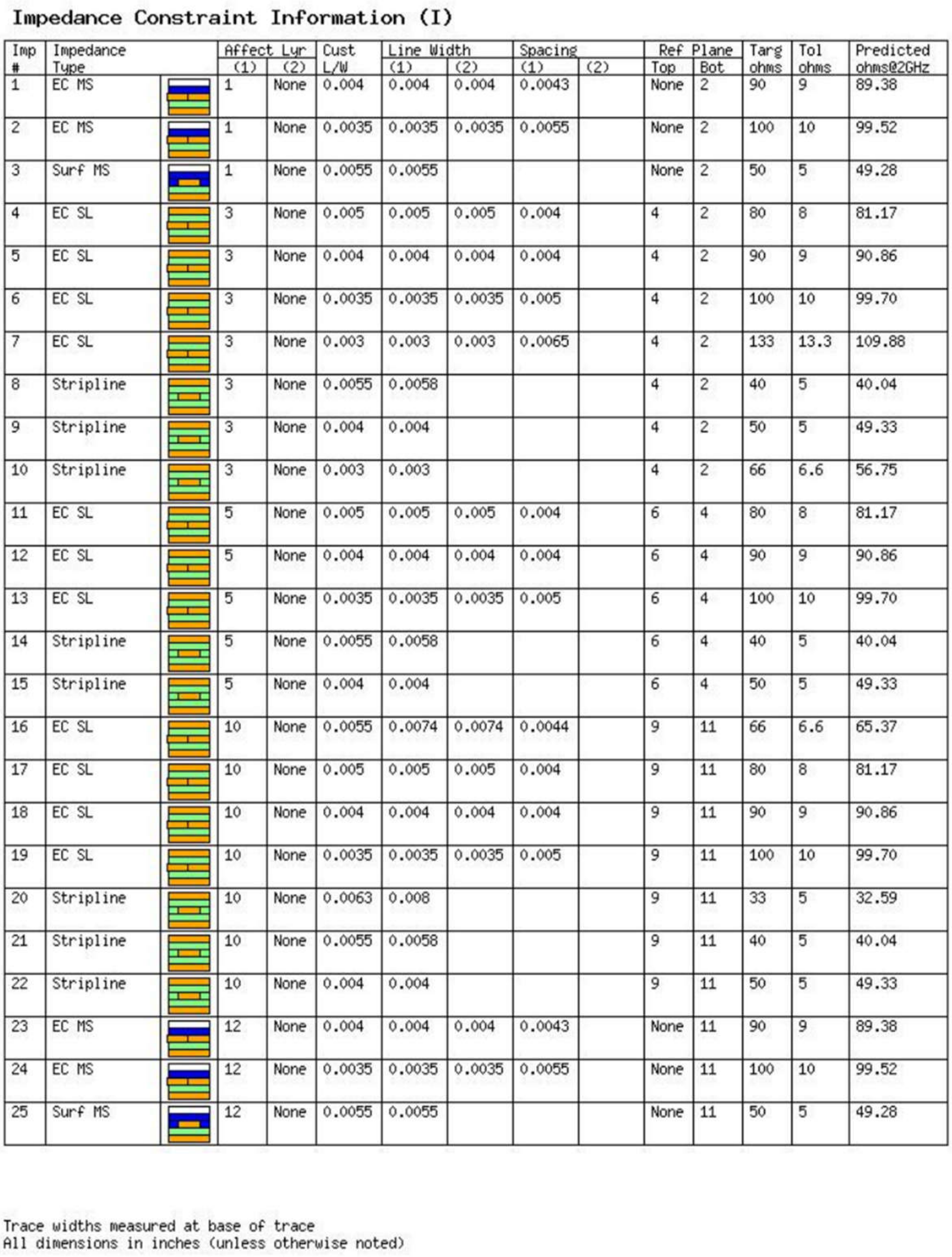


Lay #	Thick (in)	Picture	Type Dk Df	Description	Drill Picture
	0.0006/0.0013		4.5 0.019	Soldermask	
1	0.0020		F/S/LPHTE	0.5oz w/plating	1
	0.0030	1067HRC	2.91 0.0058	fill	
2	0.0006		P/RTF5P	0.5oz	2
	0.0030	1080	3.14 0.0059	core	
3	0.0006		M/RTF5P	0.5oz	3
	0.0044	0106*2	2.93 0.0058	fill	
4	0.0006		P/RTF5P	0.5oz	4
	0.0030	1080	3.14 0.0059	core	
5	0.0006		M/RTF5P	0.5oz	5
	0.0044	0106*2	2.93 0.0058	fill	
6	0.0006		P/RTF5P	0.5oz	6
	0.0030	1080	3.14 0.0059	core	
7	0.0006		P/RTF5P	0.5oz	7
	0.0045	0106*2	2.92 0.0058	fill	
8	0.0006		P/RTF5P	0.5oz	8
	0.0030	1080	3.14 0.0059	core	
9	0.0006		P/RTF5P	0.5oz	9
	0.0044	0106*2	2.93 0.0058	fill	
10	0.0006		M/RTF5P	0.5oz	10
	0.0030	1080	3.14 0.0059	core	
11	0.0006		P/RTF5P	0.5oz	11
	0.0030	1067HRC	2.91 0.0058	fill	
12	0.0020		F/S/LPHTE	0.5oz w/plating	12
	0.0006/0.0013		4.5 0.019	Soldermask	

0.0486	Total thickness (in) Over plated copper
0.0458	After lamination thickness (in)
0.0472	Over laminate thickness (in) (with soldermask)
0.0490	Customer Requirement (in)
+/-0.0049	Customer Tolerance (in)

Notes and Recommendations:

1. Assume copper usage: 75% for GND layer, 60% for Mix layer.
2. In order to meet impedance, suggest to use 3mil core instead of 4mil core,
   L1-2&L12-11 Pre-preg is about 2.95mil(1x 1067 PP)
   The final board thickness is 49mil exclude solder mask.
3. Suggest to relax tolerance to +/-5ohm for 40OHM impedance.
4. Suggest to relax tolerance to +/-5ohm for 33OHM impedance.
5. For "L10 33E single ended(6.3mils for 33E SE)"
   --> We need adjust 6.3mil to 8mil to meet 33ohm+/-5ohm.
6. For "L10 66E differential(5.5mil/6.3mil for 66E differential)"
   --> We need adjust 5.5mil/6.3mil to 7.4mil/4.4mil to meet 66ohm+/-10%.
7. For "L3 66E single ended(3 mils for 66E SE)"
   --> 3mil line can not be ajusted to more thin.
   the impedance value only meet 57ohm.
8. For "L3 133E differential(3mils/6.5mil for 133E differential)"
   --> 3mil line can not be ajusted to more thin.
   the impedance value only meet 110ohm.



Impedance Constraint Information (I)

Imp #	Impedance Type		Affect Lyr (1)	Affect Lyr (2)	Cust L/W	Line Width (1)	Line Width (2)	Spacing (1)	Spacing (2)	Ref Plane Top	Ref Plane Bot	Targ ohms	Tol ohms	Predicted ohms@2GHz
1	EC MS		1	None	0.004	0.004	0.004	0.0043		None	2	90	9	89.38
2	EC MS		1	None	0.0035	0.0035	0.0035	0.0055		None	2	100	10	99.52
3	Surf MS		1	None	0.0055	0.0055				None	2	50	5	49.28
4	EC SL		3	None	0.005	0.005	0.005	0.004		4	2	80	8	81.17
5	EC SL		3	None	0.004	0.004	0.004	0.004		4	2	90	9	90.86
6	EC SL		3	None	0.0035	0.0035	0.0035	0.005		4	2	100	10	99.70
7	EC SL		3	None	0.003	0.003	0.003	0.0065		4	2	133	13.3	109.88
8	Stripline		3	None	0.0055	0.0058				4	2	40	5	40.04
9	Stripline		3	None	0.004	0.004				4	2	50	5	49.33
10	Stripline		3	None	0.003	0.003				4	2	66	6.6	56.75
11	EC SL		5	None	0.005	0.005	0.005	0.004		6	4	80	8	81.17
12	EC SL		5	None	0.004	0.004	0.004	0.004		6	4	90	9	90.86
13	EC SL		5	None	0.0035	0.0035	0.0035	0.005		6	4	100	10	99.70
14	Stripline		5	None	0.0055	0.0058				6	4	40	5	40.04
15	Stripline		5	None	0.004	0.004				6	4	50	5	49.33
16	EC SL		10	None	0.0055	0.0074	0.0074	0.0044		9	11	66	6.6	65.37
17	EC SL		10	None	0.005	0.005	0.005	0.004		9	11	80	8	81.17
18	EC SL		10	None	0.004	0.004	0.004	0.004		9	11	90	9	90.86
19	EC SL		10	None	0.0035	0.0035	0.0035	0.005		9	11	100	10	99.70
20	Stripline		10	None	0.0063	0.008				9	11	33	5	32.59
21	Stripline		10	None	0.0055	0.0058				9	11	40	5	40.04
22	Stripline		10	None	0.004	0.004				9	11	50	5	49.33
23	EC MS		12	None	0.004	0.004	0.004	0.0043		None	11	90	9	89.38
24	EC MS		12	None	0.0035	0.0035	0.0035	0.0055		None	11	100	10	99.52
25	Surf MS		12	None	0.0055	0.0055				None	11	50	5	49.28

Trace widths measured at base of trace
All dimensions in inches (unless otherwise noted)

Table 7-8. AM62Ax PDN Targets and Decoupling Example

	Static PDN Target	Dynamic PDN Targets			Number of Decoupling Capacitors Per Supply (1) (2)(3) (4) (5) (6) (9)		
Supply Name (10) (11)	Max R_{eff} (mΩ) (7)	Frequency of Interest (MHz)	Dec. Cap. Max LL (nH) (6) (8)	Z_{TARGET} (mΩ)	0.1 µF	1 µF	2.2 µF
VDD_CORE	6.8	≤1	1.5	6	4	9	1
		1-20		11			
		20-50		22			

Table 7-8. AM62Ax PDN Targets and Decoupling Example (continued)

Supply Name (10) (11)	Static PDN Target	Dynamic PDN Targets			Number of Decoupling Capacitors Per Supply (1) (2)(3) (4) (5) (6) (9)		
	Max R_{eff} (mΩ) (7)	Frequency of Interest (MHz)	Dec. Cap. Max LL (nH) (6) (8)	Z_{TARGET} (mΩ)	0.1 µF	1 µF	2.2 µF
VDDS_DDR	For more information, see *AM62Ax DDR Board Design and Layout Guidelines*.						

1. For more information on peak-to-peak noise values, see the *Recommended Operating Conditions* table in the device-specific data manual.
2. Loop ESL (excluding the intrinsic decap ESL) from the capacitor pads to the SoC BGA must be as low as possible and not exceed 1.5 nH.
3. The Power Delivery Network (PDN) impedance characteristics are defined versus the device activity (that runs at different frequency) based on the *Recommended Operating Conditions* table of the *Specifications* chapter of the device-specific processor data manual.
4. The static drop requirement drives the maximum acceptable PCB resistance between the PMIC or the external SMPS and the processor power balls.
5. This assumes that the external SMPS (power IC) feedback sense is located very close to processor power balls.
6. High-frequency (30 MHz to 70 MHz) PCB decoupling capacitors.
7. Maximum R_{eff} from VRM/SMPS/PMIC to Processor.
8. Maximum Loop Inductance for decoupling capacitor when placed underneath processor BGA.
9. The decoupling capacitor counts and values presented here are provided as a baseline recommendation only and are based on a specific PCB design. TI recommends that all PCB designs be simulated prior to fabrication to ensure that all processor PDN requirements are met.
10. Ganged rails must meet all requirements of each member rail.
11. Rails not listed in this table are not simulated by TI due to low load transients. For more information, see the device-specific EVM layout for example implementation of these rails.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 1, 2022 to February 29, 2024 (from Revision F (November 2022) to Revision G (February 2024))

Page

- Updated the numbering format for tables, figures and cross-references throughout the document.................. 2
- Updated AM62xx section...28
- Updated Section 7.7...29
- Added Section 7.8..31

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated