User's Guide

Jacinto Processors TDA4AP-Q1/TDA4VP-Q1/TDA4AH-Q1/ TDA4VH-Q1 EVM User's Guide

Texas Instruments

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1 Introduction

The TDA4AP-Q1/TDA4VP-Q1/TDA4AH-Q1/TDA4VH-Q1 EVM is a standalone test, development, and evaluation module which gives developers the basic resources to develop software and evaluate performance of the Jacinto7 processor. The J784S4 is a super-set processor/device available in different configurations targeted for different markets and applications (TDA4AP-Q1, TDA4VP-Q1, TDA4AH-Q1, TDA4VH-Q1). This user's guide describes the hardware, settings, and interfaces of the EVM.

1.1 Inside the Box

The TDA4AP-Q1/TDA4VP-Q1/TDA4AH-Q1/TDA4VH-Q1 EVM kit includes:

- EVM mounted with a J784S4 Super-Set device
- Micro-SD Card
- USB Cable (Type-A to Micro-B) for serial terminal/logging
- Paper Card with Start-up Link/Support Information
- Modular Cable Plug to Plug RJ45 Ethernet cable
- USB 3.1 Cable A Female to C Male
- USB C PLUG TO USB 3.1 A Receptacle Cable
- Cable Assembly DisplayPort Male to DisplayPort Male
- Assembled Power cable with banana jack for bench supply

An EVM power supply is NOT included. For more information on the types of supplies recommended with the EVM, see Section 2.1.

The EVM's orderable part number is: J784S4XG01EVM.

1.2 Key Features and Interfaces

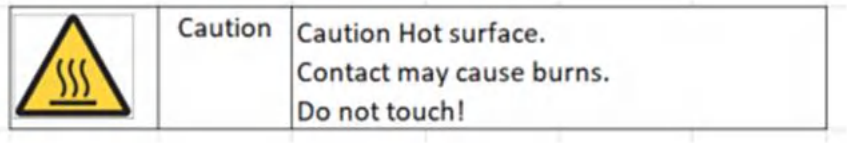
Below are the EVM's key features:

- Processor:
  - Texas Instruments Jacinto J784S4 Super-Set processor
- Optimized Power Management Solution:
  - Dynamic Voltage Scaling
  - Multiple Clock and Power Domains
  - Multiple Low Power/Sleep Modes
- Memory:
  - 32GB LPDDR4 DRAM (4266 MT/s), support inline ECC
  - Two 512Mb Non-Volatile NOR Memories, 1x Octal-SPI and 1x Quad-SPI
  - 1Gb Non-Volatile NAND Memory, Octal-SPI
  - 32GB Non-Volatile eMMC Memory, JEDEC/MMC v5.1 compliant
  - 32GB Non-Volatile UFS Memory, 2Lane, Gear3
  - Multimedia Card (MMC)/Secure Digital Card (Micro SD) Cage, UHS-1
- USB:
  - USB3.1 (Gen 1) Type C Interface, support DFP, DRP, UFP modes
  - USB2.0 Hub to 2x Type A (Host), 1x Pin Header for PCIe WiFi support
  - Two USB2.0 Micro B (for Dual/Quad UART-over-USB Transceiver)
- Display:
  - VESA Display Port (v1.4), supports 4K UHD with MST support
  - VESA Display Port (v1.4), supports 2K QHD
  - Custom CSI2-TX Expansion Interface
- Wired Network:
  - Two Gigabit Ethernet (RJ45 Connector)
  - Six CAN-FD Interfaces
  - Two LIN Interfaces
- Camera:
  - Three CSI2-RX Camera Interfaces (Custom Interface/Dual-QSH connectors)
- Audio:
  - 3.5-mm Stereo Input/Output

- Expansion/Add-on:
  - Two PCIe/Gen3 4L Card Slots (1x with 4Lane support, 1x with 2L support)
  - Serial Ethernet Modules
  - Multiple Pin Headers for ADC, I2C, I3C, and SPI Access
- User Control/Indication:
  - Pushbuttons (Resets, Power Modes, User Defined)
  - LEDs (Power, User Defined, Serial Port)
  - User Configurations (Boot Mode, USB Mode)
  - External or On-board Emulator Support (MIPI-60 w/ adapters to 14-pin or 20-pin CTI)
- REACH and RoHS Compliant
- EMI/EMC Radiation Compliant

1.3 Thermal Compliance

There is elevated heat on the processor/heatsink, use caution particularly at elevated ambient temperatures! Although the processor/heatsink is not a burn hazard, caution should be used when handling the EVM due to increased heat in the area of the heatsink.



1.4 Reach Compliance

In compliance with the Article 33 provision of the EU REACH regulation, we are notifying you that this EVM includes component(s) containing at least one Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are listed in Table 1-1.

Table 1-1. REACH Compliance

Component Manufacturer	Component type	Component part number	SVHC Substance	SVHC CAS (when available)
Tensility	Power Cable	10-02937	Lead	7439-92-1
Littelfuse	Power fuse	015406.3DR	Lead	7439-92-1

1.5 EMC, EMI, and ESD Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). It is recommended this product be used in an ESD controlled environment. This may include a temperature and/or humidity controlled environment to limit the buildup of ESD. It is also recommended to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is to be used in the basic electromagnetic environment, as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

2 User Interfaces

Figure 2-1 and Figure 2-2 identify the key user interfaces on the EVM (top and bottom view).

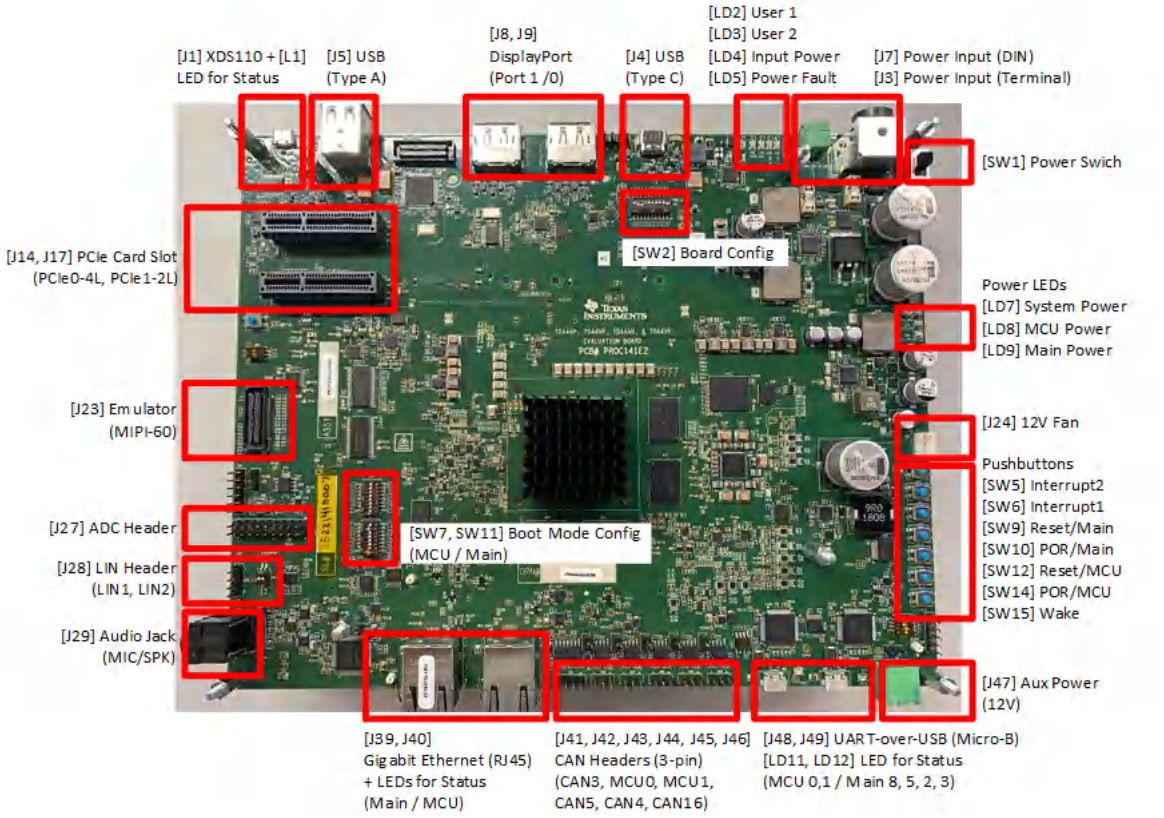


Figure 2-1. User Interfaces (Top)

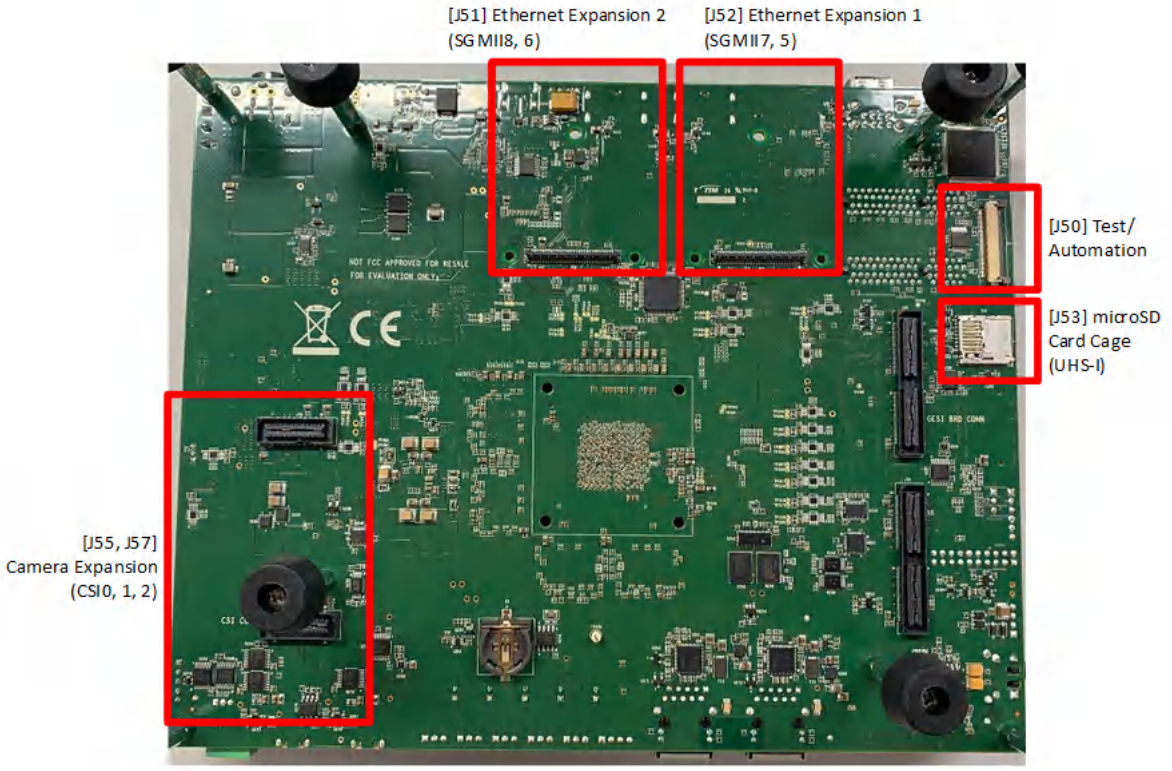


Figure 2-2. User Interfaces (Bottom)

2.1 Power Input

A power supply is not included with the EVM and must be purchased separately.

External Power Supply or Power Accessory Requirements:

- Output Voltage: 24-48 VDC
- Output Power Capacity: 100-160 W (depending on use case and connected peripherals)
- Efficiency Level V

Note

TI recommends using and external power supply or power accessory which complies with the applicable regional safety standards such as (by example) UL, CSA, VDA, CCC, PSE, etc.

2.1.1 Power Input [J7] [J3] with LED for Status [LD4][LD5]

The EVM supports two separate power input connectors [J7] [J3], either of which can be used to power the system. (Note both should not be used as the same time, as connecting power supply outputs together can cause damage to the EVM and/or power supplies.) The input can accept a wide range of voltages (20 to 48 VDC). The exact power required for the EVM is largely dependent on the application and connected peripherals. The recommended supplies are listed in Table 2-1. There are many power supply manufacturers and models available in the market, and it is not possible to test the EVM with every combination.

Table 2-1 lists a few recommended supplies that have been tested with the EVM.

Table 2-1. Recommended External Power Supply

DigiKey Part#	Manufacturer	Manufacturer Part #
SDI120-24-UC-P51	CUI Inc.	SDI120-24-UC-P51
SDI120-48-UC-P51	CUI Inc.	SDI120-48-UC-P51

Connector [J7] is a four pin DIN power input connector. This connector mates with the recommend supplies listed in Table 2-1. Connector [J3] is a two pin power input connector, and is used to power the EVM from bench

power supply(s) or similar equipment. The EVM kit includes a cable assembly for connecting the bench supply (via banana plug) to the [J3] power input.

A green power led [LD4] will be illuminated when a valid power source is connected to either power input. A red power led [LD5] will be illuminated when a power source not within the correct voltage range (less than 22 VDC or greater than 52 VDC).

2.1.2 Power Control [SW1] with LED for Status [LD7][LD8][LD9]

The EVM supports a manual switch [SW1] for power control to the EVM. The switch [SW1] is a two-position switch. The OFF position disconnects input power from on-board circuitry. The ON position connects the input power.

Three status LEDs [LD7][LD8][LD9] are used to communicated power status to the user.

Table 2-2. Power Domain Status

LED	'ON' State	'OFF' State
[LD7]	Power switch [SW1] is in the ON position, and input power is being supplied to the EVM.	Power switch [SW1] is in the OFF or there is some other issue causing power to not be supplied.
[LD8]	MCU domain of the EVM is powered	MCU domain of the EVM is not powered/OFF (1)
[LD9]	MAIN domain of the EVM is powered	MAIN domain of the EVM is not powered/OFF (1)

Note

The power management IC (PMIC) includes functions to monitor power domains, including over/under voltage, over current, and residual voltage. If the PMIC detects and error, it may transition to 'safe-mode' where it powers down both the MCU and MAIN domains.

2.1.3 Power Budget Considerations

The exact power required for the EVM is largely dependent on the application, usage of the on-board peripherals, and power needs of the add-on devices. Table 2-3 shows the design's power allocations. Again, the input supply must be capable of supplying the power needs of your application.

Table 2-3. Power Allocation

Function	Power	Description
Processor Core	TBD	Processor, DDR Memory
Memory, Non-Volatile	TBD	xSPI NOR, eMMC, UFS, etc.
On-Board Peripherals	TBD	Ethernet, CPLD, Boot Logic, etc.
USB Port(s)	TBD	Type A Port(s), Type C
Expansion Interface(s)	TBD	PCIe, PCIe M.2, SGMII Expansion
Camera Port(s)	TBD	RPI Camera(s), Camera Expansion
Display(s)	TBD	DisplayPort/HDMI Panel(s), DP/HDMI Transceiver(s)

2.2 User Inputs

The EVM supports several mechanisms for the user to configure, control, and provide input to the system.

2.2.1 Board Configuration Settings [SW2] [SW4] [SW13] [SW16]

Dip switches [SW2] [SW4] [SW13] [SW16] are used to configure different options available on the EVM.

Table 2-4. Dip Switch [SW2] [SW13] EVM Configuration Settings

[SW2] Position	Default	Function	Description
SW2.1	OFF	Octal-SPI Memory Selection	MUX to select between non-volatile Octal-SPI memory connected to the MCU_OSPI0 interface: '0' (OFF) = xSPI Memory is selected '1' (ON) = Octal-NAND is selected

Table 2-4. Dip Switch [SW2] [SW13] EVM Configuration Settings (continued)

[SW2] Position	Default	Function	Description
SW2.2	ON	Debug/Trace Enable	MUX to select between Debug/Trace (connected via MIPI 60 emulation interface) and variety of 'other' EVM features (1): '0' (OFF) = 'Other' EVM features are selected/enabled '1' (ON) = Debug/Trace is enabled to MIPI-60 emulation interface
SW2.[4:3]	OFF:OFF	USB Type C Mode Selection	Set Mode for USB Type C interface (USB0): '00' (OFF/OFF) = DFP (Downstream Facing Port) '01' (OFF/ON) = DRP (Dual Role Port) '1X' (ON, Don't Care) = UFP (Upstream Facing Port)
SW2.5	OFF	PCIe0 Mode Selection	Set Mode for PCIe0 (4-Lane) '0' (OFF) = Root Complex '1' (ON) = End Point
SW2.6	OFF	PCIe1 Mode Selection	Set Mode for PCIe1 (2-Lane) '0' (OFF) = Root Complex '1' (ON) = End Point
SW2.7	ON	IO Voltage for Serial Camera Add-on Board(s)	Configures IO supply for Serial Camera Expansion Interface (I2C, GPIO, etc). Voltage levels of CSI2-RX signals is defined by MIPI specification. '0' (OFF) = IO Levels are set to 3.3VDC '1' (ON) = IO Levels are set to 1.8VDC
SW2.8	ON	Reserved	Reserved for future feature enhancement. Must be set to '1' (ON) for EVM to function correctly. '0' (OFF) = Invalid setting '1' (ON) = Must be set to '1'
SW2.9	ON	EVM Configuration EEPROM Write Protection	Sets EVM's configuration EEPROM Write Protection '0' (OFF) = Configuration EEPROM can be updated '1' (ON) = Configuration EEPROM cannot be updated/is protected
SW2.10	ON	User Defined	User Defined, maps to GPIO/IO Expander Input (See GPIO tables) '0' (OFF) = User Defined '1' (ON) = User Defined
SW13.1	OFF	LIN1 Mode Selection	Configure Master/Slave mode for LIN1 Interface '0' (OFF) = Slave Mode '1' (ON) = Master Mode
SW13.2	OFF	LIN2 Mode Selection	Configure Master/Slave mode for LIN2 Interface '0' (OFF) = Slave Mode '1' (ON) = Master Mode

Note

A variety of signals multiplex with the Debug/Trace interface on the processor. If Trace is enabled, the following signals are no longer available on the EVM (impacting some peripherals), including: Audio, CAN Bus 4/5, and RGMII1 Ethernet.

Table 2-5 shows the J7AHP EVM configuration switches [SW4] [SW16] to set the various Power Management IC (PMIC) and reset functions.

Table 2-5. Dip Switch [SW4][SW16] EVM Configuration Settings

[SW16] Position	Default	Function	Description
SW4.1	OFF	Reserved / Test Mode (Wait Reset)	Reserved, Must set to '0' (OFF) for normal EVM operation (only used in Test Mode)
SW4.2	OFF	Reserved / Test Mode (Wait Reset)	Reserved, Must set to '0' (OFF) for normal EVM operation (only used in Test Mode)
SW16.1	ON	Reserved / Tests Mode (PMIC Enable)	Reserved, Must set to '1' (ON) for normal EVM operation (only used in Test Mode) '0' (OFF) = Disable PMIC (Do Not Use) '1' (ON) = Enable PMIC
SW16.2	ON	Reserved / Test Mode (VMonitor Enable)	Reserved, Must set to '1' (ON) for normal EVM operation (only used in Test Mode) '0' (OFF) = Disable Voltage Monitor (Do Not Use) '1' (ON) = Enable Voltage Monitor
SW16.3	ON	Reserved / Test Mode (Disable)	Reserved, Must set to '1' (ON) for normal EVM operation '0' (OFF) = Enable Test Mode (Do Not Use) '1' (ON) = Disable Test Mode
SW16.4	ON	Watchdog Disable	Enable/Disable of Watchdog Timer within PMIC. (Note this can cause processor reset if watchdog is not managed.) '0' (OFF) = Watchdog Timer is Enabled '1' (ON) = Watchdog Timer is Disabled

2.2.2 Boot Configuration Settings [SW7] [SW11]

Dip switches [SW7] [SW11] are used to configure different boot options available on the processor.

Two common boot mode settings are documented below. For a complete definition and list of all supported modes, see the TDA4AP-Q1/TDA4VP-Q1/TDA4AH-Q1/TDA4VH-Q1 Technical Reference Manual (TRM).

No Boot: The processor will not attempt to boot any software. This is often selected when downloading software using an emulator.

SW7 [8:1] = 0000 1110

SW11[8:1] = 0001 0001

SD Card Boot: The processor will attempt to boot from image on SD Card.

SW7[8:1] = 0000 0000 (Default)

SW11 [8:1] = 0100 0001 (Default)

The Dip Switch boot tables are formatted to align with how the settings are documented in the TRM.

Table 2-6. Dip Switch [SW7] Configuration for MCU_BOOTMODE

MCU_BOOTMODE Pin Mapping							
0:2 [SW7.1]	3 [SW7.2]	4 [SW7.3]	5 [SW7.4]	6 [SW7. 5]	7 [SW7.6]	8 [SW7.7]	9 [SW7.8]
PLL Configuration Must be set to '0' (OFF)	Primary Boot Mode A			MCU Only	Reserved Must be set to '0' (OFF)	POST Config	

Table 2-7. Dip Switch [SW11] Configuration for BOOTMODE

BOOTMODE Pin Mapping							
0 [SW11.1]	1 [SW11.2]	2 [SW11.3]	3 [SW11.4]	4 [SW11.5]	5 [SW11.6]	6 [SW11.7]	7 [SW11.8]
Primary Boot B	Backup Boot Mode			Primary Boot Mode Config			Backup Boot Mode Config

2.2.3 Reset Pushbuttons [SW9] [SW10] [SW12] [SW14]

When pressed, the specific EVM domain is issued a reset, and is held in reset until the button is released.

Table 2-8. Reset Pushbuttons

Push Button	Domain	Function	Description
[SW14]	All	Power-On Reset	Power-On/Cold Reset for EVM, resets both processor domains (MCU, MAIN) and all EVM peripherals.
[SW12]	MCU	MCU Warm Reset	Warm reset for MCU domain
[SW10]	MAIN	Power-On Reset	Power-On/Cold Reset for MAIN domain, MCU domain is unaffected
[SW9]		Warm Reset	Warm reset for MAIN domain

2.2.4 User Pushbuttons [SW3] [SW5] [SW6] [SW8] [SW15] with User LED Indication [LD2] [LD3]

The pushbutton(s) primary function is to be user/application defined. The inputs can be monitored and/or configured to generate an interrupt. Some pushbutton(s) support a secondary function. They can be used to wake the system from a low power mode. Table 2-9 lists a complete definition for each pushbutton.

Table 2-9. User Pushbuttons and LEDs

Push Button	Primary Function	Alternate Function
[SW3]	User Define (GPIO0_11)	Wake from low power mode (MAIN IO_RET)
[SW5]	User Define (WKUP_GPIO0_7)	Wake from software initiated power-down (OFF)
[SW6]	User Define (GPIO0_0)	External Interrupt (EXTINTn)
[SW8]	User Define (WKUP_GPIO0_70)	Wake from low power mode (MCU IO_RET)
[SW15]	User Define (PMIC_GPIO4)	Wake from low power mode (any LP_STBY).
LED	**Primary Function**	**Alternate Function**
[LD2]	User Define (IO_EXP 0x22, bit P26)	None
[LD3]	User Define (IO_EXP 0x22, bit P27)	None

Note

The user-defined pushbutton inputs and LED outputs are connected to processor pins. The pins can be accessed via GPIO functions of the pin. The specific pin/GPIO used is identified in the table.

2.3 Standard Interfaces

The EVM provides industry standard interfaces/connectors to connect with a wide variety of peripherals. As these interfaces are standard, pin specific information is not provided in this document.

2.3.1 Uart-Over-USB [J48] [J49] with LED for Status [LD11] [LD12]

Six UART ports of the processor are interfaced with the UART-over-USB transceiver(s). When the EVM's USB micro-B connectors [J48] and/or [J49] are connected to a Host-PC using supplied USB cable (Type-A to Micro-B), the computer can establish Virtual Com Port(s) to be used with any terminal application. Virtual Com Port drivers for the transceiver(s) can be obtained from:

https://www.ftdichip.com/Products/ICs/FT2232H.html

https://www.ftdichip.com/Products/ICs/FT4232H.htm

Once installed, the Host-PC will create the Virtual Com Ports (two ports for FT2232, four ports for FT4232). Depending on the other Host-PC resources available, the Com Ports may not be located at COM1-2 and/or COM1-4. However, they will remain in the same numerical order for each transceiver.

The circuit(s) are powered from USB bus power and therefore the COM connection will not be lost when the EVM power is removed. LED(s) [LD11] [LD12] are used to indicated an active COM connection with Host-PC.

Table 2-10. UART to COM Port Mapping [J48] w/ Status [LD11]

UART Port	Host-PC COM Port
MCU_UART0	COM 1
WKUP_UART0	COM 2

Table 2-11. UART to COM Port Mapping [J49] w/ Status [LD12]

UART Port	Host-PC COM Port
UART8	COM 1
UART5	COM 2
UART2	COM 3
UART3	COM 4

The EEPROM of FTDI bridges are programmed with the EVM serial number, users to identify the connected COM port with board serial number when one or more boards connected to the computer.

Note

The maximum length for the IO cables should not exceed three meters.

2.3.2 Gigabit Ethernet [J39] [J40] with Integrated LEDs for Status

Two wired Ethernet networks are supported via RJ45 cable interfaces [J39] [J40]. Both are compatible with IEEE 802.3 10BASE-Te, 100BASE-TX, ad 1000BASE-T specification. The connector includes LEDs for link status and activity.

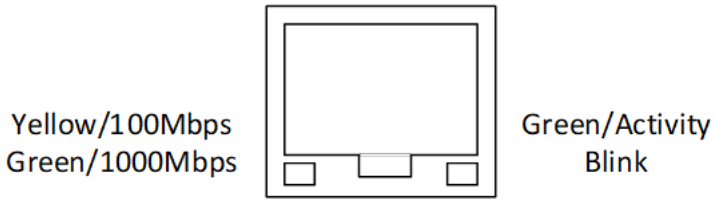


Figure 2-3. RJ45 LED Indicators [39] [J40]

Power-Over-Ethernet (PoE) is not supported.

2.3.3 USB3.1 Gen1 Interface [J4]

The EVM supports one USB3.1 Gen1 Type C interface [J4], which can function as DFP, UFP, or DRP. For details on how to select the USB mode, see Section 2.2.1. The VBUS output for this port is limited to 1.5 A. When operating as UFP, the EVM cannot be powered from this port.

The processor supports a single USB interface. Therefore, the user must configure for either the USB3.1 Type C interface or the USB2.0 Type A interface. Both cannot be operated simultaneously.

2.3.4 USB2.0 Interface [J5]

The EVM supports two USB2.0 Type A interfaces [J5] via an on-board USB hub. These ports can only function as Host. The VBUS output for each port is limited to 0.5 A.

The processor supports a single USB interface. Therefore, the user must configure for either the USB2.0 Type A interface or the USB3.1 Type C interface. Both cannot be operated simultaneously.

Note

The USB2.0 Micro-B connectors [J48] [J49] and [J1] are discussed in the UART-over-USB and/or Emulation sections. While these are USB interfaces, they are dedicated to peripherals and cannot be used for USB development.

2.3.5 PCIe Card Slot [J14] [J17]

The EVM supports two 4Lane PCIe Card slots for interfacing with up to PCIe Gen3 cards. PCIe0 interface [J14] supports the full 4 Lanes, while PCIe1 interface [J17] bandwidth is reduced to 2 Lanes. The PCIe1 interfaces [J17] requires the processor to generate the REFCLK. For PCIe0 [J14], the REFCLK is automatically generated (on-board).

2.3.6 Display Port Interfaces [J8] [J9]

The EVM supports two DisplayPort panels via standard DP cables interfaces [J8] [J9]. The processor's native DP [J9] supports resolutions up to 4K UHD (3840x216) including MST (Multi-Stream Transport) for connecting multiple panels. The second DisplayPort [J8] is supported via DP bridge device (SN65DSI86) and supports resolutions up to 1080p. The second DisplayPort (via bridge device) does not support integrated audio.

2.3.7 MicroSD Card Cage [J53]

The EVM supports a micro-SD card cage [J53]. It supports UHS-1 class memory cards, including SDHC and SXDC. The connector is a push-push connector, meaning your push to insert the card and push again to eject/ remove the card.

A micro-SD card is included with the EVM kit.

2.3.8 Stereo Audio Interface [J29]

The EVM supports stacked 3.5-mm jacks [J29] for audio input/output. The top jack supports stereo microphone (with Mic bias) and the bottom jack supports stereo headphone outputs. The analog audio is supported via the PCM3168A codec, which supports sampling rates up to 96-KHz ADC/192-KHz DAC.

2.3.9 JTAG/Emulation Interface [J23] [J1]

The EVM includes an on-board emulation device (XDS110) for inspection and debugging of software. It is accessed via the USB microAB connector [J1]. If external emulation adapter is to be used, it is connected via the external emulation interface [J23]. This connector is aligned with the 60-pin MIPI standard for debug and trace (MIPI-60). On-board logic detects when adapter is connected and automatically switches emulation interface from on-board XDS110 to external.

2.4 Expansion Interfaces

The EVM provides several expansion interfaces that have non-standard/custom pinouts. Each of these interfaces are introduced and specific pin information is provided.

Note that some of the interfaces include ‘Direction’ information. This is relative to the EVM, so INPUT is input to the EVM/output of the connected device. OUTPUT is output of the EVM/input to the connected device.

2.4.1 Heatsink [ACC1] with Fan Header [J24]

The heatsink supports cooling of the device at ambient temperatures. If your environment or use case requires additional cooling, a fan can be added to the heatsink.

The fan connector is a 3-pin header (440054-3 from TE Connectivity), and supports 12VDC fans. Mating connector is 440129-3 and 1735801-1.

Table 2-12. Fan Header Pin Definition [J24]

Pin #	Pin Name	Description	Direction
1	<open>	Unconnected	n/a
2	12V	12V Supply	Output
3	GND	Ground	

2.4.2 CAN-FD Connectors [J41-J46]

The EVM supports up to six (6) CAN Bus interfaces.

Table 2-13. CAN-FD Interface Assignment

Connector	Process Resource
J41	CAN3
J42	MCU CAN0
J43	MCU CAN1
J44	CAN5
J45	CAN4
J46	CAN16

Each Controller Area Network (CAN) Bus interface is supported on a 3-pin, 2.54-mm pitch header. The interface meets ISO 11898-2 and ISO 11898-5 physical standards, and supports CAN and optimized CAN-FD performance up to 8 Mbps. Each includes CAN Bus end-point termination. If the EVM is included in a network with more than two nodes, the termination my need to be adjusted.

Table 2-14. CAN-FD Header Pin Definition [J41-J46]

Pin #	Pin Name	Description	Direction
1	CAN-H	High-Level CAN Bus Line	BI-Dir
2	GND	Ground	
3	CAN-L	Low-Level CAN Bus Line	Bi-Dir
4	WAKE (J41 only)	Assert PHY Wake Function	Input

2.4.3 LIN Connectors [J28]

The EVM supports up to two (2) LIN Bus interfaces. The Local Interconnect Network (LIN) is a single wire bidirectional bus used for low speed in-vehicle networks. The two EVM interfaces are supported on a 4-pin, 2.54-mm pitch header [J28]. The interface meets LIN 2.2A and ISO/DIS17987-4.2 physical standards, and supports rates up to 100kbps, and is design to support 12-V applications. Each LIN interface has option of being master or slave. See Section 2.2.1 for configuration details.

Table 2-15. LIN Header Pin Definition [J28]

Pin #	Pin Name	Description	Direction
1	VBUS_LIN	LIN Bus Power (4V-45V)	Input (optional)
2	LIN #1	Interface using UART6	Bi-Dir
3	LIN #2	Interface using UART9	Bi-Dir
4	GND	Ground	

2.4.4 Serial Ethernet Expansion Interfaces [J52] [J51]

The EVM include dual 60-pin (3x30, 0.8-mm pitch) high speed connectors [J52] [J51] for connecting with serial Ethernet PHYs and other serial Ethernet peripherals. Each expansion connector can support up to two SGMII interfaces. The bandwidth of the SGMII interfaces are 10Gbps and 2.5Gbps. The expansion connectors(s) also include power and other IO for communicating with the Ethernet peripheral(s). The voltage levels for all control IO is 3.3 V.

Table 2-16. Serial Ethernet Expansion Pin Definition [J52] [J51]

Pin #	Pin Name	Description Processor Resource for [J52] / [J51]	Dir
1	GND	Ground	
2	SGMIIa_TX_P	Serial Ethernet Transmit (SGMII5 / SGMII6)	Output
3	SGMIIa_TX_N	Serial Ethernet Transmit (SGMII5 / SGMII6)	Output
4	GND	Ground	
5	SGMIIa_RX_P	Serial Ethernet Receive (SGMII5 / SGMII6)	Input

Table 2-16. Serial Ethernet Expansion Pin Definition [J52] [J51] (continued)

Pin #	Pin Name	Description Processor Resource for [J52] / [J51]	Dir
6	SGMIIa_RX_N	Serial Ethernet Receive (SGMII5 / SGMII6)	Input
7	GND	Ground	
8	<open>		
9	<open>		
10	GND	Ground	
11	Power	Power for IO Level, 3.3 V	Output
12	Power	Power for IO Level, 3.3 V	Output
13	GND	Ground	
14	EEPROM_A0	Expansion EEPROM Address (A0)	Output
15	EEPROM_A1	Expansion EEPROM Address (A1)	Output
16	EEPROM_A2	Expansion EEPROM Address (A2)	Output
17	GND	Ground	
18	EEPROM_WP	Expansion EEPROM Write Protect	Output
19	REFCLK	Reference Clock, 25 MHz	Output
20	GND	Ground	
21	EEPROM_I2C_SCL	EEPROM I2C Clock (WKUP_I2C0)	Output
22	EEPROM_I2C_SDA	EEPROM I2C Data (WKUP_I2C0)	Bi-Dir
23	GND	Ground	
24	I2C_SCL	I2C Bus Clock (I2C0)	Output
25	I2C_SDA	I2C Bus Data (I2C0)	Bi-Dir
26	GND	Ground	
27	Power	Power, 12 V	Output
28	Power	Power, 12 V	Output
29	GND	Ground	
30	GPIO	PowerDown (IO Expander 0x22 bit P20 / bit P11)	Output
31	GPIO	Interrupt (WKUP_GPIO0_84 / WKUP_GPIO0_85)	Input
32	GND	Ground	
33	SGMIIb_TX_P	Serial Ethernet Transmit (SGMII1 / SGMII2)	Output
34	SGMIIb_TX_N	Serial Ethernet Transmit (SGMII1 / SGMII2)	Output
35	GND	Ground	
36	SGMIIb_RX_P	Serial Ethernet Receive (SGMII1 / SGMII2)	Input
37	SGMIIb_RX_N	Serial Ethernet Receive (SGMII1 / SGMII2)	Input
38	GND	Ground	
39	REFCLK_N	Diff Reference Clock, 125 MHz	Output
40	REFCLK_P	Diff Reference Clock, 125 MHz	Output
41	GND	Ground	
42	MDIO_C	MDIO Bus Clock (MDIO1)	Output
43	MDIO	MDIO Bus Data (MDIO1)	Bi-Dir
44	GND	Ground	
45	GPIO	Resetz (IO Expander 0x22 bit P21 / bit P24)	Output
46	GPIO	GPIO (IO Expander 0x22 bit P22 / bit P01)	Bi-Dir
47	GPIO	GPIO (IO Expander 0x22 bit P23/ bit P12)	Bi-Dir
48	GND	Ground	
49	Power	Power, 5 V	Output
50	Power	Power, 5 V	Output

Table 2-16. Serial Ethernet Expansion Pin Definition [J52] [J51] (continued)

Pin #	Pin Name	Description Processor Resource for [J52] / [J51]	Dir
51	GND	Ground	
52	<open>		
53	<open>		
54	GND	Ground	
55	Power	Power, 3.3 V	Output
56	Power	Power, 3.3 V	Output
57	GND	Ground	
58	<open>		
59	<open>		
60	GND	Ground	

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

2.4.5 Camera Interfaces [J55] [J57]

The EVM includes dual 40-pin (2x20, 0.5-mm pitch) high speed connectors [J57] [J55] for connecting with cameras and other image capture devices. Each expansion connectors can support up to two CSI2 interfaces. The bandwidth of each CSI2 interface is 10Gbps (4 data lanes each up to 2.5Gbps). The expansion connector(s) also includes power and other IO for communicating with the capture devices. All control signals are configurable for 3.3-V or 1.8-V IO voltage levels. See Section 2.2.2 for configuration details.

Table 2-17. High Speed Camera Expansion Pin Definition [J57][J55]

Pin #	Pin Name	Description Processor Resource for [J57] / [J55]	Dir
1	Power	Power, 12 V	Output
2	I2C_SCL	I2C Bus Clock (I2C5)	Bi-Dir
3	Power	Power, 12 V	Output
4	I2C_SDA	I2C Bus Data (I2C5)	Bi-Dir
5	CSIa_CLK_P	CSI Port 0 / Port 2	Input
6	GPIO0/PWMA	IO Expander 0x20 bit P1 / Open	Output
7	CSIa_CLK_N	CSI Port 0 / Port 2	Input
8	GPIO1/PWMV	IO Expander 0x20 bit P2 / bit P4	Bi-Dir
9	CSIa_D0_P	CSI Port 0 / Port 2	Input
10	REFCLK	25MHz Reference Clock	Output
11	CSIa_D0_N	CSI Port 0 / Port 2	Input
12	GND	Ground	
13	CSIa_D1_P	CSI Port 0 / Port 2	Input
14	RESETz	GPIO, IO Expander 0x20 bit P0	Output
15	CSIa_D1_N	CSI Port 0 / Port 2	Input
16	GND	Ground	
17	CSIa_D2_P	CSI Port 0 / Port 2	Input
18	GPIO2	GPIO0_26 / IO Expander 0x20 bit P5	Bi-Dir
19	CSIa_D2_N	CSI Port 0 / Port 2	Input
20	GPIO3	IO Expander 0x20 bit P3 / bit P6	Bi-Dir
21	CSIa_D3_P	CSI Port 0 / Port 2	Input
22	GPIO4	GPIO0_28 / IO Expander 0x20 bit P7	Bi-Dir
23	CSIa_D3_N	CSI Port 0 / Port 2	Input

Table 2-17. High Speed Camera Expansion Pin Definition [J57][J55] (continued)

Pin #	Pin Name	Description Processor Resource for [J57] / [J55]	Dir
24	GND	Ground	
25	CSIb_CLK_P	CSI Port 1 / Open	Input
26	CSIb_D3_P	CSI Port 1 / Open	Input
27	CSIb_CLK_N	CSI Port 1 / Open	Input
28	CSIb_D3_N	CSI Port 1 / Open	Input
29	CSIb_D0_P	CSI Port 1 / Open	Input
30	Power	Power, 3.3 V	Output
31	CSIb_D0_N	CSI Port 1 / Open	Input
32	Power	Power, 3.3 V	Output
33	CSIb_D1_P	CSI Port 1 / Open	Input
34	Power	Power, 3.3 V	Output
35	CSIb_D1_N	CSI Port 1 / Open	Input
36	Power	Power, 3.3 V	Output
37	CSIb_D2_P	CSI Port 1 / Open	Input
38	Power	Power, IO Level (1.8 V or 3.3 V)	Output
39	CSIb_D2_N	CSI Port 1 / Open	Input
40	Power	Power, IO Level (1.8 V or 3.3 V)	Output

Note

In the DIR column, output is to the expansion module, input is from the expansion module. Bi-Dir signals can be configured as either input or output.

2.4.6 Automation and Control Connector [J50]

The EVM supports an interface to allow for automated control of the system, including functions like on/off, reset, and boot mode settings.

Table 2-18. Test Automation Interface Pin Definition [J50]

Pin #	Pin Name	Description	Dir
1	Power	Power, 3.3 V	Output
2	Power	Power, 3.3 V	Output
3	Power	Power, 3.3 V	Output
4-6	<open>		
7	GND	Ground	
8-15	<open>		
16	GND	Ground	
17-24	<open>		
25	GND	Ground	
26	POWERDOWNz	EVM Power Down	Input
27	PORz	EVM Power-On/Cold Reset (MCU_PORz)	Input
28	RESETz	EVM Warm Reset (RESETz)	Input
29	<open>		
30	INT1z	EXTINT / GPIO0_0	Input
31	INT2z	WKUP_GPIO0_7	Bi-Dir
32	<open>		
33	BOOTMODE_RSTz	Bootmode Buffer Reset	Input
34	GND	Ground	
35	<open>		

Table 2-18. Test Automation Interface Pin Definition [J50] (continued)

Pin #	Pin Name	Description	Dir
36	Bus #1 I2C_SCL	INA Bus #1 I2C (optional connection to Processor I2C1)	Bi-Dir
37	Bus #2 I2C_SCL	INA Bus #2 I2C	Input
38	Bus #1 I2C_SDA	INA Bus #1 I2C (optional connection to Processor I2C1)	Bi-Dir
39	Bus #2 I2C_SDA	INA Bus #2 I2C	Bi-Dir
40	GND	Ground	
41	GND	Ground	
42	GND	Ground	

Note

In the DIR, column, output is to the test automation controller, input is from the automation controller. Bi-Dir signals can be configured as either input or output.

Note

The Signal polarity is defined with a trailing 'z' in the Pin Name, which indicates the signal is active LOW. For example, POWERDOWNz is an active low signal, meaning '0' = EVM is Powered Down, '1' = EVM is NOT Powered Down.

2.4.7 ADC [J27]

The EVM supports a interface for connecting external peripherals with ADC inputs. A 20-pin, dual row, 2.54-mm pitch pin header [J27] supports eight (8) input channels to ADC0, two (2) channels to ADC1, and trigger, and ADC reference signals. See the EVM schematic for pinout details.

2.4.8 SPI [J26]

The EVM supports connecting external peripherals with SPI interface. A 6-pin, 2.54-mm pitch pin header [J26] supports a single SPI interface (SPI5), including clock, data input, data output, two chip selects, and GND. See the EVM schematic for pinout details.

2.4.9 CSI-TX [J10]

The EVM includes a 40-pin (2x20, 0.5-mm pitch) high speed camera transmit interface [J10]. The expansion connector supports a single CSI2-TX (4Lane) interface. The interface is designed for internal testing, and may not include all the required power/signals for interfacing with a display. See schematic for connector pinout details.

2.4.10 Accessory Power Connector [J47]

A power output connector [J47] is provided for conditions where an expansion board requires additional power. The 2-pin connector (Phoenix 1757242) supplies a regulated 12-V output, up to 5000 mA. Mating connector is TBD.

Table 2-19. Accessory Power Connector [J47]

Pin #	Pin Name	Description	Dir
1	GND	Ground	
2	Power	Power, 12 V	Output

3 Circuit Details

This section provides additional details of the EVM design and processor connections.

3.1 Top Level Diagram

Figure 3-1 shows the functional block diagram of the EVM.

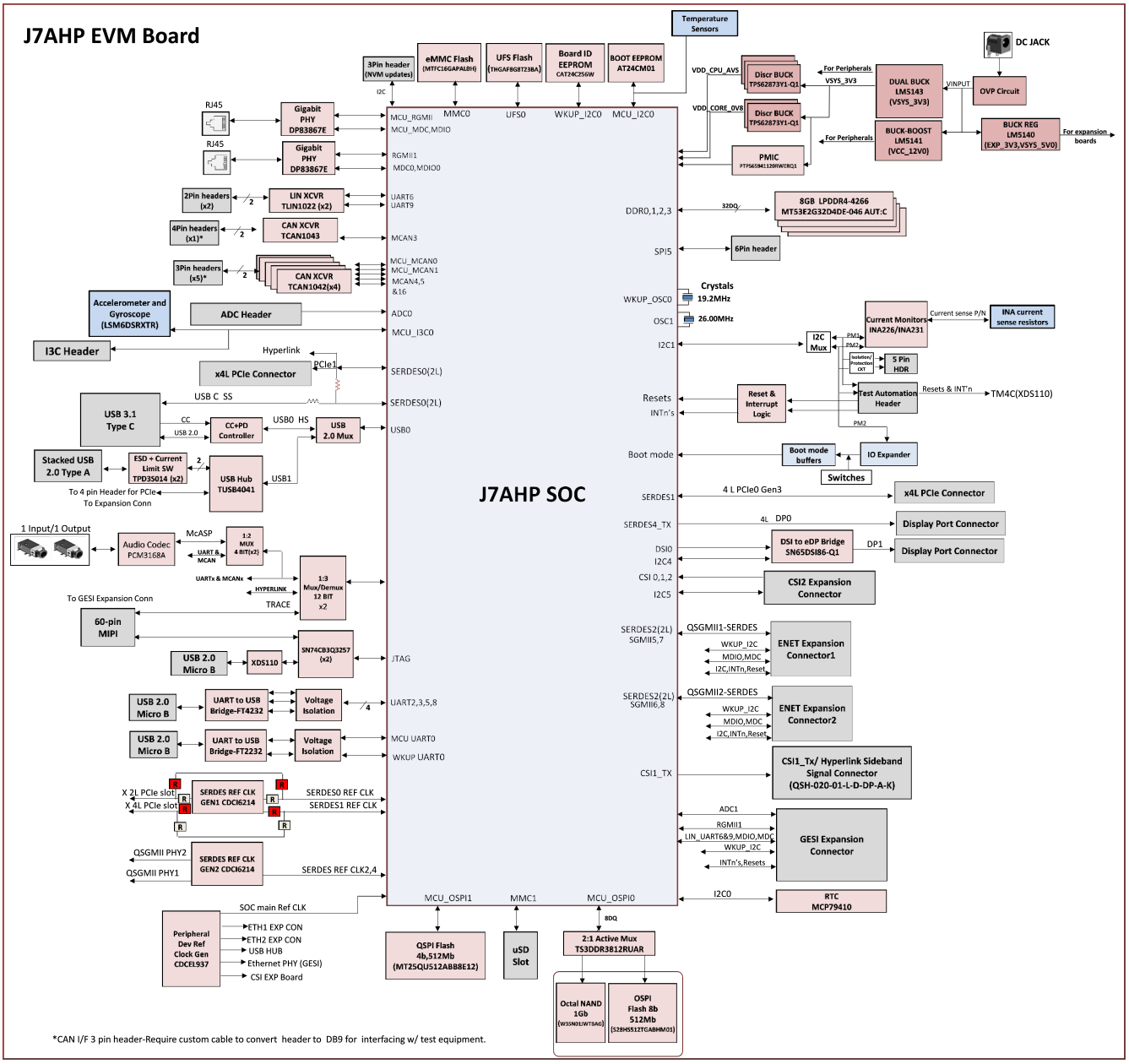


Figure 3-1. J7AHP EVM Board Functional Block Diagram

3.2 Interface Mapping

The EVM interface mapping tables is provided in Table 3-1.

Table 3-1. Interface Mapping Table

Connected Peripheral	Processor Resource(s)	Component/Part Numbers
Memory, LPDDR4 DRAM	DDR0, DDR1, DDR2, DDR3	(4x) Micron, MT53E2G32D4DE-046 AUT:C
Memory, xSPI NOR Flash	MCU_OSPI0	Cypress, S28HS512TGABHM010
Memory, Octal NAND	MCU_OSPI0	Winbond, W35N01JWTBAG

Table 3-1. Interface Mapping Table (continued)

Connected Peripheral	Processor Resource(s)	Component/Part Numbers
Memory, Quad SPI NOR Flash	MCU_OSPI1	Micron, MT25QU512ABB8E12-0SIT
Memory, eMMC	MMC0	Micron, MTFC16GAPALBH-AAT ES
Memory, microSD Card	MMC1	
EEPROM, Board Identification	WKUP_I2C0	On-Semi, CAT24C256WI-GT3
EEPROM, Boot	MCU_I2C0	Microchip Tech, AT24CM01
Memory, UFS 2L Gear3	UFS0	Toshiba, THGAF8G8T23BAIL
Wired Ethernet	MCU_RGMII1, RGMII1	(2x) Texas Instruments, DP83867ERGZT
USB Type C + CC Controller	USB0 + SERDES0 (L2, L3)	Texas Instruments, TUSB321RWBR
USB Type A (2x)	USB0	Texas Instruments, TUSB4041IPAP
Audio Codec	McASP0	Texas Instruments, PCM3168APAP
PCIe 4L Card Slot	PCIe1 / SERDES0 (L0, L1)	
PCIe 4L Card Slot	PCIe0, SERDES1	
Quad USART Terminal	UART 8,5,2 & 3	FTDI, FT4232HL
Dual USART Terminal	WKUP_UART0, MCU_UART0	FTDI, FT2232HL
CAN (6x)	MCU_MCAN0, MCU_MCAN1, MCAN4, MCAN5, MCAN16	Texas Instruments, TCAN1042HGVD
	MCAN3	Texas Instruments, TCAN1043-Q1
LIN (2x)	UART6, UART9	Texas Instruments, TLIN1022DMTTQ1
CSI RX Interface	CSI0, CSI1, CSI2	QSH Connector-J57(QSH-020-01-L-D-DP-A-K)
Display Port	DP0	
	DSI0	Texas Instruments, SN65DSI86IPAPQ1
ADC Header	MCU_ADC0	

Note

MCU_OSPI1 is connected to two different flash memories, target memory selected via a mux.

3.3 I2C Address Mapping

Table 3-2 provides the complete I2C address mapping details for the EVM.

Table 3-2. I2C Mapping Table

Connected Peripheral	Processor Resources		Component / Part Number
	I2C Port	I2C Address	
EEPROM, Board Identification	WKUP_I2C0	0x50	On-Semi, CAT24C256WI-GT3
Power Management IC (PMIC)	WKUP_I2C0	0x48-4B	Texas Instruments, TPS659413
Power Management IC (PMIC)	WKUP_I2C0	0x40, 0x43	(2x) Texas Instruments, TPS62873
Voltage Monitor	WKUP_I2C0	0x30, 0x31	(2x) Texas Instruments, PPS38900603NRTERQ1
Temperature Sensors	MCU_I2C0	0x48, 0x49	Texas Instruments, TMP100NA/3K
EEPROM, Boot	MCU_I2C0	0x50, 0x51	Microchip Tech, AT24CM01
PCIe0 / PCIE1 Card Slot(s)	I2C0	0x70, Add-On	Texas Instruments, TCA9543APWR
RTC Clock	I2C0	0x57,0x6F	Microchip, MCP79410-I/SN
Clock Generator, SERDES	I2C0	0x77,0x76	Texas Instruments, CDCI6214
Clock Generator, Peripherals	I2C0	0x6D	Texas Instruments, CDCEL937-Q1
I2C IO Expander, 16b	I2C0	0x20	Texas Instruments, TCA6416ARGJR
I2C IO Expander, 24b	I2C0	0x22	Texas Instruments, TCA6424ARGJR
ADC, Power Measurement	I2C1	0x40 to 0x4F	Texas Instruments, INA226

Table 3-2. I2C Mapping Table (continued)

Connected Peripheral	Processor Resources		Component / Part Number
	I2C Port	I2C Address	
I2C IO Expander, 8b	I2C3	0x20	Texas Instruments, TCA6408ARGTR
Audio Codec	I2C3	0x44	Texas Instruments, PCM3168A-Q1
I2C IO Expander, 8b	I2C4	0x20	Texas Instruments, TCA6408ARGTR
DisplayPort, Bridge	I2C4	0x2C, Add-On	Texas Instruments, SN65DSI86IPAPQ1
Expansion, Serial Ethernet	WKUP_I2C0	Add-On	
Expansion, Camera	WKUP_I2C0, I2C5	Add-On	

3.4 GPIO Mapping

The General Purpose IOs (GPIO) of the EVM are broken into two major groups, IO connected to processor or connected to I2C-based Expander. They are separated into two tables below.

Table 3-3. Processor Mapping for Processor IO

J784S4 GPIO	Function	DIR/Level	Remarks
WKUP_GPIO0_1	Boot EEPROM Write Protect	Output	'0' – Memory is NOT Write-Protected '1' – Memory is Write-Protected (default)
WKUP_GPIO0_2	MCU CAN Bus #1 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
WKUP_GPIO0_3	MCU CPSW2G Ethernet Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_6	SPI Flash Memory Selection	Bi-Dir	'0' – xSPI NOR Flash is selected '1' – Octal-NAND Flash is selected (Note Default is set via dip switch)
WKUP_GPIO0_7	Pushbutton [SW5] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
WKUP_GPIO0_28	USB Type C Cable Orientation	Input	'0' – Low Position Detected (Default) '1' – High Position Detected
WKUP_GPIO0_39	Power Management IC (PMIC) Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_55	System Power Down	Output	'0' – Normal Operation (default) '1' – System Power Down/Off
WKUP_GPIO0_56	MCU CPSW2G Ethernet Reset	Output	'0' – Ethernet PHY is Reset '1' – Ethernet PHYT is NOT Reset (default)
WKUP_GPIO0_66	Power Measurement Bus Selection	Bi-Dir	'0' – Selects Bus #1 for access to INAs (default) '1' – Selects Bus #2 for access to INAs
WKUP_GPIO0_69	MCU CAN Bus #0 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
WKUP_GPIO0_70	Pushbutton [SW8] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
WKUP_GPIO0_84	Serial Ethernet Expansion #1 Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
WKUP_GPIO0_85	Serial Ethernet Expansion #2 Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)

Table 3-3. Processor Mapping for Processor IO (continued)

J784S4 GPIO	Function	DIR/Level	Remarks
WKUP_GPIO0_86	IO Expander Interrupt (Bus I2C0)	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_3	DSI/DisplayPort Bridge Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_8	SD Card IO Voltage Selection	Output	'0' – SD Card IO Voltage is 1.8V '1' – SD Card IO Voltage is 3.3V (default)
GPIO_11	Pushbutton [SW3] System / User Interrupt	Input	'0' – Pushbutton is pressed '1' – Pushbutton is NOT pressed (default)
GPIO_18	IO Expander Interrupt (Bus I2C5)	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_21	CPSW2G Ethernet Interrupt	Input	'0' – Active Interrupt Request '1' – No Interrupt Requested (default)
GPIO_26	Camera Expansion #1 GPIO #2	Bi-Dir	Camera Expansion Board Specific (Pin 18)
GPIO_28	Camera Expansion #1 GPIO #4	Bi-Dir	Camera Expansion Board Specific (Pin 22)

Note

GPIO functions sometimes share pins with other functions. The default state of these IO are set by the MCU_BOOTMODE and/or BOOTMODE pins. For the EVM, these pins are set via dip switches.

Table 3-4. GPIO Mapping for Expansion IO

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P00	PCIe1 Mode Selection	Input	'0' – Processor/PCIe1 is Root Complex '1' – Processor/PCIe1 is End Point (Note Default is set via dip switch)
P01	PCIe1 PERSTz Status	Input	'0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P02	PCIe1 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe1 Reset is asserted '1' – PCIe1 Reset is NOT asserted
P03	PCIe1 PERSTz to PORz (End Point Mode)	Output	'0' – PCIe1 PERSTz is separate from PORz '1' – PCIe1 PERSTz can control PORz
P04	PCIe0 Mode Selection	Input	'0' – Processor/PCIe0 is Root Complex '1' – Processor/PCIe0 is End Point (Note Default is set via dip switch)
P05	PCIe0 PERSTz Status	Input	'0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted
P06	PCIe0 PERSTz Output (Root Complex Mode)	Output	'0' – PCIe0 Reset is asserted '1' – PCIe0 Reset is NOT asserted
P07	PCIe0 PERSTz to PORz (End Point Mode)	Output	'0' – PCIe0 PERSTz is separate from PORz '1' – PCIe0 PERSTz can control PORz
P10	PCIe1 Card Presence Detection	Input	'0' – Card detected for PCIe1 '1' – Card NOT detected for PCIe1 (default)
P11	PCIe0 Card Presence Detection	Input	'0' – Card detected for PCIe0 '1' – Card NOT detected for PCIe0 (default)

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P12	External Clock enabled for PCIe0	Output	'0' – External Clock is NOT enabled for PCIe0 '1' – External Clock is enabled for PCIe0 (default)
P13	External Clock enabled for PCIe1	Output	'0' – External Clock is NOT enabled for PCIe1 '1' – External Clock is enabled for PCIe1 (default)
P14	McASP (Audio) / CAN Mux Select	Output	'0' – McASP0 is selected to Codec (CAN3, CAN5 are disabled) (default) '1' – CAN3, CAN5 are selected, McASP0 (audio) is disabled
P15	GESI Expansion Mux Control	Output	Reserved (GESI Expansion is not supported)
P16	GESI Expansion Mux Control	Output	Reserved (GESI Expansion is not supported)
P17	GESI Expansion Ethernet Reset	Output	Reserved (GESI Expansion is not supported)
I2C0/TCA6424 Addr: 0x22	**Function**	**DIR/Level**	**Remarks**
P00	Serial Ethernet #1 Expansion Power Down	Output	'0' – Expansion board is active (default) '1' – Expansion board is powered down
P01	Serial Ethernet #1 GPIO1	Output	Expansion Board specific (Pin 46)
P02	Serial Ethernet REFCLK Program Enable	Output	'0' – I2C is not connected to CDC clock def (default) '1' – Expansion board is NOT reset
P03	Serial Ethernet #1 GPIO2	Bi-Dir	Expansion Board specific (Pin 47)
P04	Serial Ethernet #2 Expansion Reset	Output	'0' – Expansion board is RESET (default) '1' – Expansion board is NOT reset
P05	User Dip Switch Input [SW2]	Input	'0' – Dip Switch SW2 position 10 set to OFF '1' – Dip Switch SW2 position 10 set to ON (Note Default is set via dip switch SW2)
P06	User LED [LD2]	Output	'0' – LED [LD2] is ON '1' – LED [LD2] is OFF (default)
P07	User LED [LD3]	Output	'0' – LED [LD3] is ON '1' – LED [LD3] is OFF (default)
P10	Power Measurement Bus Enable	Output	'0' – Enabled access to INA from processor (I2C1) (default) '1' – Disables access to INA from processor
P11	Serial Ethernet #2 Expansion Power Down	Output	'0' – Expansion board is active (default) '1' – Expansion board is powered down
P12	Serial Ethernet #2 GPIO2	Bi-Dir	Expansion Board specific (Pin 47)
P13	External Clock Generator Reset	Output	'0' – Expansion board is RESET '1' – Expansion board is NOT reset (default)
P14	USB0 Mux Select	Output	'0' – USB0 is connected to Type C (default) '1' – USB0 interface is connected Type A (via hub)

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P15	Debug/Trace Enable (Note: This setting can affect other interfaces. See TBD)	Bi-Dir	'0' – Debug/Trace signals are enabled to MIPI-60 emulation interface [J23] '1' – Debug/Trace signals are NOT enabled to MIPI-60 interface [J23] (Note Default is set via dip switch SW2.2)
P16	Interface Mux Selection #1 (Note: This setting can affect other interfaces. See TBD)	Output	'0' – Alternate Interfaces are selected for Mux #1 '1' – Standard Interfaces are selected for Mux #1 (default)
P17	Interface Mux Selection #2 (Note: This setting can affect other interfaces. See TBD)	Output	'0' – Alternate Interfaces are selected for Mux #2 '1' – Standard Interfaces are selected for Mux #2 (default)
P20	CPSW2G Ethernet Reset	Output	'0' – Ethernet PHY is Reset '1' – Ethernet PHYT is NOT Reset (default)
P21	Serial Ethernet #2 GPIO1	Output	Expansion Board specific (Pin 46)
P22	SD Card Power Enable/Reset	Output	'0' – SD Card Power is disabled/Reset '1' – SD Card Power is enabled/active (default)
P23	USB Type C Power Enable	Output	'0' – USB Type C Power is disabled '1' – USB Type C Power is enabled (default)
P24	USB Type C Mode Selection	Bi-Dir	'00' = DFP (Downstream Facing Port) '01' = DRP (Dual Role Port)
P25			'1x' = UFP (Upstream Facing Port) (Note Default is set via dip switch [SW2 bits 3:4])
P26	LIN Bus PHY Enable	Output	'0' – LIN Bus PHY is Disabled (default) '1' – LIN Bus PHY is Enabled
P27	CAN Bus #3, #4, #5 Stand-by	Output	'0' – Normal Mode '1' – Standby Mode (default)
I2C3/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	Audio Codec Enable/Reset	Output	'0' – Audio Codec is disabled/Reset (default) '1' – Audio Codec is enabled/active
P01 – P07	Reserved / Unused	Bi-Dir	Reserved / Unused
I2C4/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**
P00	DisplayPort #0 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled
P01	DisplayPort #1 Power Enable	Output	'0' – DisplayPort Power is disabled (default) '1' – DisplayPort Power is enabled
P02	DisplayPort #1 Transmitter Enable	Output	'0' – DisplayPort Transmitter is disabled (default) '1' – DisplayPort Transmitter is enabled
P03-P07	Reserved / Unused	Bi-Dir	Reserved / Unused
I2C5/TCA6408 Addr: 0x20	**Function**	**DIR/Level**	**Remarks**

Table 3-4. GPIO Mapping for Expansion IO (continued)

I2C0/TCA6416 Addr: 0x20	Function	DIR/Level	Remarks
P00	Camera Expansion Reset (#1 and #2)	Output	'0' – Camera Expansion is disabled/Reset (default) '1' – Camera Expansion is enabled/active
P01	Camera Expansion #1 GPIO #0	Bi-Dir	Camera Expansion Board Specific (Pin 6)
P02	Camera Expansion #1 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8)
P03	Camera Expansion #1 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20)
P04	Camera Expansion #2 GPIO #1	Bi-Dir	Camera Expansion Board Specific (Pin 8)
P05	Camera Expansion #2 GPIO #2	Bi-Dir	Camera Expansion Board Specific (Pin 18)
P06	Camera Expansion #2 GPIO #3	Bi-Dir	Camera Expansion Board Specific (Pin 20)
P07	Camera Expansion #2 GPIO #4	Bi-Dir	Camera Expansion Board Specific (Pin 22)

3.5 Power Monitoring

The EVM includes power monitoring/measurement of 32 discrete power rails. The on-board analog-to-digital converters (INA226) are accessed via I2C. The processor can access using I2C1. The test automation [J50] can access the I2C bus, or it can be access externally via 5-pin header [J30]. Due to the number of rails, the ADCs are split across two I2C buses. Selection of the buses is done via mux setting (see Section 3.4)

Table 3-5. GPIO Mapping for Expansion IO

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x40	Processor MCU VDD (VDD_MCU_0V85)	0.85V	10m-ohm	0x40	Processor IO at 1.8V (VDD_IO_1V8)	1.8V	10m-ohm
0x41	Processor MCU RAM (VDD_MCU_RAM_0V85)	0.85V	10m-ohm	0x41	Processor IO at 3.3V (VDD_IO_3V3)	3.3V	10m-ohm
0x42	(VDA_MCU_1V8)	1.8V	10m-ohm	0x42	Processor Dual Voltage IO (VDD_SD_DV)	DV	10m-ohm
0x43	Processor MCU IO at 3.3V (VDD_MCUIO_3V3)	3.3V	10m-ohm	0x43	LPDDR4 Memory (VDD1) (VDD1_DDR_1V8)	1.8V	10m-ohm
0x44	Processor MCU IO at 1.8V (VDD_MCUIO_1V8)	1.8V	10m-ohm	0x44	(VDD_DDR_SOC_1V1)	1.1V	
0x45	(VDD_CORE_0V8)	N/A	N/A	0x45	(VCCA_3V3_CORE)	3.3V	5m-ohm
0x46	(VDD_RAM_0V85)	0.85V	10m-ohm	0x46	MCU Peripherals at 1.8V (VSYS_MCUIO_1V8)	1.8V	10m-ohm
0x47	(VDD_GPIORET_WK_0V8)	0.8V	10m-ohm	0x47	MCU Peripherals at 3.3V (VSYS_MCUIO_3V3)	3.3V	10m-ohm
0x48	(VDD_CPU_AVS)	N/A	N/A	0x48	(VSYS_IO_1V8)	1.8V	10m-ohm
0x49	(VSYS_GPIORET_IO_3V3)	3.3V	10m-ohm	0x49	(VSYS_IO_3V3)	3.3V	10m-ohm
0x4A	Processor LPDDR IO (VDD_DDR_1V1)	N/A	N/A	0x4A	(VCC_12V0_N)	12V	??m-Ohm
0x4B	(VDD_PHYCORE_0V8)	0.8V	10m-ohm	0x4B	(VSYS_5V0)	5V0	
0x4C	(VDA_PLL_1V8)	1.8V	10m-ohm	0x4C	(VSYS_3V3)	3V3	
0x4D	(VDA_PHY_1V8)	1.8V	10m-ohm	0x4D	(VCCA_3V3_DDR)	3.3V	10m-ohm
0x4E	(VDA_USB_3V3)	3.3V	10m-ohm	0x4E	(VDA_DLL_0V8)	0.8V	10m-ohm

Table 3-5. GPIO Mapping for Expansion IO (continued)

Bus #1 Address	Power Rail	Nom V	Shunt Value	Bus #2 Address	Power Rail	Nom V	Shunt Value
0x4F	(VDD_GPIORET_IO_3V3)	3.3V	10m-ohm	0x4F	(VCCA_3V3_CPU_AVS)	3.3V	5m-ohm

Note

In the table, the '(_name)' refers to the net name used in the schematic.

3.6 Shared Interfaces / Signal Muxing

Due to the number of features available on the EVM, there are some limitations for which features can be used simultaneously. Many of the conflicts revolve around the emulation/trace functionality. When trace is selected/ enabled, the following features are not accessible: Audio, Power Measurement (access from processor), LIN Bus, reduce CAN-FD availability (only MCU and MCAN16 available), as well as few other items. See schematic for a complete definition of interfaces which share resources.

3.7 Power Delivery Network (PDN)

Refer to separate document.

3.8 Identification EEPROM

The EVM board identity and revision information are stored in an on-board EEPROM. The first 259 bytes of the memory are pre-programmed with EVM identification information. The format of the data is provided in Table 3-6. The remaining bytes are available to user defined storage.

Table 3-6. Board ID Information

Field Name	Offset /Size	Value	Comments
MAGIC	0000 / 4B (Hex)	0xEE3355AA	Header Identifier
M_TYPE	0004 / 1B (Hex)	0x1	Fixed length and variable position board ID header
M_LENGTH	0005 / 2B (Hex)	0x10B	Size of payload
B_TYPE	0007 / 1B (Hex)	0x10	Payload type
B_LENGTH	0008 / 2B (Hex)	0x2E	Offset to next header
B_NAME	000A / 16B (CHAR)	J784S4X-EVM	Name of the board
DESGIN_REV	001A / 2B (CHAR)	E1	Revision number of the design
PROC_NBR	001C / 4B (CHAR)	141	PROC number
VARIANT	0020 / 2B (CHAR)	1	Design variant number
PCB_REV	0022 / 2B (CHAR)	E1	Revision number of the PCB
SCHBOM_REV	0024 / 2B (CHAR)	0	Revision number of the schematic
SWR_REV	0026 / 2B (CHAR)	1	first software release number
VENDORID	0028 / 2B (CHAR)	1	0x1: Manufactured by Mistral
BUILD_WK	002A / 2B (CHAR)		week of the year of production
BUILD_YR	002C / 2B (CHAR)		year of production
BOARDID	002E / 6B (CHAR)	0	
SERIAL_NBR	0034 / 4B (CHAR)	4	incrementing board number
DDR_TYPE	0038 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0039 / 2B (Hex)	0x2	offset to next header

Table 3-6. Board ID Information (continued)

Field Name	Offset /Size	Value	Comments
DDR_CONTROL	003B / 2B (Hex)	0xC560	DDR Control Word Bit 1:0 = ‘00’ First DDR Bit 3:2 = ‘00’ No SPD Bit 5:4 = ‘10’ LPDDR4 Bit 7:6 = ‘01’ 32 bits Bit 9:8 = ‘01’ 32 bits Bit 10 = ‘1’ dual rank Bit 13:11 = ‘000’ Density 64 Gb(bit 0 to 3) Bit 14 = ‘1’ ECC bits present (inline, not separate bits) Bit 15 = ‘1’ Density 64 Gb (bit 4)
DDR_TYPE	003D / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	003E / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	0040 / 2B (Hex)	0xC560	DDR Control Word)
DDR_TYPE	0042 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0043 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	0045 / 2B (Hex)	0xC560	DDR Control Word)
DDR_TYPE	0047 / 1B (Hex)	0x11	DDR Header Identifier
DDR_LENGTH	0048 / 2B (Hex)	0x2	offset to next header
DDR_CONTROL	004A / 2B (Hex)	0xC560	DDR Control Word)
MAC_TYPE	004C / 1B (Hex)	0x13	MAC address Header Identifier
MAC_LENGTH	004D / 2B (Hex)	0xC2	Size of payload
MAC_CONTROL	004F / 1B (Hex)	0x0	MAC header control word (0 = 1 MAC address)
MAC_ADDRS	0051 / 192B (Hex)		MAC address
END_LIST	0111 / 1B (Hex)	0xFE	End Marker

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