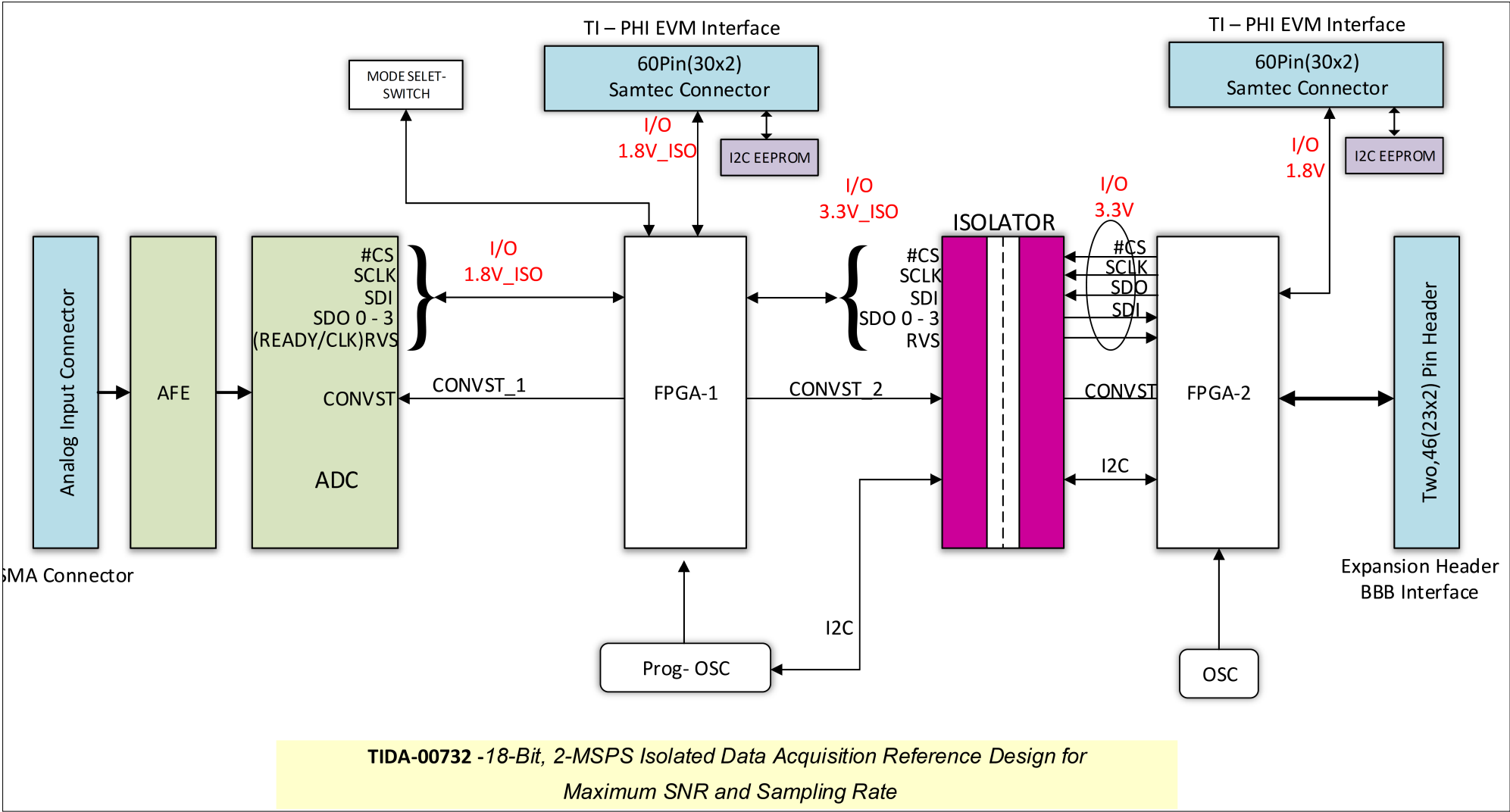


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

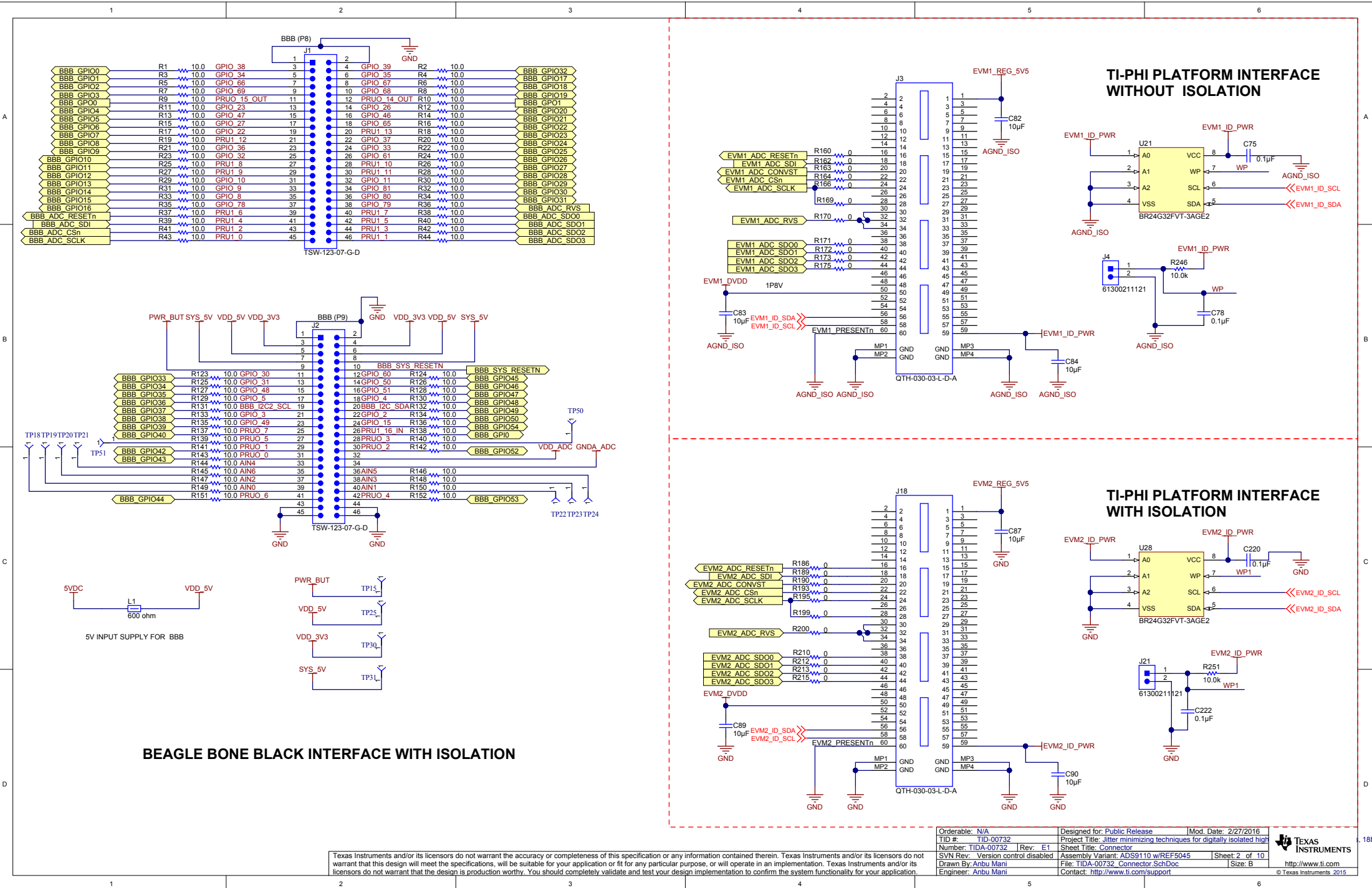


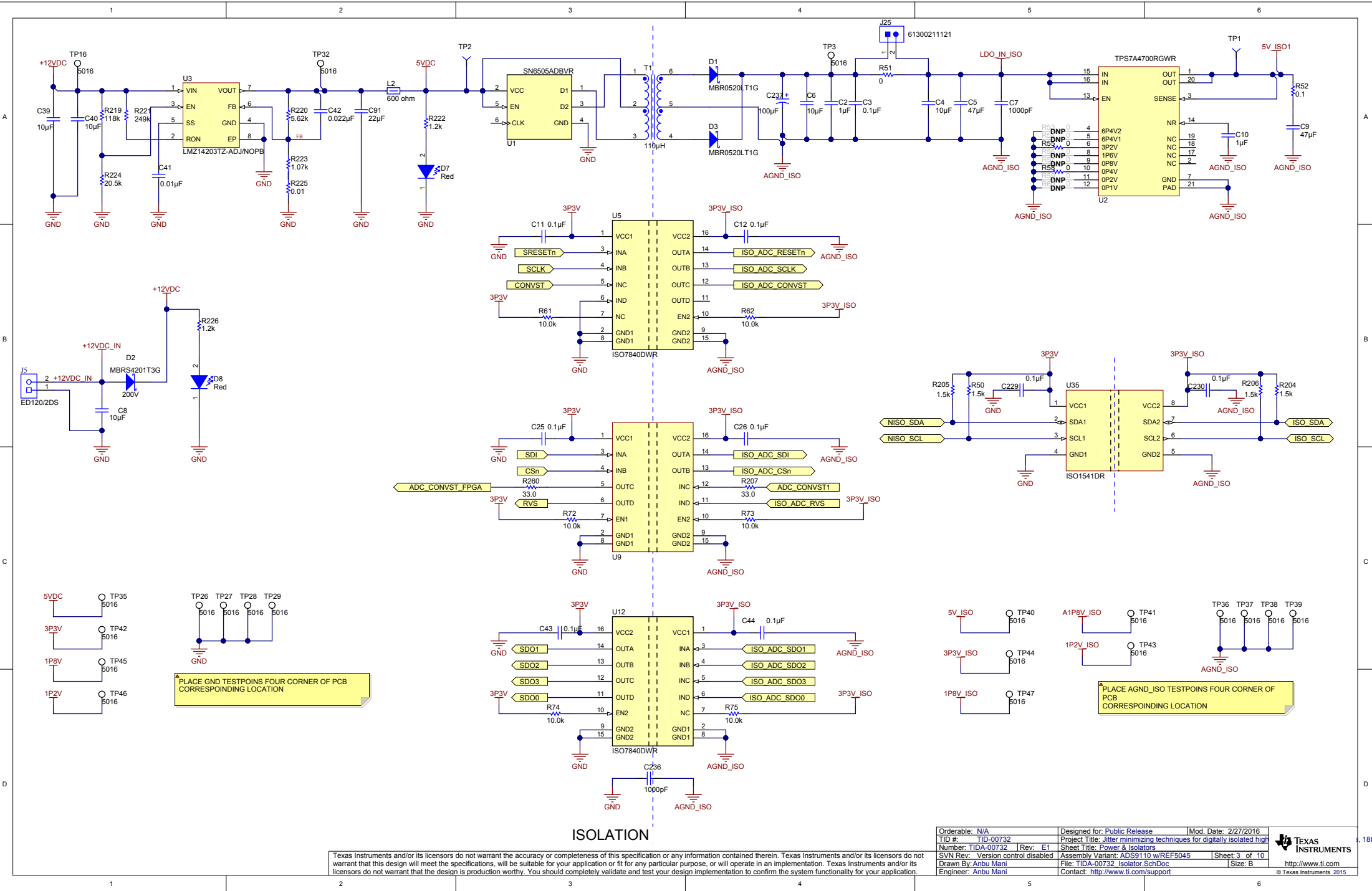
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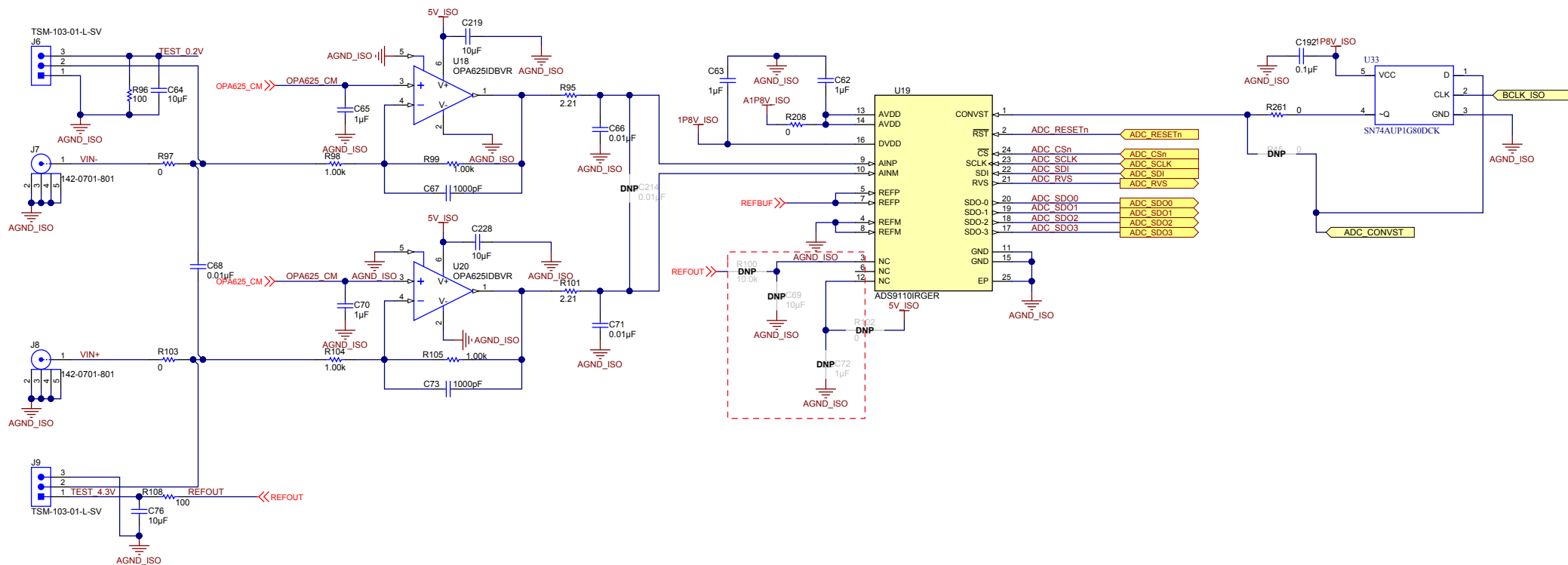
Orderable: N/A	Designed for: Public Release	Mod. Date: 5/26/2016
TID #: TIDA-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: Block Diagram
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 1 of 10
Drawn By: Anbu Mani	File: TIDA-00732_CoverSheet_SchDoc	Size: B
Engineer: Anbu Mani	Contact: http://www.ti.com/support	http://www.ti.com



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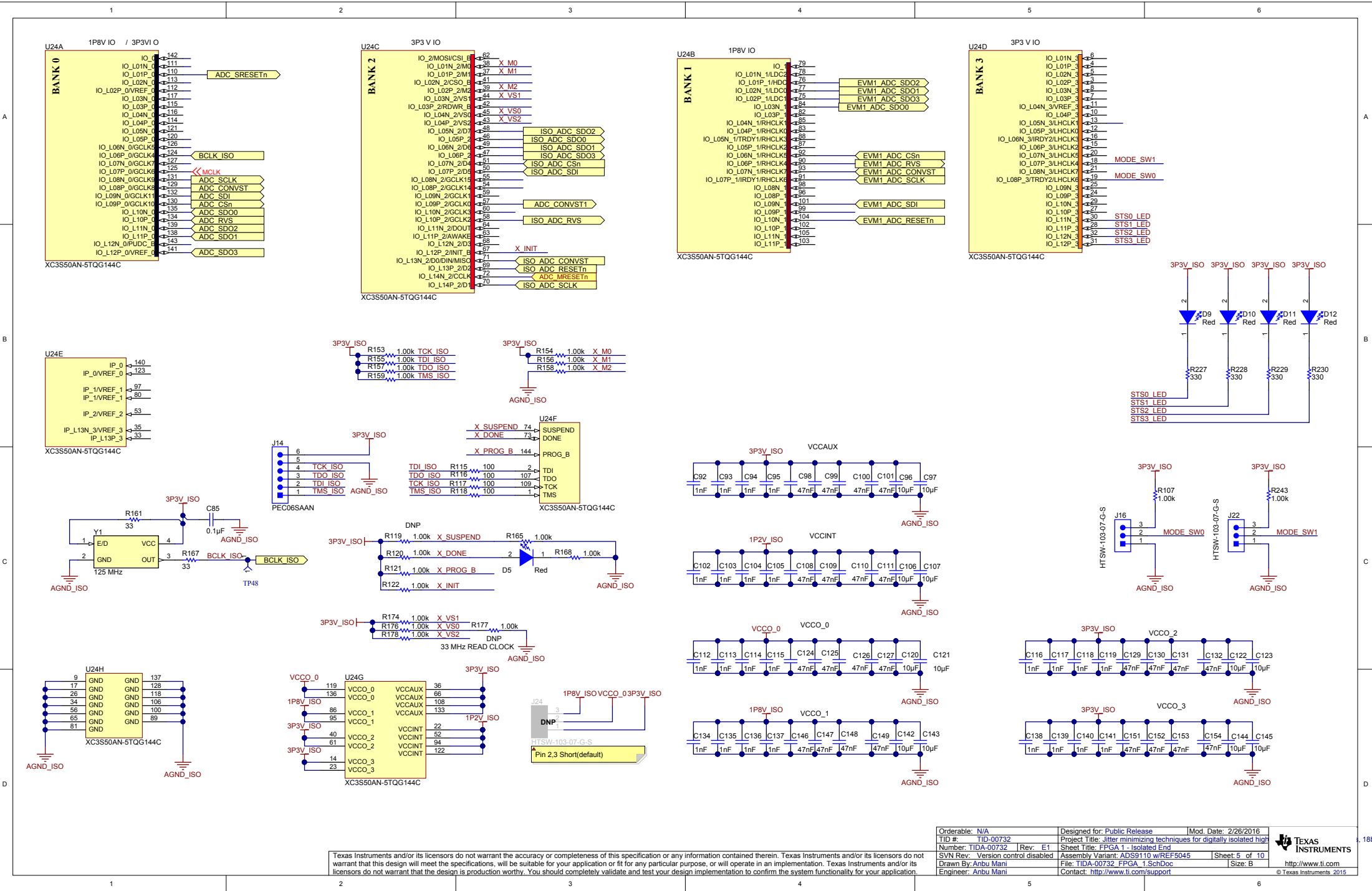


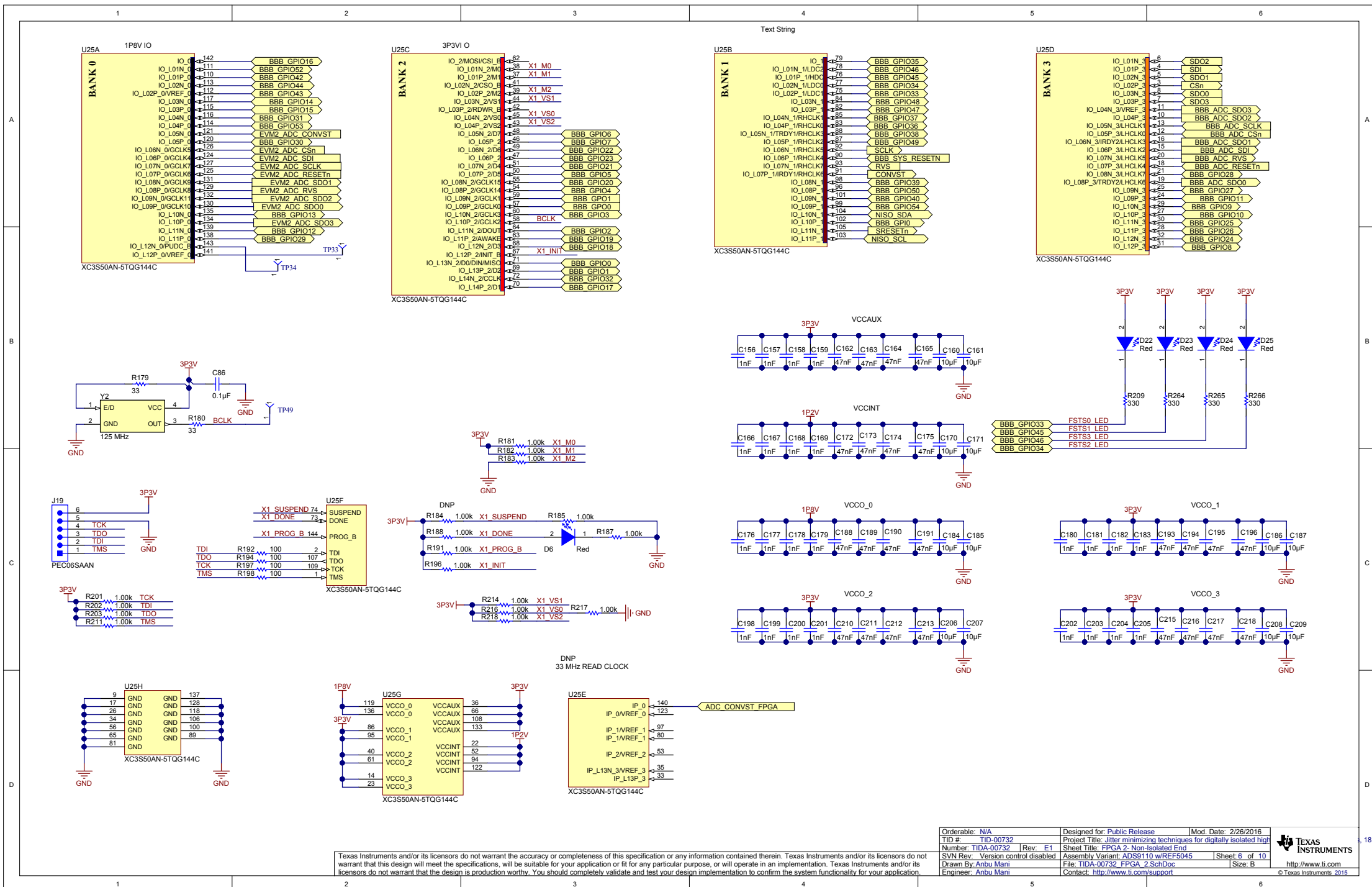


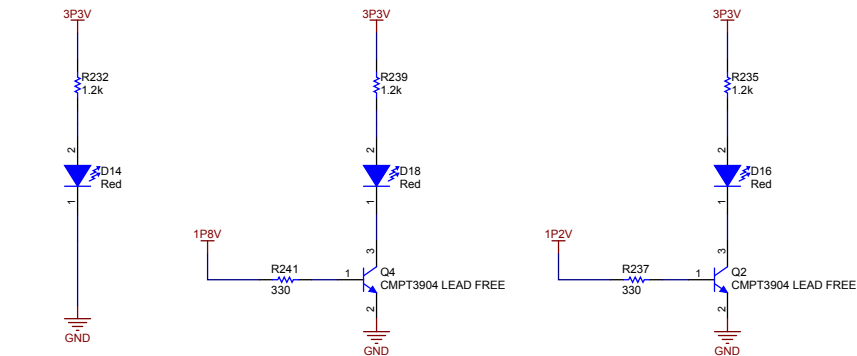
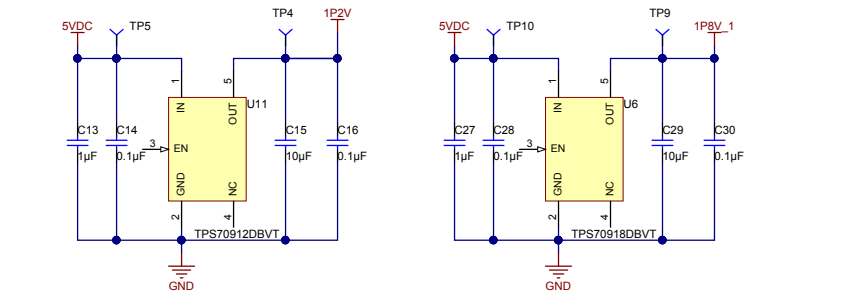
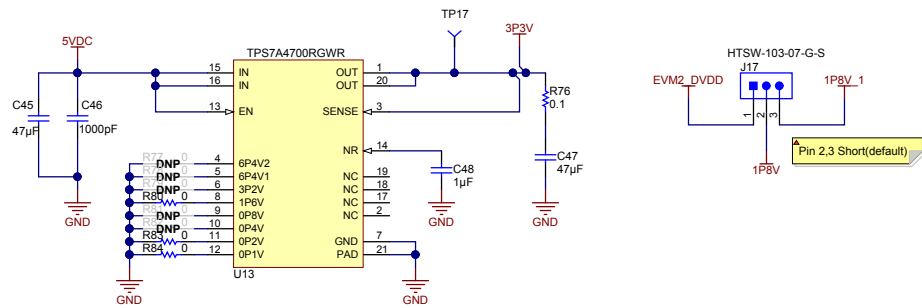


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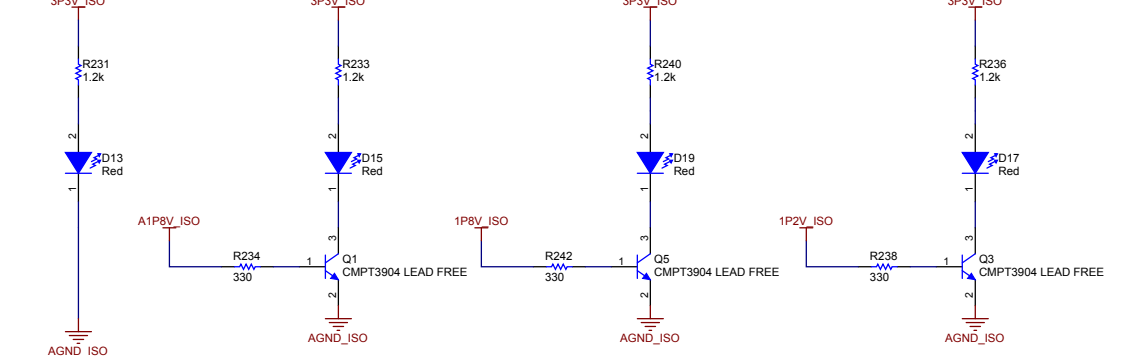
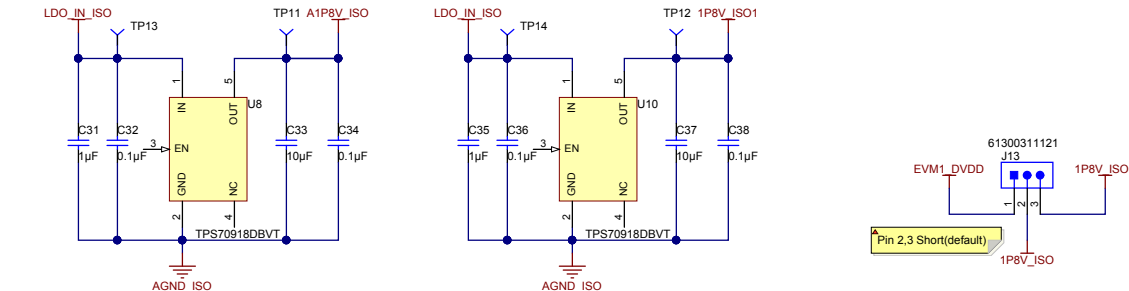
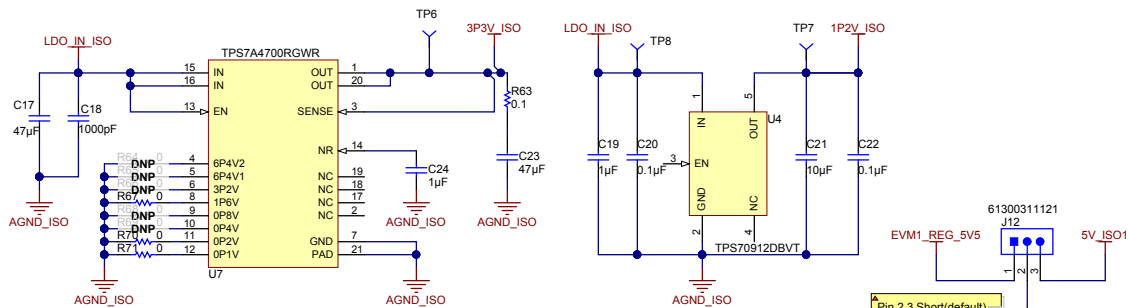
Orderable: N/A	Designed for: Public Release	Mod. Date: 2/27/2016
TID #: TIDA-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: Analog Front End & ADC
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 4 of 10
Drawn By: Anbu Mani	File: TIDA-00732_ADC_SchDoc	Size: B
Engineer: Anbu Mani	Contact: http://www.ti.com/support	http://www.ti.com
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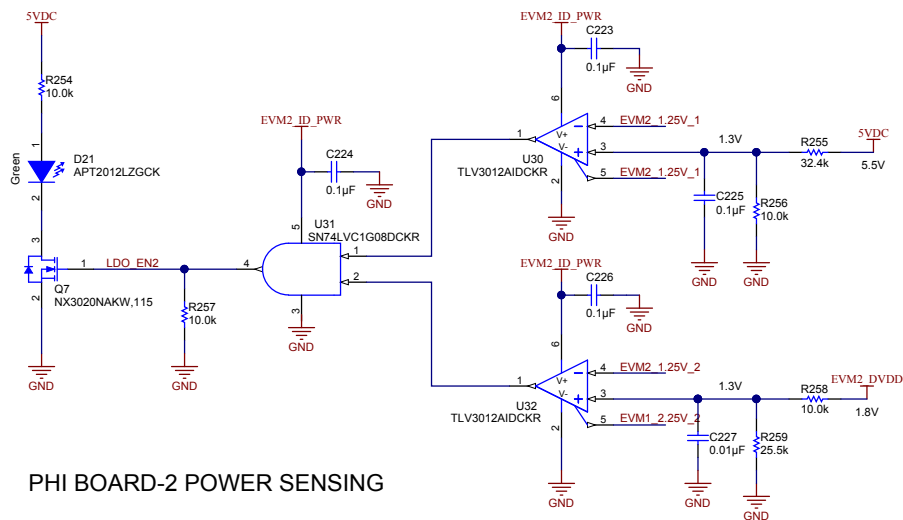
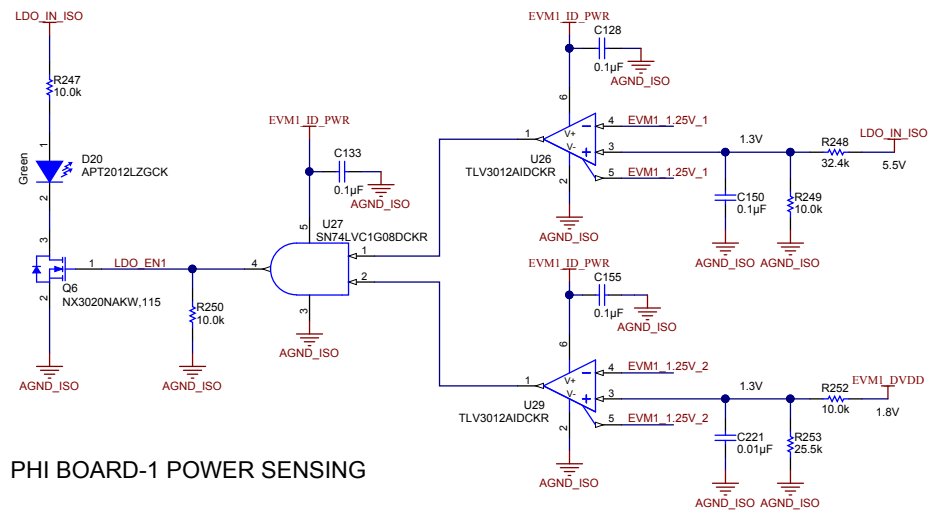
NON-ISOLATED POWER RAIL



ISOLATED POWER RAIL

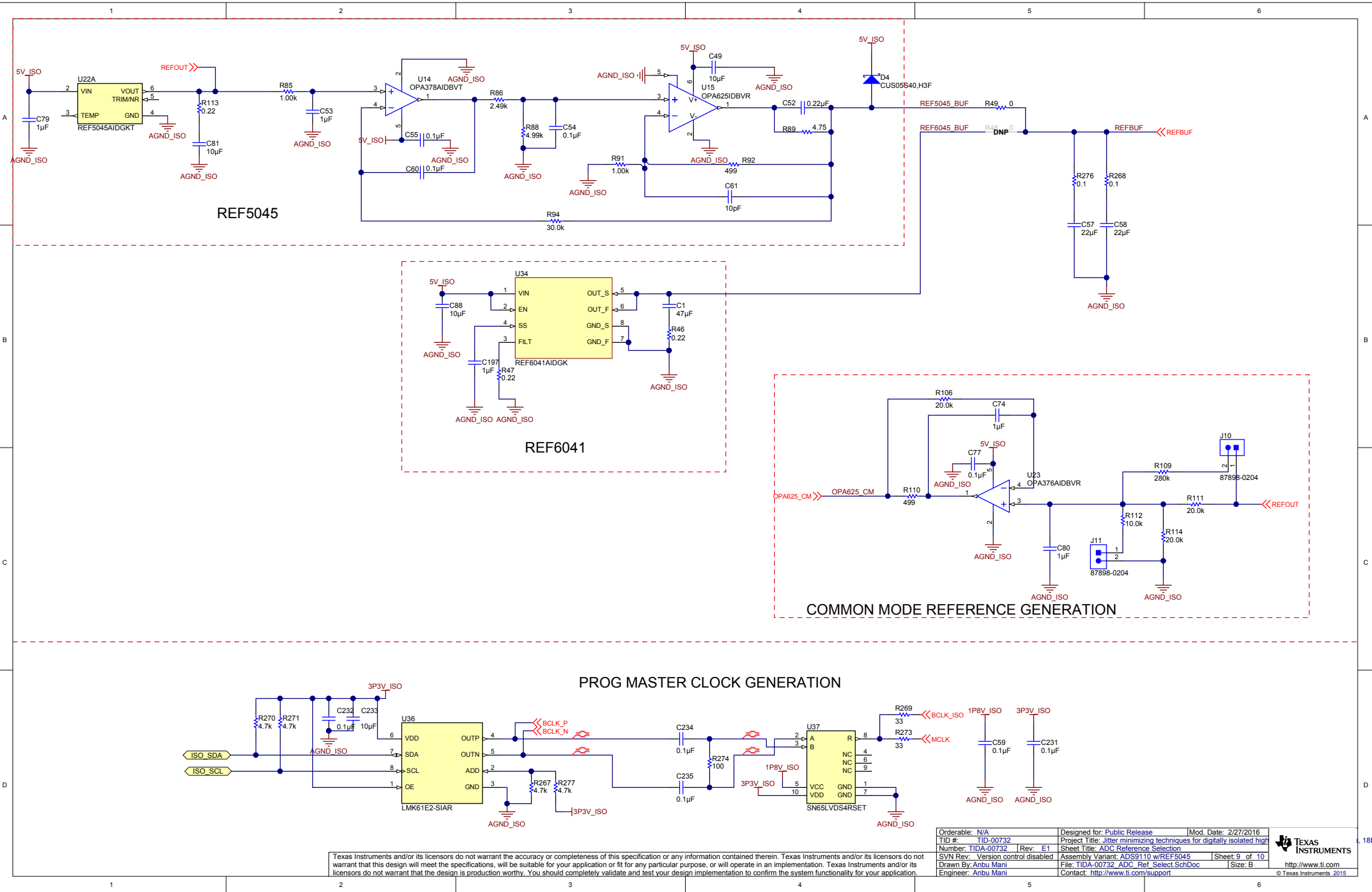
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TID #: TID-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: LDO's Isolated & Non Isolated
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 7 of 10
Drawn By: Anbu Mani	File: TIDA-00732_Pwr_SchDoc	Size: B
Engineer: Anbu Mani	Contact: http://www.ti.com/support	http://www.ti.com
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Orderable: N/A	Designed for: Public Release	Mod. Date: 2/27/2016
TID #: TID-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: Power Sense - PH1 & PH2 Interface
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 8 of 10
Drawn By: Anbu Mani	File: TIDA-00732_Pwr_Sense_SchDoc	Size: B
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Orderable: N/A	Designed for: Public Release	Mod. Date: 2/27/2016
TID #: TID-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: ADC Reference Selection
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 9 of 10
Drawn By: Anbu Mani	File: TIDA-00732_ADC_Ref_Select.SchDoc	Size: B
Engineer: Anbu Mani	Contact: http://www.ti.com/support	http://www.ti.com
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DNP FID1 DNP FID2 DNP FID3 FID4 FID5 FID6 FID7 FID8

PCB Number: TIDA-00732
PCB Rev: E1

PCB
LOGO
Texas Instruments

LBL1
PCB Label
Size: 0.65" x 0.20"

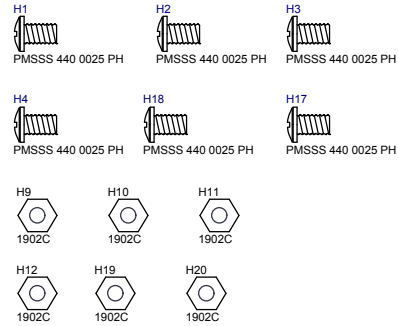
ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

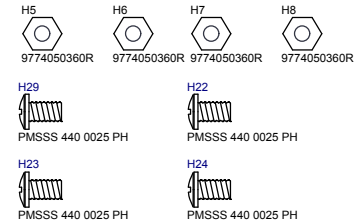
ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

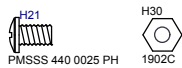
For Corner Mounting



For PHI1 Mounting

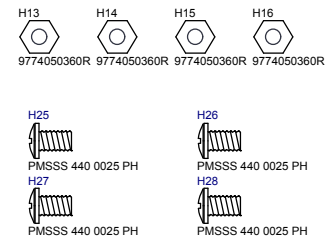


For Beagle Bone Block Mounting



For PHI2 Mounting

EVM2 mounting



Label Table	
Variant	Label Text

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Orderable: N/A	Designed for: Public Release	Mod. Date: 2/27/2016
TID #: TID-00732	Project Title: Jitter minimizing techniques for digitally isolated high	
Number: TIDA-00732	Rev: E1	Sheet Title: Fasteners
SVN Rev: Version control disabled	Assembly Variant: ADS9110 w/REF5045	Sheet 10 of 10
Drawn By: Anbu Mani	File: TIDA-00732_TID_Hardware.SchDoc	Size: B
Engineer: Anbu Mani	Contact: http://www.ti.com/support	http://www.ti.com

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