TI Designs

Optical Front-End System Reference Design

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Design Resources

TIDA-00725	Design Folder
OPA857	Product Folder
THS4541	Product Folder
ADC34J45	Product Folder
ADC34J45EVM	Product Folder
TINA-TI™	Tools Folder
HSDC PRO	Tools Folder

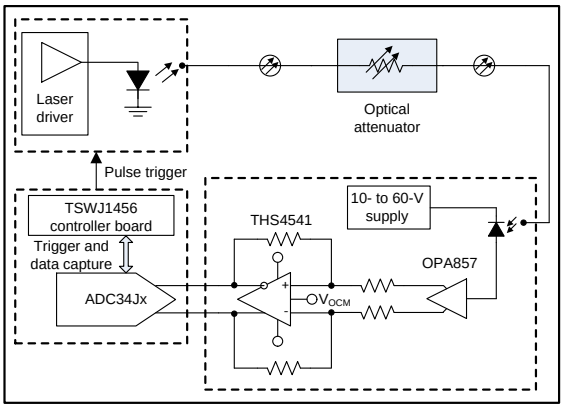
TI E2E™ Community — ASK Our E2E Experts

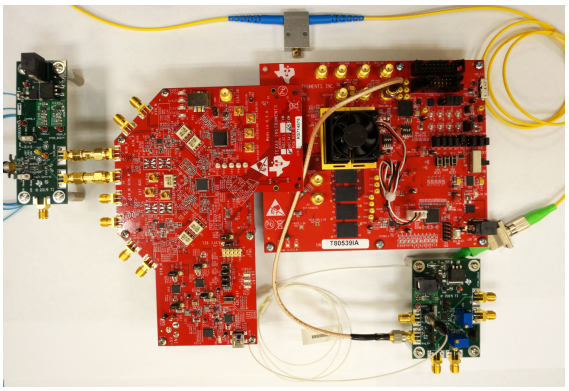
Design Features

- Optical Front-End Design With Demonstrated System Performance
- High-Speed Amplifier Signal Path With Bandwidth Greater Than 120 MHz
- High-Speed 14-Bit ADC With JESD204B Interface
- Ultrafast Laser-Diode Driver and Laser Diode to Generate Tx Signal
- Avalanche Photodiode (APD) Front-End With Onboard High-Voltage Supply
- High-Speed Transimpedance Amplifier for I-to-V Conversion
- A Fully Differential Amplifier (FDA) to Drive the ADC
- Flexibility to Easily Change Components in the Optical, Amplifier, or Data-Converter Signal-Path

Featured Applications

- OTDR
- Optical Amplifiers
- CAT-Scanner Front Ends
- Photodiode Monitoring
- Machine Vison
- Distance Measurement
- Missle Guidance
- 3D Scanning





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1 Key System Specifications

Parameter	Specification
Supply voltage	5-V external supply
Analog bandwidth	120 MHz
ADC sampling rate	160 MSPS
Maximum system gain	100 kΩ
Programmable transimpedance gain	5 kΩ/20 kΩ
Maximum signal swing	1 V_{PP}
Noise performance	≥ 60-dB SNR
Averaged noise performance	< 10-μV_{RMS}

2 System Description

Figure 1 is a detailed block diagram of the evaluation system and subblocks. The system is an interface of the following four different PCBs.

- Laser-diode driver + laser-diode board
- Amplifier signal-chain board
- ADC34J45, analog-to-digital converter (ADC) board
- TSW14J56 digital-capture board

A high-speed laser driver pulses the laser diode that transmits an optical pulse through the fiber. The optical attenuator controls the strength of the optical pulse incident on the photo-diode without changing the operating point of the laser diode or its driver. A high-speed photodiode placed in close proximity to the transimpedance amplifier converts the optical energy into an output current. The transimpedance amplifier converts the current into a pseudo-differential output voltage. The subsequent fully differential amplifier (FDA) stage converts the signal to a fully differential signal and level-shifts the output common-mode to match the ADC. The FDA drives the ADC through a doubly terminated 50-Ω resistor.

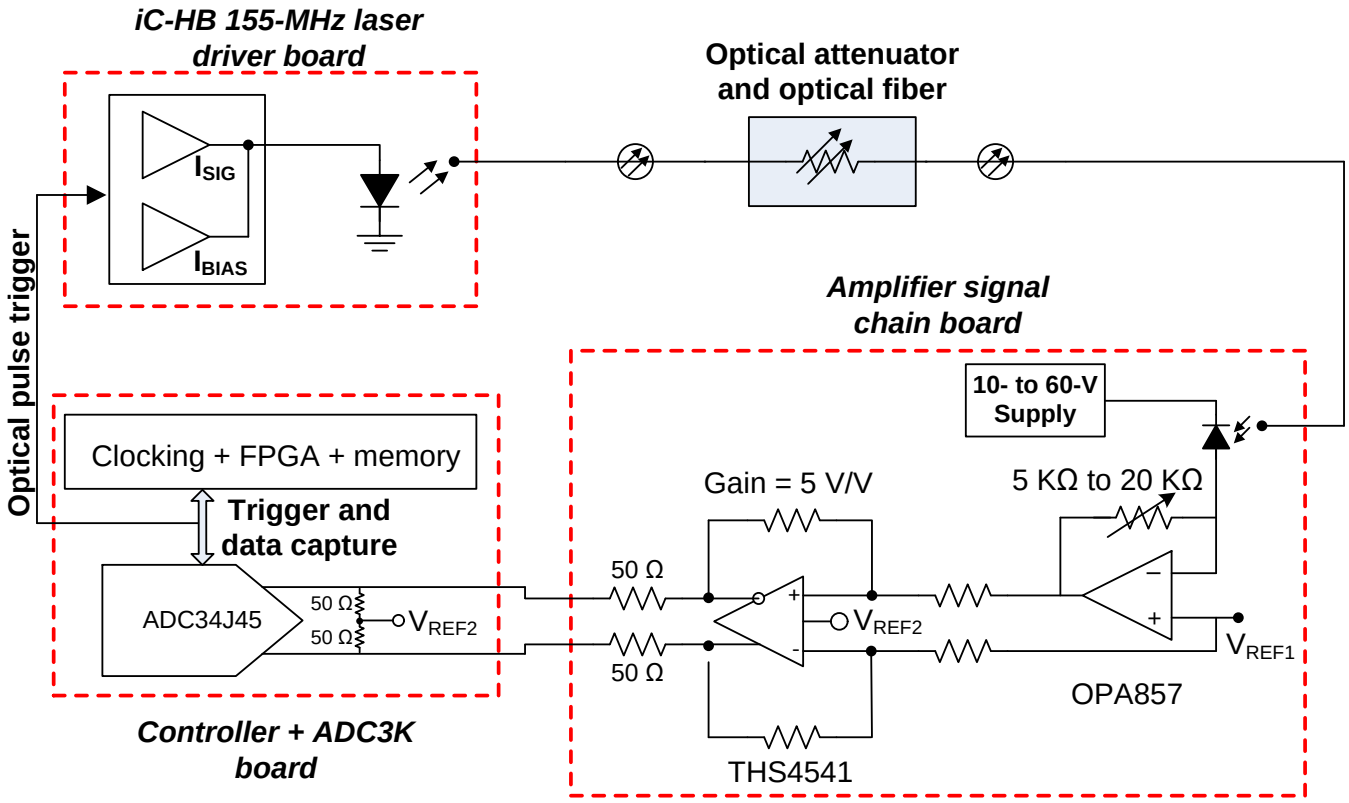

Figure 1. Block Diagram of System for Evaluation

The TSW1456 digital-capture board generates triggers to pulse the laser diode while simultaneously sending a signal to the ADC to convert data. The firmware allows multiple triggers with a programmable repetition rate. The firmware can also control the time-delay between the trigger that fires the laser and the trigger to the ADC that converts data. The ADC results are buffered into memory and the average result is computed on the PC. In test and measurement systems such as optical time-domain reflectometry (OTDR), this averaging feature can lower the noise floor of the entire system, which improves SNR. The system block diagram in Figure 1 is a loop-back system to enable evaluation of the electrical signal chain in a controlled environment.

2.1 OPA857 Transimpedance Amplifier

The OPA857 is a high-bandwidth, programmable gain, integrated-transimpedance amplifier (TIA). Standard operational amplifiers have a gain-bandwidth relationship, where bandwidth decreases as gain is increased. In the case of the OPA857, switching the transimpedance gain also changes the internal compensation of the amplifier. The closed-loop bandwidth does not follow convention and optimizes the bandwidth of amplifiers.

The OPA857 also has a pseudo-differential output that makes it easier to interface to the subsequent FDA stage. The pseudo-differential output also reduces the common-mode noise of the TIA stage. The OPA857 close to the photodiode on the amplifier signal-chain board minimizes parasitic capacitance. The board is powered off a 5-V DC supply, which is plugged into the AC mains. A TPS79901 adjustable-linear regulator converts the 5-V input into a 3.3-V output that drives the OPA857. The output common-mode of the OPA857 is V_{CC} × 5/9 = 1.83 V. The photodiode is biased and only sources an output current, which is important because the OPA857 output is optimized to swing less than its common-mode voltage. For more information, see Figure 2.

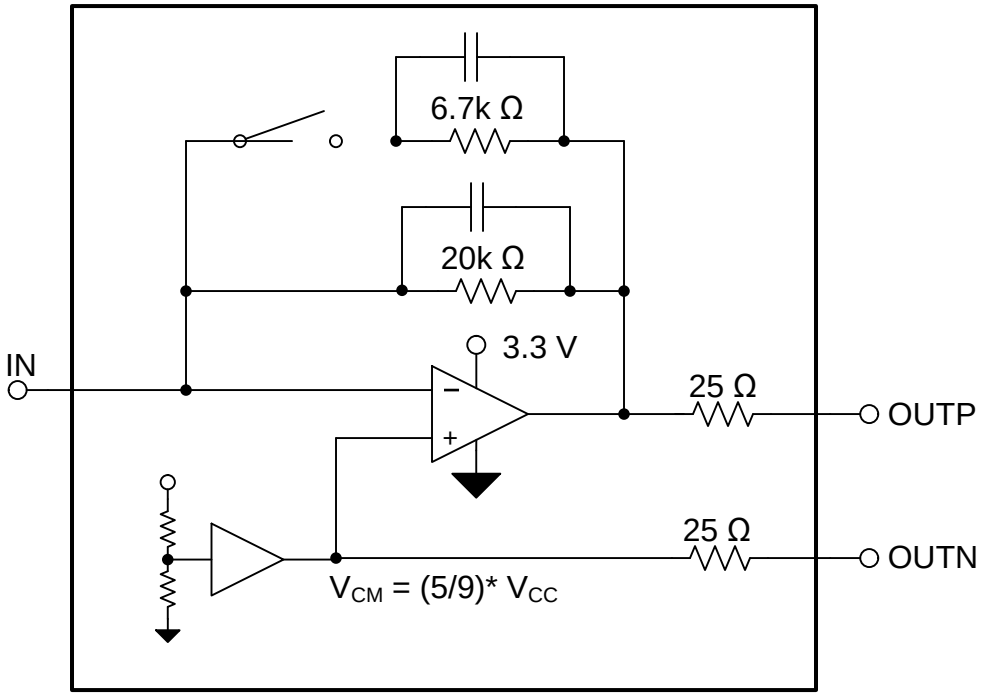

Figure 2. OPA857 Transimpedance Amplifier

2.2 THS4541 Differential-Amplifier Stage

The THS4541 is a high-bandwidth, low-noise FDA used to provide additional gain to the output of the TIA stage. The THS4541 also converts the pseudo-differential output of the OPA857 into a fully differential signal to drive the next ADC stage. The THS4541 level-shifts the output common-mode of the OPA857 to match the specified input common-mode of the ADC. An onboard resistor divider connected between the FDA power supply and GND sets the output common-mode of the THS4541. The FDA stage is powered by 3.3 V from its TPS79901 linear regulator. The THS4541 is configured in a gain of 5 V/V, which results in an estimated closed-loop bandwidth of 170 MHz.

Increasing the closed-loop gain increases the phase margin of the amplifier and reduces the overshoot to a pulsed input. A smooth-settling transient response reduces blind-spots and other test artifacts in applications like OTDR systems. Increasing the R_G value improves the response of the OPA857 because the bandwidth of the OPA857 decreases as the output loading is reduced. The gain resistor (R_G) forms the output load of the OPA857. A large value of R_F drives up the value of R_G, which reduces the output load on the OPA857.

A large R_F may reduce the phase-margin of the amplifier. The feedback resistance with the input capacitance of the amplifier creates a zero in the noise-gain response of the amplifier. This zero can reduce the phase-margin. Add an appropriately sized feedback capacitance (C_F) in parallel with R_F to compensate for the zero in the noise-gain response. The combination of R_F and C_F creates a pole in the response. The pole in the response helps shape the final closed-loop response of the amplifier.

The FDA and ADC are on separate PCBs connected through SMA connectors. The placement of the FDA and ADC creates some physical separation between the two devices and a suboptimal layout. To reduce the effects of reflections, each output of the THS4541 is doubly terminated with 50-Ω resistors. Because the THS4541 is doubly terminated with 50-Ω resistors, the 6-dB output attenuation reduces the overall amplifier gain to 2.5 V/V. In a dedicated single-board system, the THS4541 and ADC34J45 can be placed close to each other to remove the requirement for the output termination.

Another effect to consider is the output swing of the THS4541. In standard CW applications, each output of the FDA swings symmetrically about its output common-mode with equal magnitude and opposite phase. In the case of a transimpedance application, the photo-diode can either source or sink current results in a unipolar output swing from the transimpedance amplifier stage. When the output signal is applied to the FDA stage, each output swings either higher or lower than its common-mode using only half the available swing of the amplifier. The ADC also uses only half its available signal swing. For more information, see Figure 3.

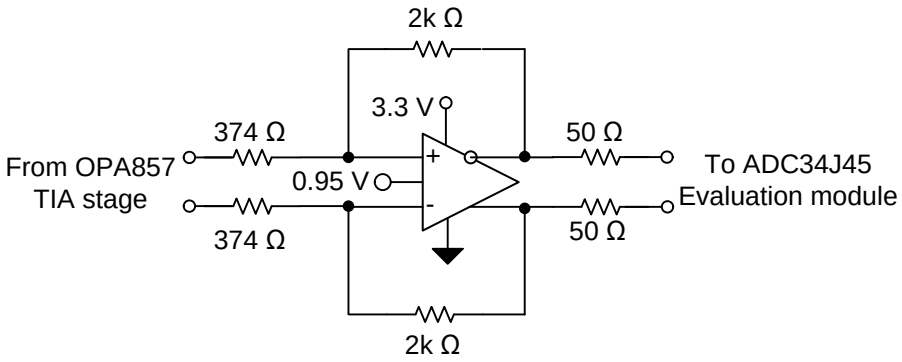

Figure 3. THS4541 FDA Block Diagram

2.3 ADC34J45 High-Speed ADC

The ADC34J45 is a highly linear, low-power, 14-bit ADC that can sample at up to 160 Msps. To accommodate many different applications, this family of devices comes in configurations that include dual or quad channels, 12 bits or 14 bits, and sample rates from 50 to 160 Msps. The JESD204B data interface allows a simple, flexible SERDES interface to many FPGAs and processors. This device also supports JESD204B subclasses 0, 1, and 2. The support for these subclasses provides various options for synchronizing the multiple devices in phased-array applications.

With an input range of 2 V_{pp}, SNR of 72 dBFS, and SFDR greater than 86 dBc, TI designed the ADC34J45 family for demanding high-frequency signals with a large dynamic range. A 3-dB input bandwidth of 450-MHz enables this device to subsample systems with frequencies up to three times greater than the maximum sample rate. In this application, a 14-bit ADC channel digitizes a repetitive, synchronous optical pulse. For more information, see Figure 4 and Figure 5.

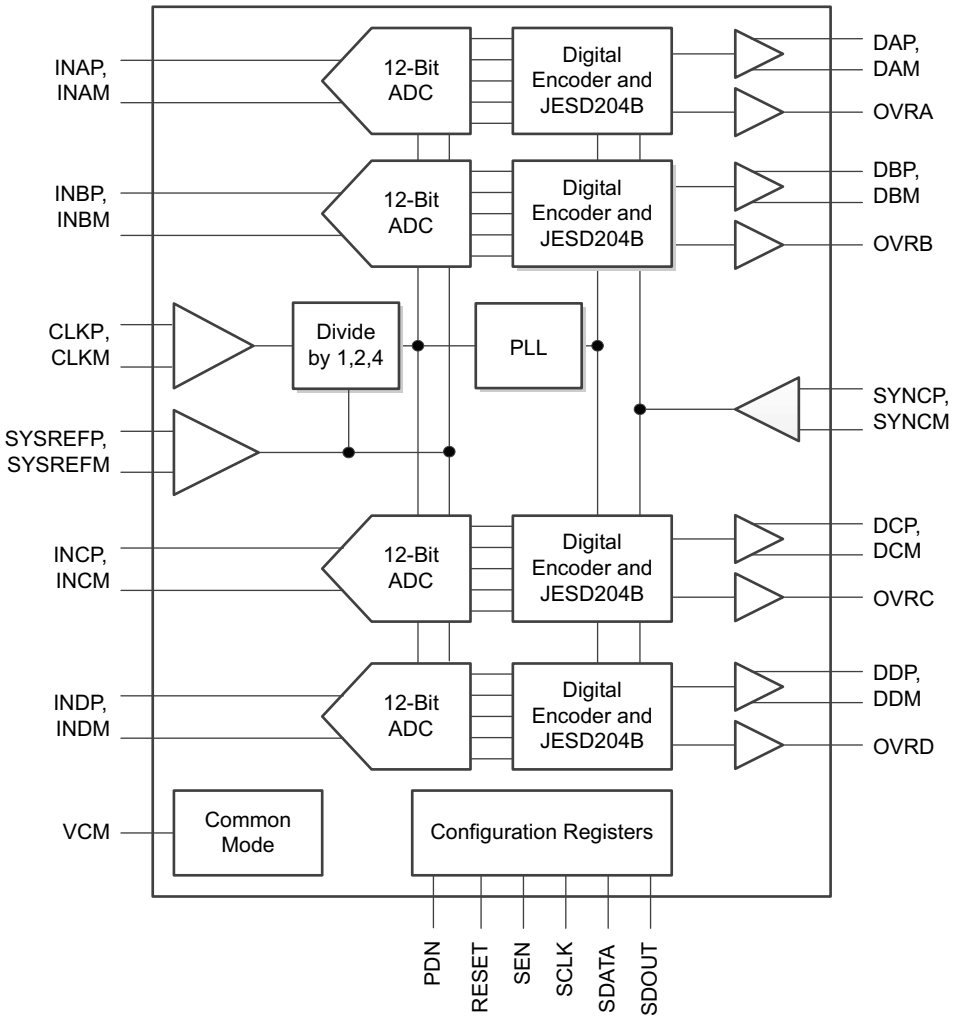

Figure 4. ADC34Jxx Functional Block Diagram

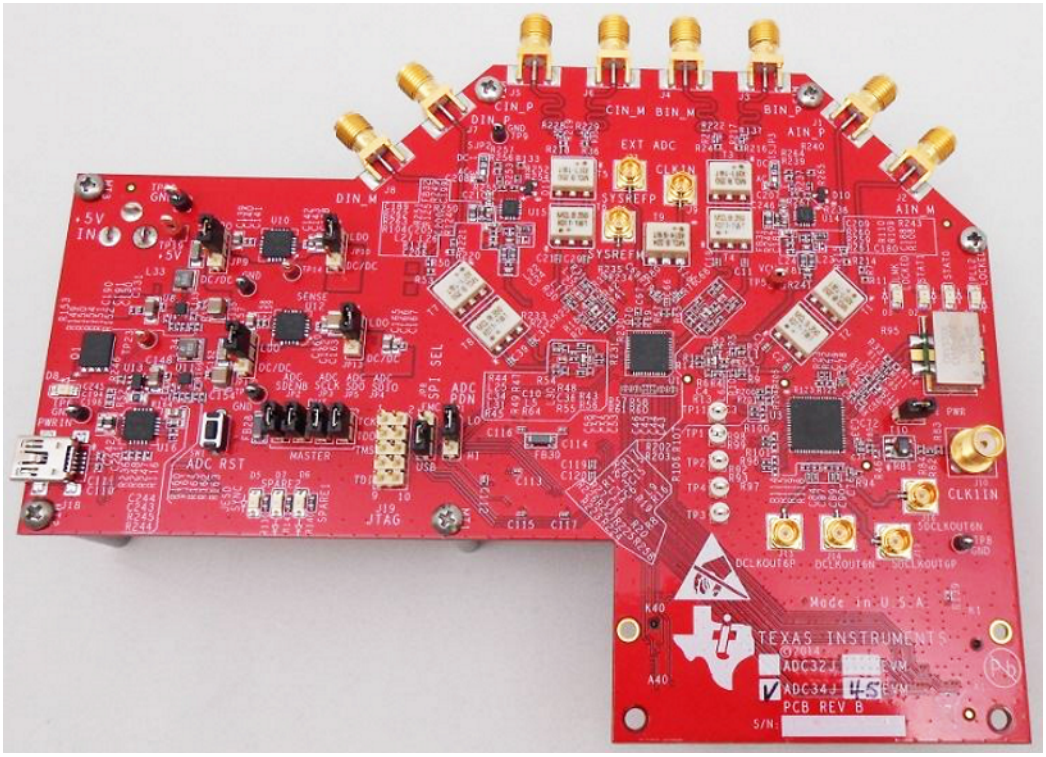

Figure 5. ADC34J45EVM Top View

2.4 TSW14J56 Digital-Capture Board

The TSW14J56 is an FPGA-based digital-capture card for ADCs that uses the JESD204B digital interface. The TSW14J56 provides up to 10 lanes running at 12.5 Gbps to support the fastest converters that use a JESD204B interface. The board has 2 Gsamples of memory in which to store samples from the ADC. The USB3.0 interface on this capture platform enables fast data transfers from the sample memory.

HSDC Pro software controls the TSW14J56. This software lets you capture data from the ADC and process it in the time domain or frequency domain using a fast Fourier transform (FFT). The TSW14J56 captures more than 10,000 triggered ADC34Jxx conversions. These successive conversions are then extracted for averaging and further analysis. See Figure 6 and Figure 7 for more information.

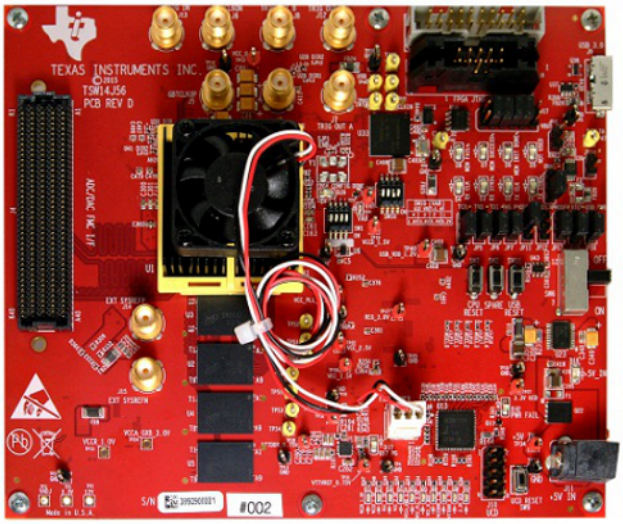

Figure 6. TSW14J56 Digital Capture Card

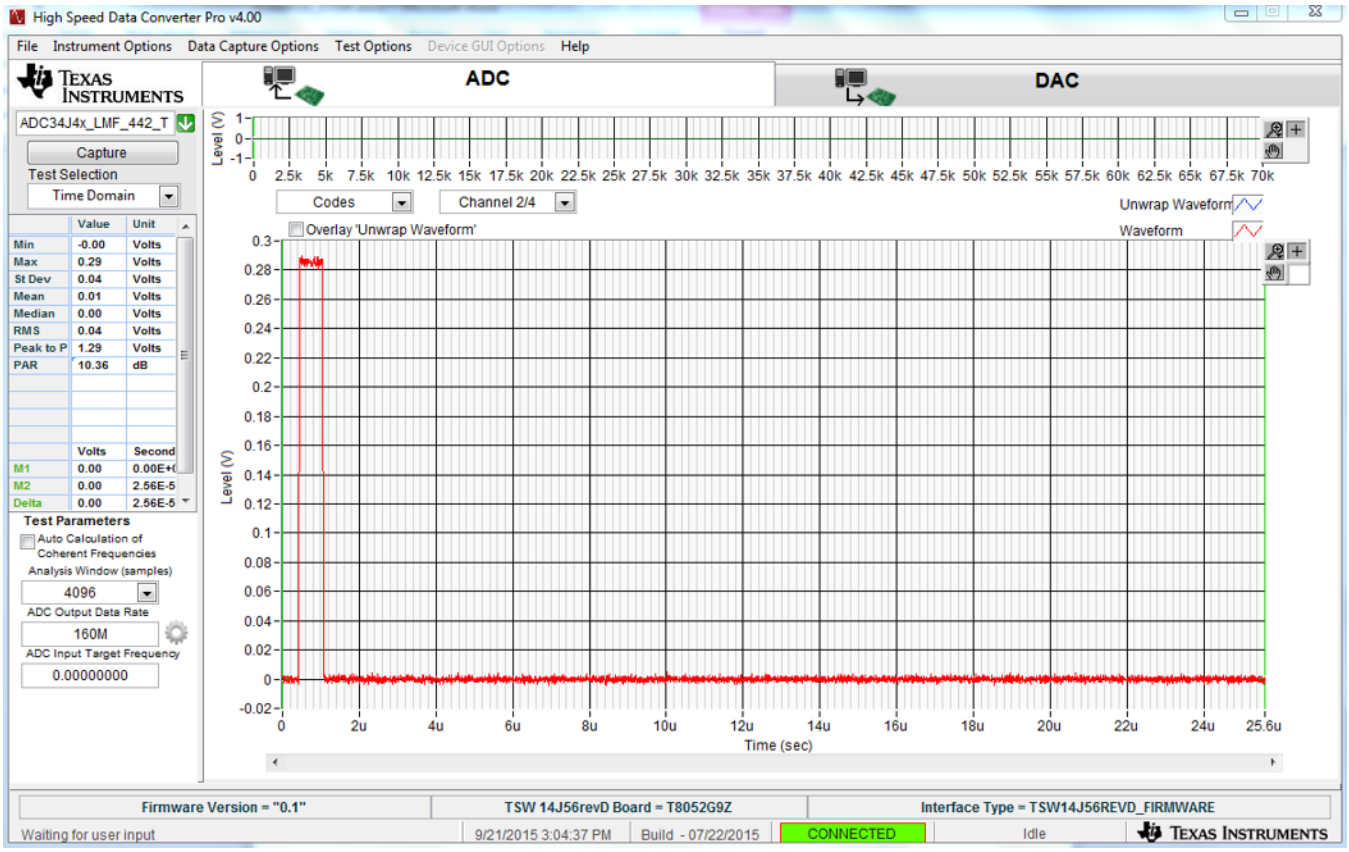

Figure 7. HSDC Pro Software GUI

2.5 Optical Components

2.5.1 Laser Driver and Laser Diode

The laser-diode driver and laser diode are on a separate PCB with a 5-V supply. The laser driver is an iC-HB, 155-MHz triple-laser switch from iC-Haus. See Laser-Diode Driver, iC-HB datasheet for the data sheet for the laser driver. The laser diode is a 1550-nm DFB LDM5S515-015. In a pulsed high-speed application, toggling a laser on and off causes suboptimal performance. Rather than turning the laser off, configure the laser just less than its turnon threshold when it is inactive to ensure a smoother and quicker turnon. This configuration minimizes the effects of parasitic capacitances that require charging and discharging during transient operation.

Figure 6 shows a simplified schematic of the laser setup. See Figure 15 for the complete PCB schematic. Consider each channel of the laser-diode driver a voltage-controlled current source (VCCS) with an enable and disable switch. The three parallel channels are as follows:

- The bias channel sets the laser at its threshold condition.
- Channel 1 drives the signal current that toggles the laser on or off.
- Channel 2 is unused in this application.

Using the onboard resistor divider and potentiometer subcircuit connected between the 5-V supply and ground, set the bias voltage to control the VCCS. Set the bias supply to 1.15 V and the signal supply on channel 1 to 1.65 V. Use the jumper to statically control the bias channel state, while the trigger generated by the TSW14J56 controls the signal channel. The adjustable linear regulator (U3) is configured to drive an output voltage of 1.8 V on the VDIG line. This voltage drives the primary side of the SN74LVC1T45 logic-level translator to shift the 0- to 1.8-V logic level from the trigger signal of the TSW14J56 to a 0- to 5-V digital signal required to drive the iC-HB chip. For more information, see Figure 8.

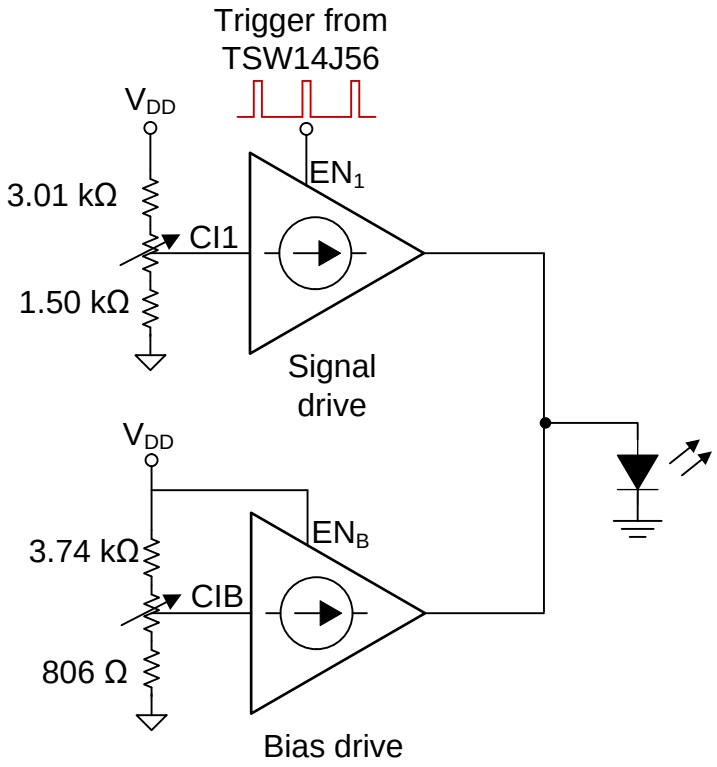

Figure 8. Laser Diode Block Diagram

2.5.2 Photodiode

TI used a low-voltage InGaAs photodiode (NR-7500) and high-voltage avalanche photodiode (NR8300) to evaluate the system. TI used an LT3995-integrated APD supply to bias the photodiodes. The LT3995 can supply a bias voltage from 10 to 60 V. This range covers the operating range of both photodiodes during evaluation.

3 Simulations

3.1 Noise Simulation

Figure 9 shows the schematic that simplifies the noise of the amplifier signal chain. A current source in the circuit represents the photodiode.

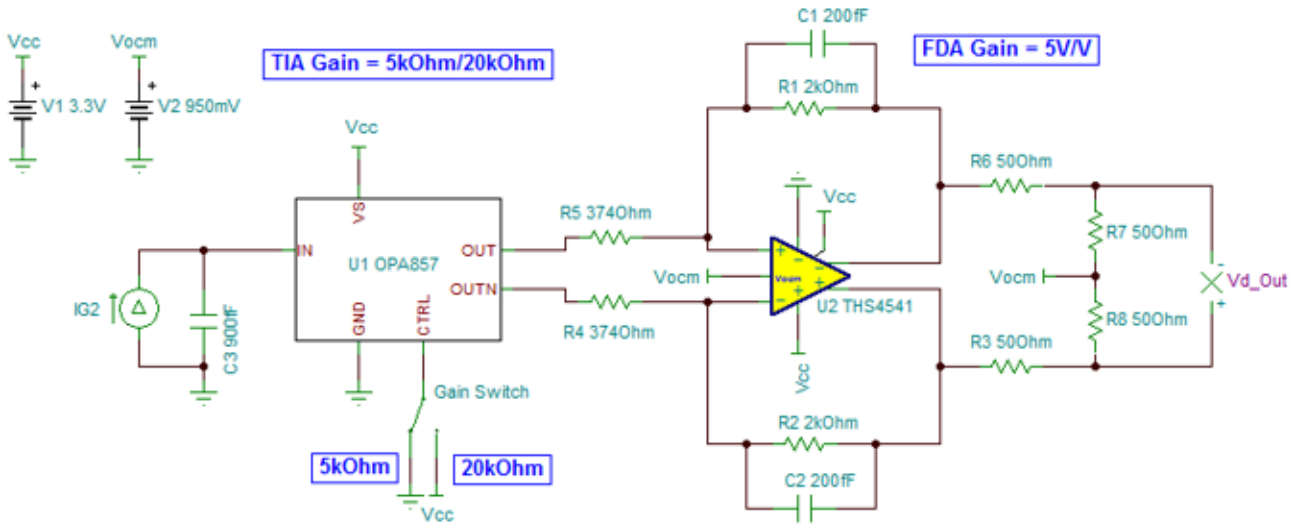

Figure 9. TINA Schematic For Noise Simulation

Figure 10 shows the output noise of the amplifier system measured at the Vd_Out node. The total simulated output noise for the 5-kΩ and 20-kΩ transimpedance-gain setting is 303 μV_{RMS} and 888 μV_{RMS}, respectively, assuming a 135-MHz brick-wall filter. The 900-fF capacitance is an estimate of the sum of the diode capacitance, PCB parasitic capacitance, and diode package parasitic capacitance.

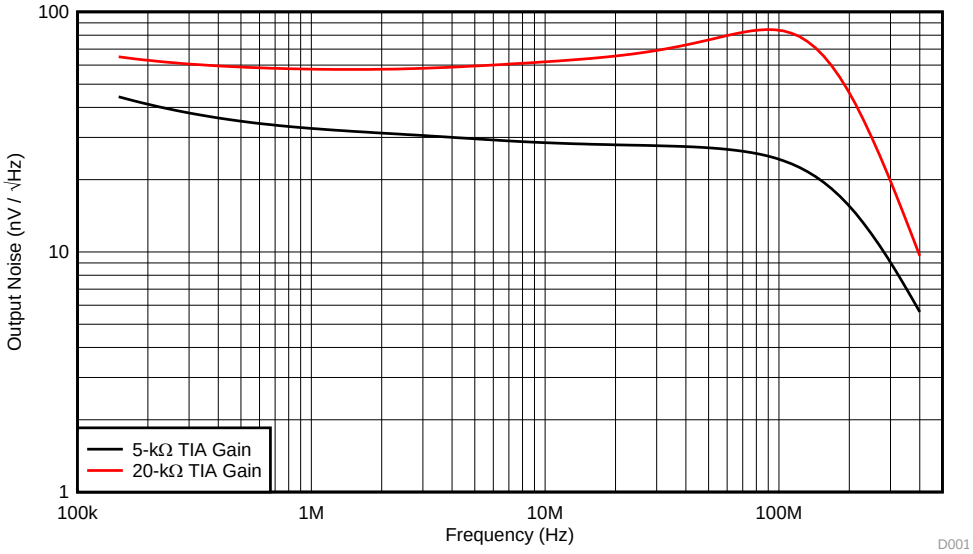

Figure 10. Simulated Output Noise of the Amplifier Chain

3.2 THS4541 Loop-Gain and Phase Margin Simulation

To get a pulse-response with minimal overshoot and ringing on the rising and falling edges of the pulse, the phase-margin of the FDA circuit must be greater than 70°. To simulate the loop-gain of the THS4541, use the circuit in Figure 11. The voltage-controlled voltage source (VCVS1) converts the single-ended source signal into a full-differential output that subsequently drives the inputs of the amplifiers.

To measure loop-gain, break the loop of the amplifier at its summing-junctions. The differential input signal drives the inputs of the amplifier forward through C1 and C2, and the L1 and L2 inductors isolate the feedback signal from the amplifiers input pins and the source. This method is similar to the loop-gain analysis in single-ended operational amplifiers. C3 and C4 show the approximate parasitic capacitance in the amplifiers feedback path. C_diff models the input common-mode and differential capacitance of the amplifier because the actual input capacitance of the amplifier has been isolated from the feedback network due to the inductors.

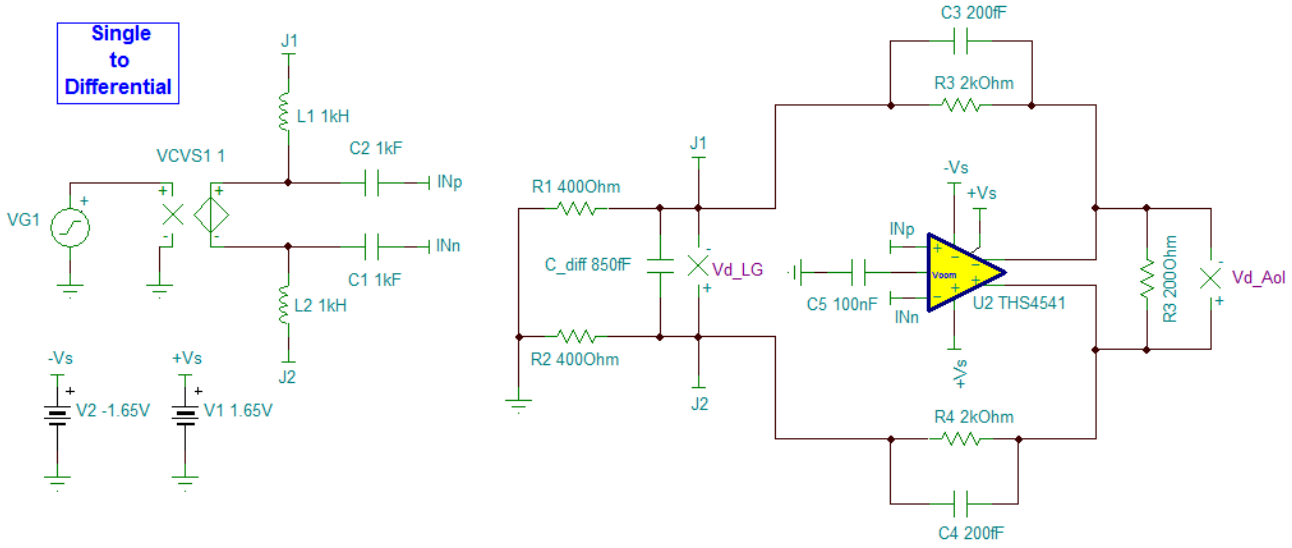

Figure 11. THS4541 Loop-Gain Analysis TINA Schematic

The simulated loop-gain magnitude and phase plotted in Figure 12 predict a phase-margin of approximately 79°. Control-loop theory estimates the pulse-overshoot for 79° of phase-margin to less than 0.001%. The simulated closed-loop bandwidth of the FDA circuit is 150 MHz.

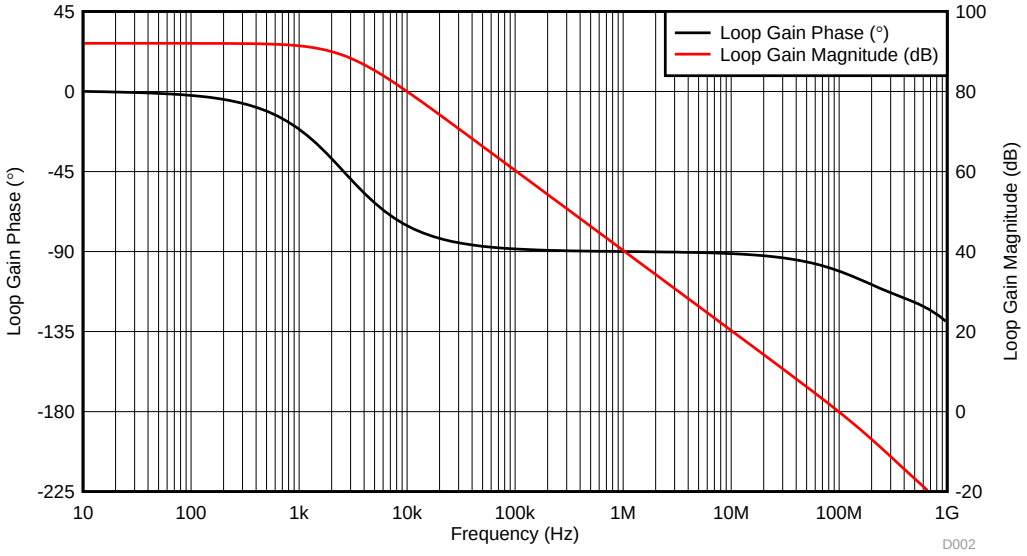

Figure 12. Simulated Loop Gain of THS4541

4 PCB Schematic and Layout

Figure 13 and Figure 15 show the PCB layout and schematic for the laser-driver board. Section 9.1 contains the bill of materials (BOM). Minimize trace lengths to reduce parasitic trace resistance and capacitance. Match the trace lengths wherever possible. To create low-impedance paths from the ICs to their respective power supplies, place bypass capacitors close to the supply pins of the amplifiers, laser driver, and APD supply.

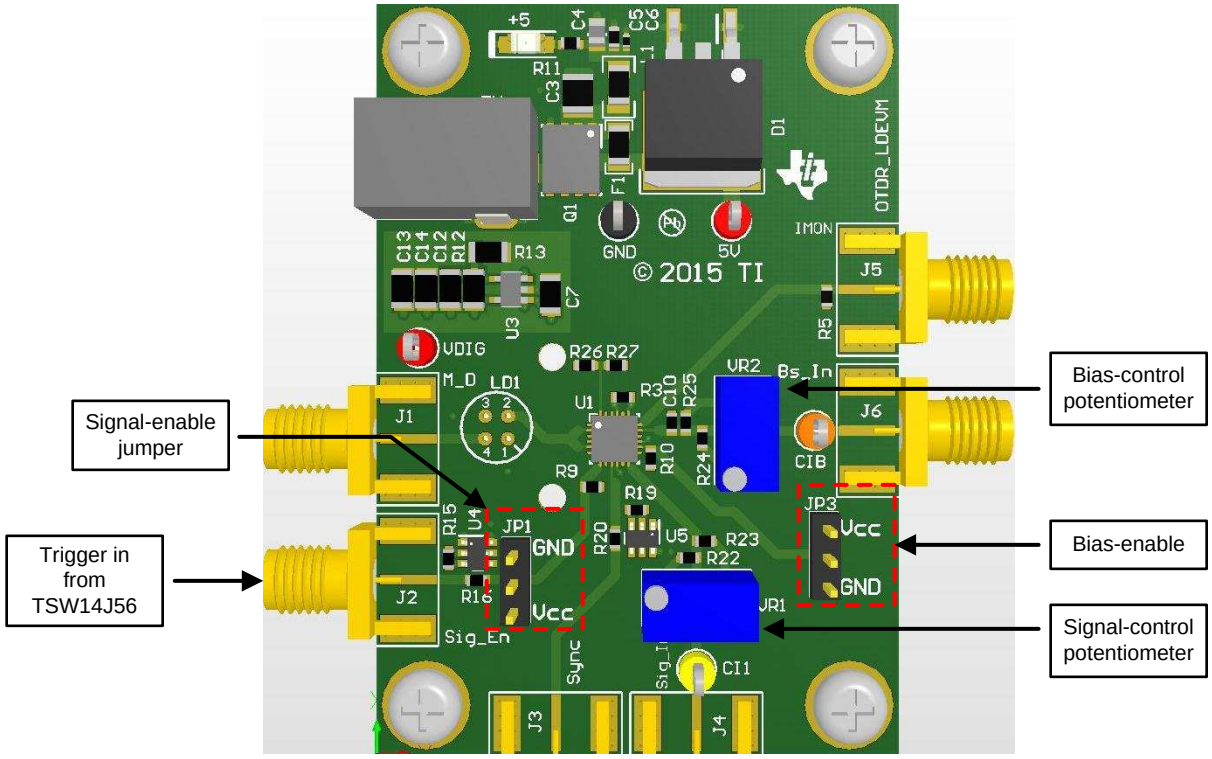

Figure 13. Laser-Driver Circuit PCB

Figure 14 and Figure 16 show the PCB layout and schematic for the signal-driver board. The amplifier signal chain occupies 38.7 mm^2 of PCB area. This area includes the two amplifiers and the surrounding resistors and capacitors. Both the OPA857 and THS4541 are available in a 3-mm × 3-mm VQFN package. The area consumed by the amplifiers is 18 mm^2.

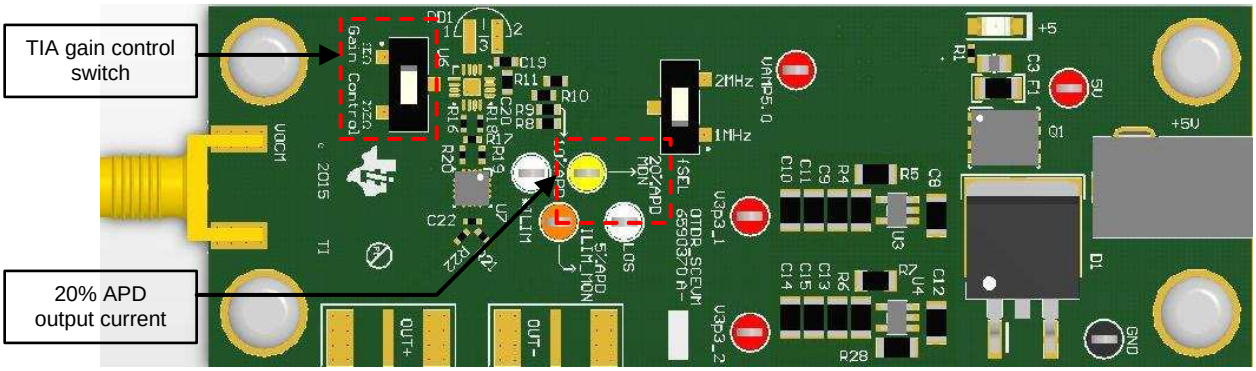

Figure 14. Signal-Chain Circuit PCB

4.1 Circuit Schematic

Figure 15 and Figure 16 show the circuit schematics.

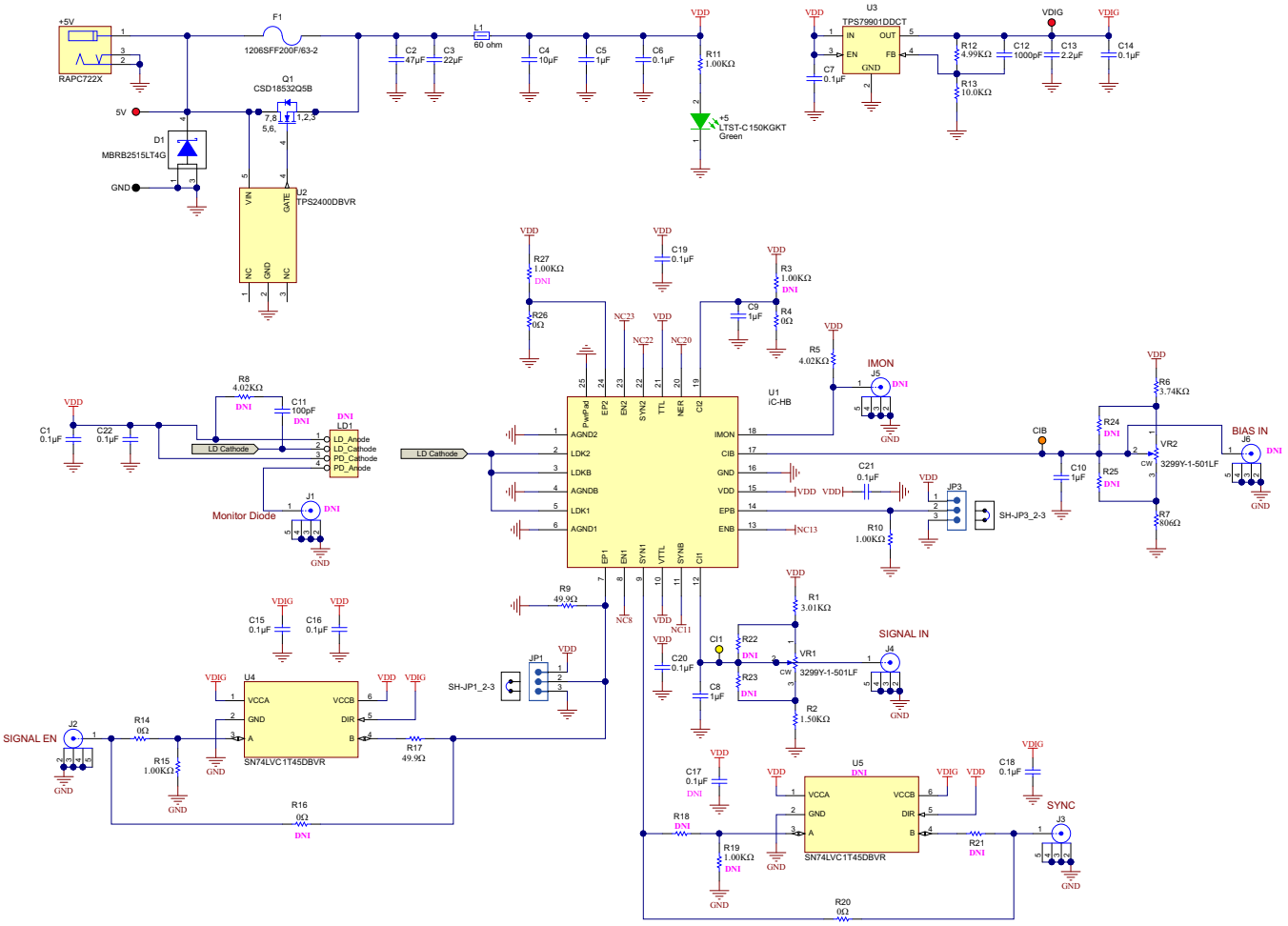

Figure 15. TIDA-00725 Laser-Driver Circuit Schematic

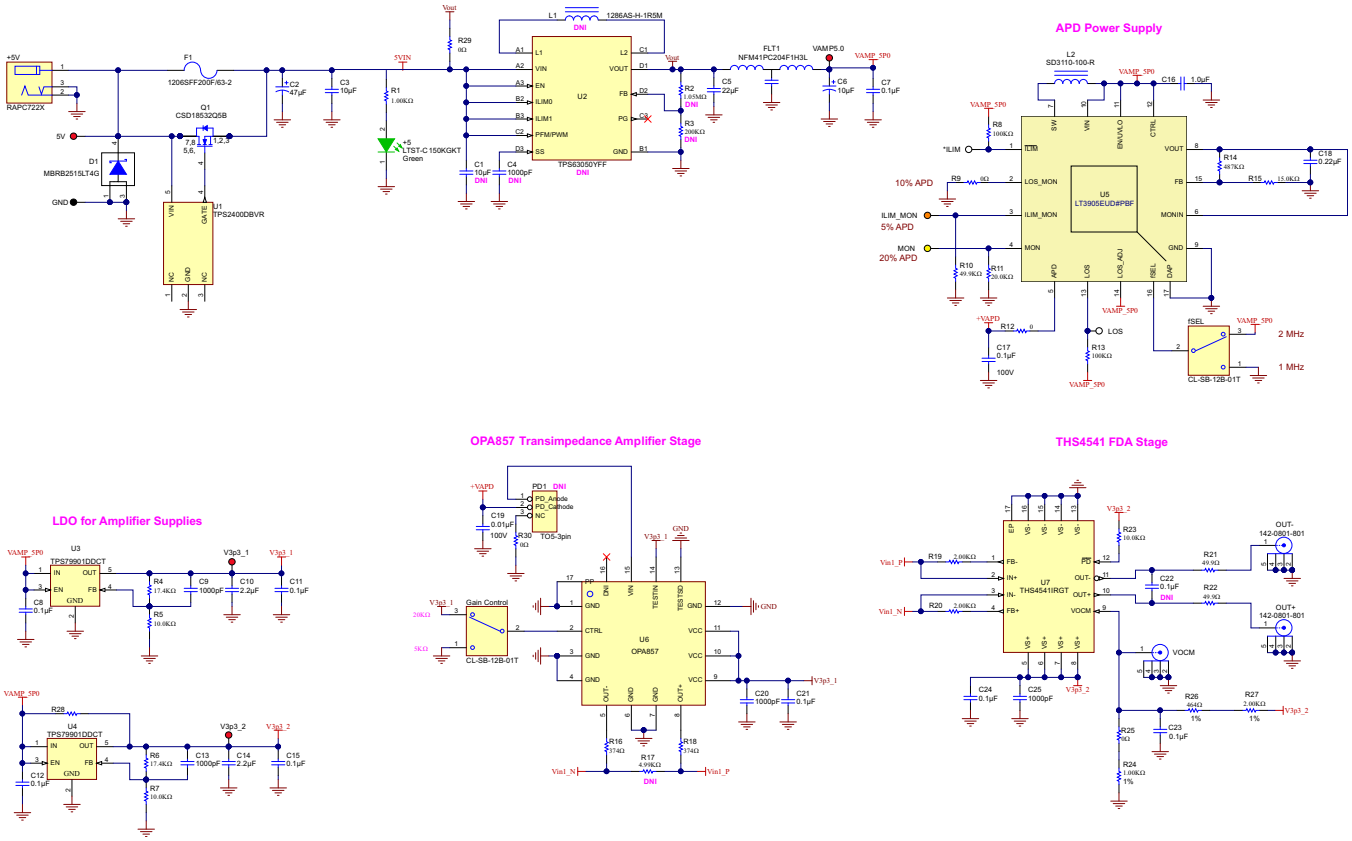

Figure 16. TIDA-00725 Signal-Chain Circuit Schematic

5 Getting Started–System Setup

To prevent damage to the sensitive optical components and ensure the software is operating in the correct mode, connect the 5-V supplies to the boards in the following order:

1. TSW14J56 and ADC3k
2. Laser driver
3. Amplifier signal chain

5.1 Laser-Driver Board Setup

1. Ensure jumpers JP1 and JP3 are grounded (JP2 is unused in this application).
2. Use the VR2 potentiometer to set the voltage on CIB (pin 17) to 1.15 V ±25 mV.

NOTE: This adjustment drives approximately 10 mA of current into the LDM5S515-015 laser diode. This current puts the laser diode at its lasing threshold.

3. Use the VR1 potentiometer to set the voltage on CI1 (pin 12) to 1.65 V ±25 mV.

NOTE: This adjustment drives approximately 40 mA of signal current into the laser diode.

4. Adjust the threshold and signal-bias voltages if using another laser diode.
5. Connect a short cable between J7 (TRIG OUT A) on the TSW controller board and J2 (SIGNAL EN) on the laser-driver board to trigger the lazer diode.
6. Use a short cable to minimize the delay between the ADC trigger initiating a conversion and the optical pulse generated by the laser.

7. Connect JP3 to VDD to set the laser at its threshold.

5.2 Signal-Chain Board Setup

Photodiode Protection: The APD power supply self-limits its output voltage if the voltage on the ILIM_MON pin exceeds 1.248 V. For this design, the maximum current through the photodiode is limited to 500 µA by tying a 100-kΩ resistor from ILIM_MON to GND. See the LT3905 data sheet (http://cds.linear.com/docs/en/datasheet/3905fa.pdf) for more details on this function.

1. Measure the output voltage on the IMON pin using a multi-meter to monitor the amount of input current into the OPA857 transimpedance stage.

NOTE: The IMON pin sources a current proportional to 20% of the photo-diode current for external current monitoring. Tie a 20-kΩ resistor from IMON to GND to set the gain of the circuit. Use Equation 1 to calculate the photodiode current.

$$I_{APD} = 5 \times \frac{V_{IMON}}{20\,k\Omega} \quad (1)$$

2. Use the fSEL switch to select the frequency of the internal clock of the APD power supply (TI performed this evaluation with f = 1 MHz; system performance was independent of the selected frequency).
3. Use the GAIN switch to set the transimpedance gain to 5 kΩ or 20 kΩ.
4. Connect the OUT– and OUT+ SMA connectors on the signal-chain board to the SMA connectors on the appropriate ADC3k channel.

NOTE: TI designed the connector spacing to be equal on the two boards to eliminate the need for cables thereby minimizing parasitics.

5.3 TSW14J56 + ADC3K Board and Software Setup

The ADC3k EVM accepts a single-ended signal that is converted to a differential signal using the onboard transformers. See Table 1 for a list of BOM changes required to modify the EVM to accept the differential output from the signal-chain board. The following changes are described for channel 2 of an ADC34J45 EVM.

HSDC Pro software (available at http://www.ti.com/tool/dataconverterpro-sw?keyMatch=hsdc pro software&tisearch=Search-EN-Everything) controls the system. The firmware to perform averaging and hardware-generated triggering is proprietary and unavailable for general use. For additional firmware information, contact the applications team at http://e2e.ti.com/support/amplifiers/high_speed_amplifiers/.

Table 1. BOM Modifications Required on ADC34J45 and Channel 2 to Accept Differential Input Signals

Reference Designator	Default State	Modified State
J4	DNI	Install
R21	DNI	Install 0-Ω resistor
R24	0 Ω	DNI
T3, T4	ADT1-1WT installed	Replace the transformers with a 0-Ω shunt across the terminals.
C11, C19	0.1 µF	Replace the capacitors with a 0-Ω shunt.
R16, R17	49.9 Ω	Replace the resistors with a 0-Ω shunt.
R19, R26	29.9 Ω	Replace the resistors with a 49.9-Ω shunt.
R20, R27	49.9 Ω	DNI

5.4 Setting Optical Power and Adjusting the Optical Attenuator

1. Keep the optical power output from the laser diode constant during evaluation in compliance with the settings in Section 5.1.
2. Turn the knob on the variable optical attenuator (VOA) clockwise for maximum attenuation.

NOTE: This adjustment ensures there is minimal optical power incident on the APD.

See Variable Fiber Optical Inline Attenuator for details on the optical attenuator.

3. Connect a multimeter to the IMON test point on the amplifier board.
4. Set jumper JP1 on the laser-diode board to VDD.

NOTE: The laser diode stays on.

5. Perform a DC measurement of the APD output current.
6. Turn the knob on the VOA counterclockwise to reduce its attenuation.
7. Observe the voltage reading on the multimeter.
8. Use Equation 1 to calculate the APD output current.
9. Remove JP1 to return control of the laser-diode driver to the trigger signal from the TSW digital-capture card.

6 Verification and Measured Performance

Figure 17 shows the bench setup to evaluate the performance of the system in the lab.

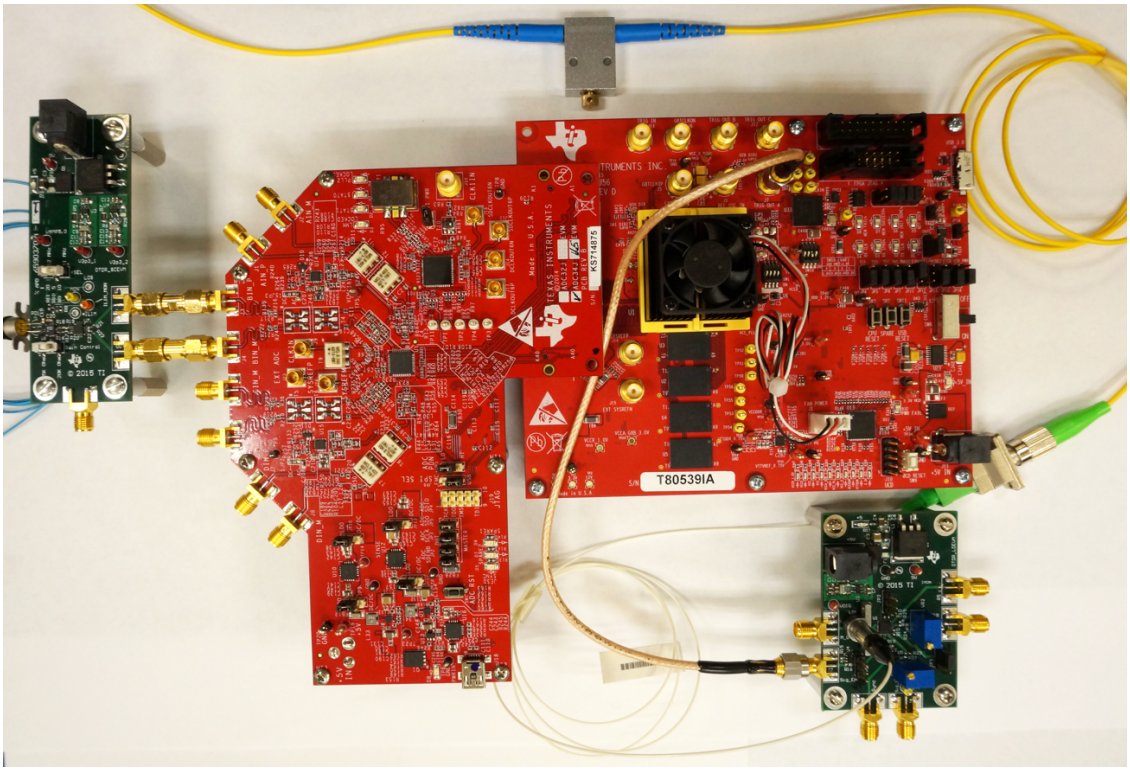

Figure 17. Laboratory Bench Setup of Optical Loop-Back System

6.1 Output Noise of Amplifier Stage

TI measured and compared the noise of the amplifier signal chain with the simulated measurements in Figure 10. TI found the total output noise of the system to be 365 µVRMS and 840 µVRMS for the 5-kΩ and 20-kΩ transimpedance-gain settings, respectively. These findings correlate to the simulated values. The calculations assume a 135-MHz brick-wall filter. For more information, see Figure 18.

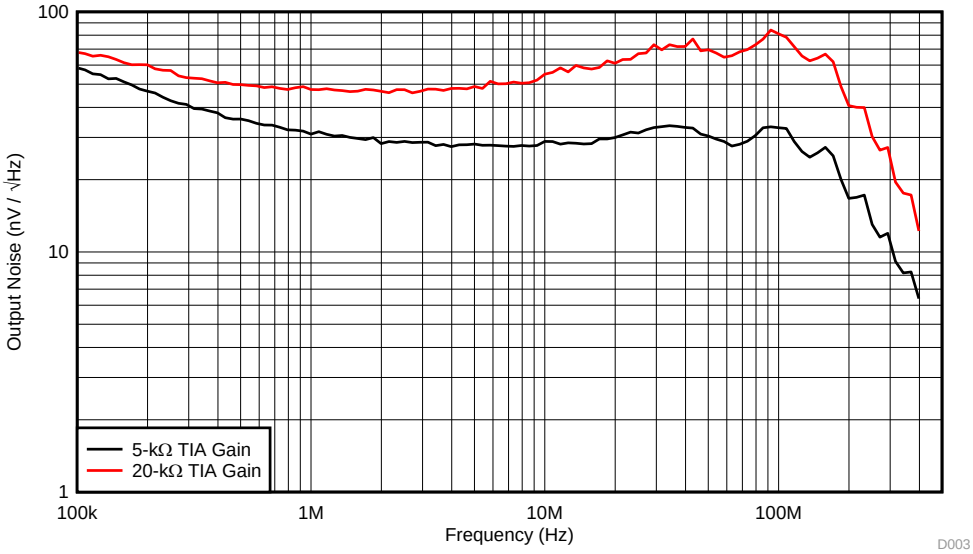

Figure 18. Measured Output Noise of Amplifier Signal Chain

6.2 System Output Noise

The total output noise of the system and its components was measured using the ADC34J45. Table 2 shows the results. The signal-chain noise correlates with the spectrum analyzer measurements. Because the photodiode is a significant contributor to the total noise of the system, TI also measured with an unilluminated photodiode.

Table 2. Output Noise of the System and Components

System Setup	Output Noise (μV_{RMS})
ADC34J45	260
OPA857 (G = 5 kΩ) + THS4541 + ADC34J45	460
OPA857 (G = 20 kΩ) + THS4541 + ADC34J45	1050
NR7500 + OPA857 (G = 5 kΩ) + THS4541 + ADC34J45	525
NR7500 + OPA857 (G = 20 kΩ) + THS4541 + ADC34J45	1300

TI measured the output noise of the system including the photodiode after averaging. Table 3 shows the results.

Table 3. System Noise vs Number of Averages

Number of Averages	Noise: 5-kΩ Gain (μV_{RMS})	Noise: 20-kΩ Gain (μV_{RMS})
10	165	405
100	51	127
1000	16.7	41
10000	6	14
100000	4	7.9

6.3 Pulse Response Measurements

6.3.1 Pulse Response vs Output Voltage

TI measured the output pulse response as a function of the output voltage swing for both transimpedance-gain settings. Figure 19 plots the response with the output voltage plotted on a log-scale to accentuate the settling performance. Figure 20 compares the settling responses for the different output voltages on a linear scale. The curves have been offset from each other by 50 µV to make comparisons easy.

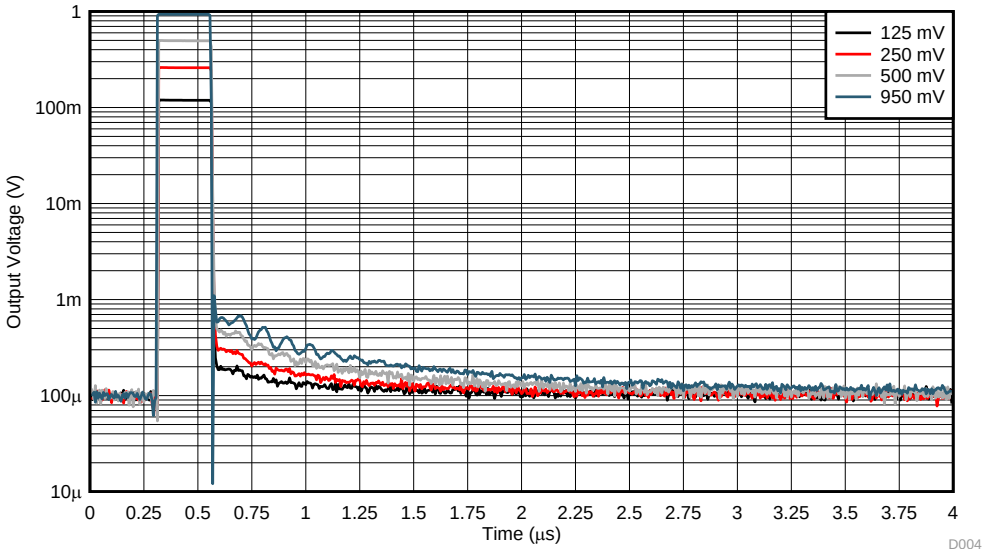

Figure 19. Pulse Response vs Output Voltage, 20-kΩ Transimpedance Gain

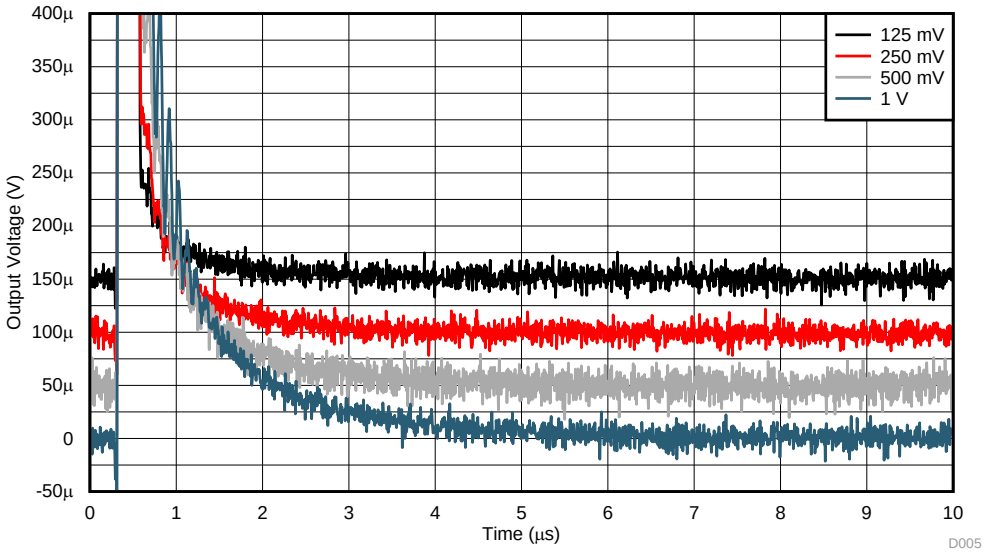

Figure 20. Long-Term Settling Response vs Output Voltage, 20-kΩ Transimpedance Gain

Figure 21 and Figure 22 show the response for the 5-kΩ transimpedance-gain setting.

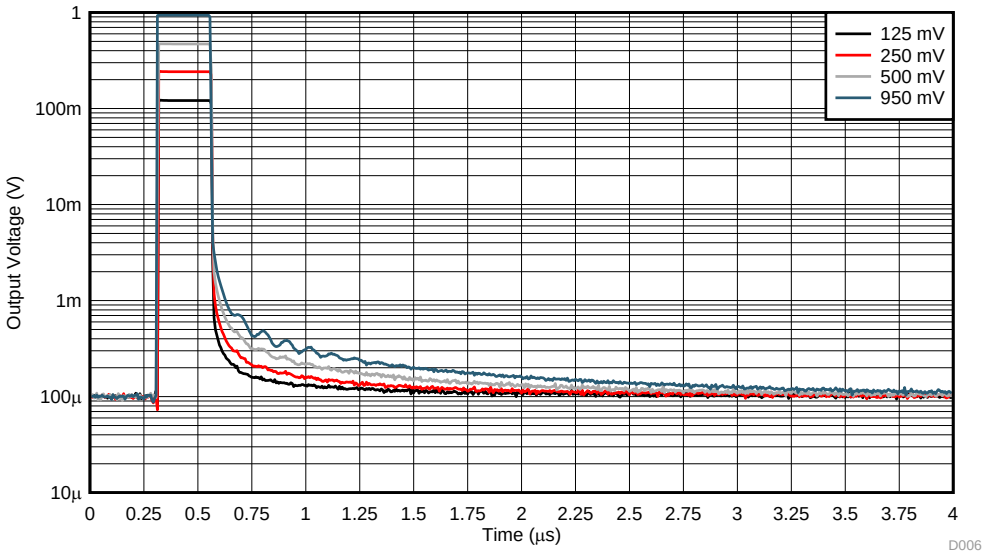

Figure 21. Pulse Response vs Output Voltage, 5-kΩ Transimpedance Gain

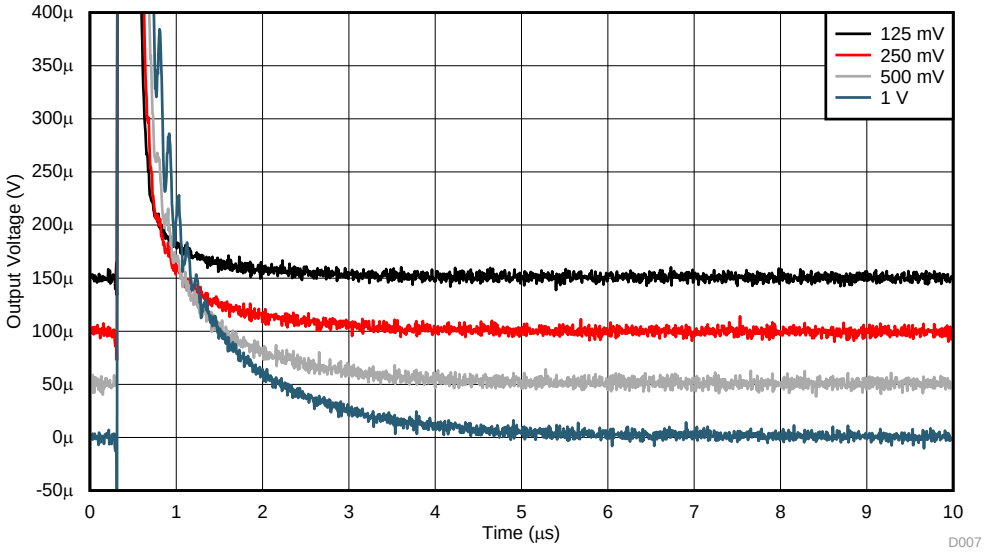

Figure 22. Long-Term Settling Response vs Output Voltage, 5-kΩ Transimpedance Gain

6.3.2 Pulse Response vs Output Pulse Width

Figures 23 through 28 show the pulse response as a function of the pulse width for the two transimpedance-gain settings. TI adjusted the optical attenuator to drive an output voltage of 0.5 V.

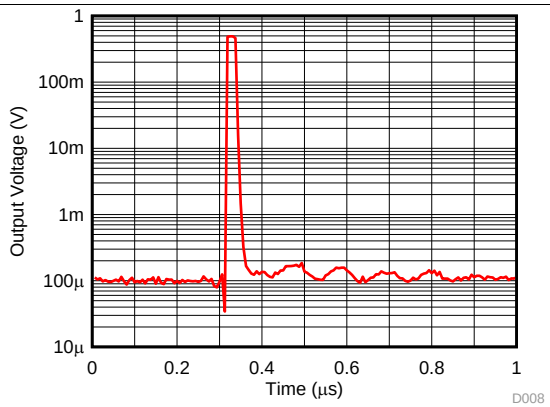

Figure 23. 25-ns Pulse Width, 20-kΩ Gain

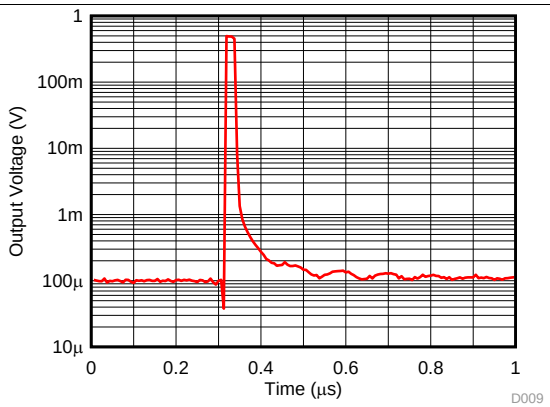

Figure 24. 25-ns Pulse Width, 5-kΩ Gain

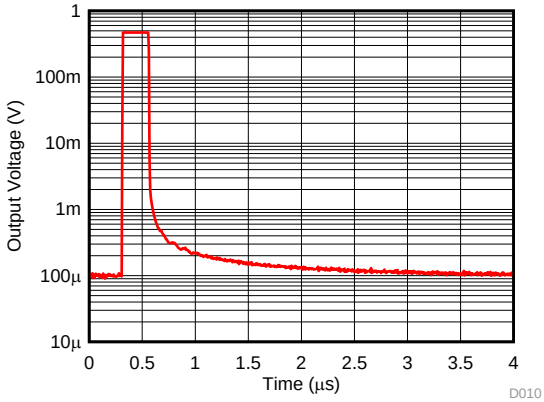

Figure 25. 250-ns Pulse Width, 20-kΩ Gain

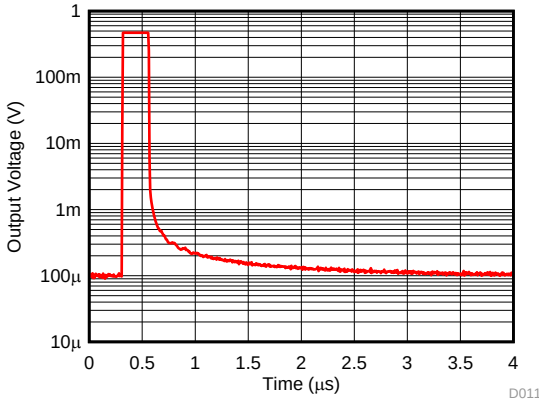

Figure 26. 250-ns Pulse Width, 5-kΩ Gain

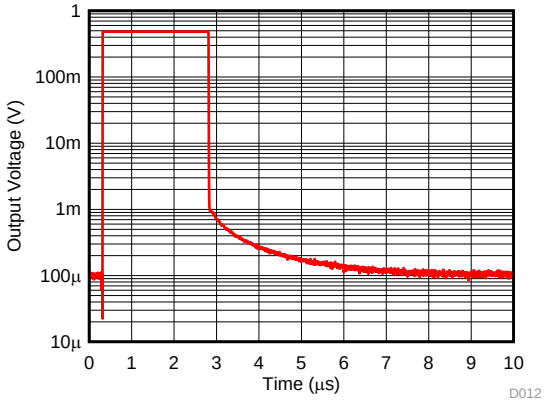

Figure 27. 2.5-µs Pulse Width, 20-kΩ Gain

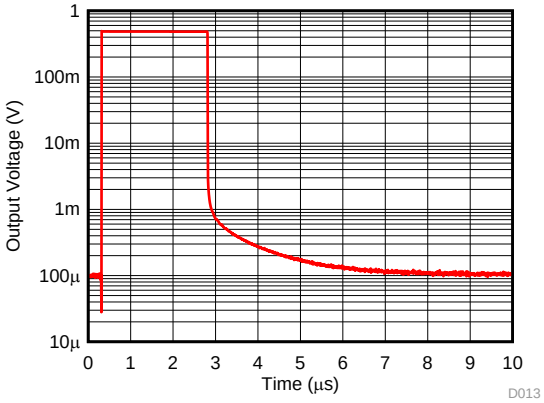

Figure 28. 2.5-µs Pulse Width, 5-kΩ Gain

6.3.3 Overloaded Pulse Response

TI also evaluated the system response for an overdriven output signal from the TIA in both gain configurations. TI adjusted the optical attenuator to vary the output current from the photodiode with the bias settings to the laser driver unchanged from the previous measurements and to set the pulse width to 250 ns for the tests. See Figure 29 and Figure 30 for more information.

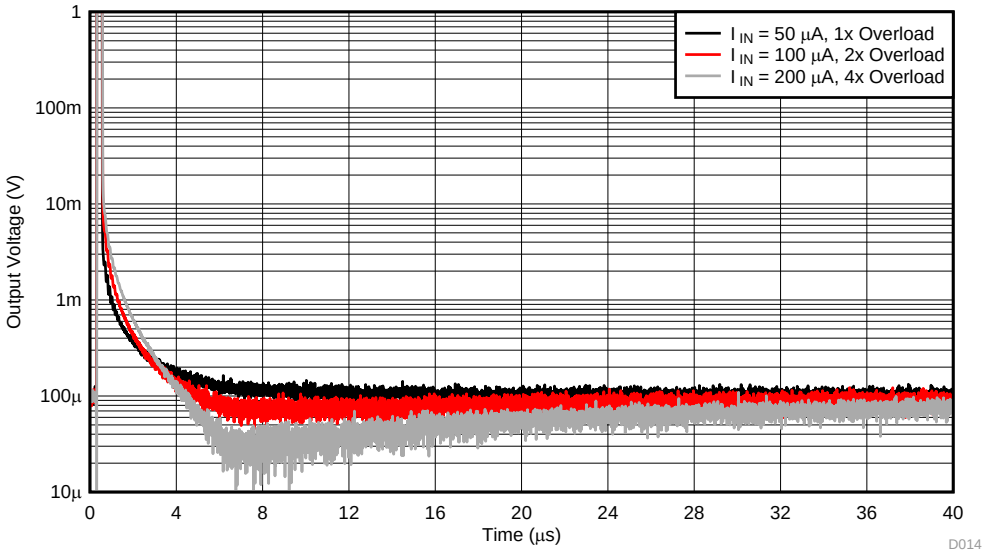

Figure 29. TIA Gain = 20 kΩ, Overloaded Response

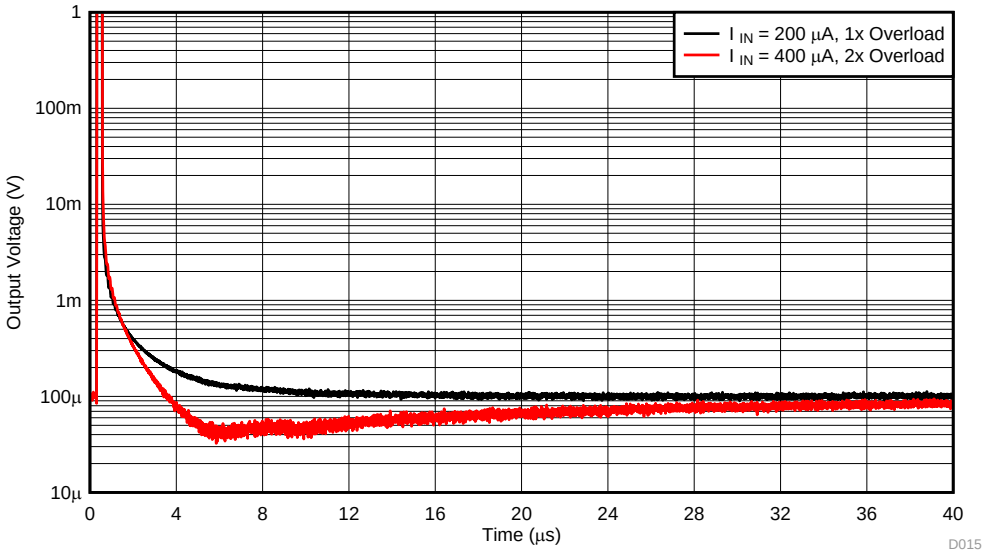

Figure 30. TIA Gain = 5 kΩ, Overloaded Response

6.3.4 Pulse Response vs Output Termination

The output of the THS4541 was doubly terminated at the ADC inputs through a 50-Ω resistor. This configuration creates a 6-dB loss in signal output resulting in an effective FDA gain of 2.5 V/V. TI configured the circuit to prevent signal reflections because of the distance between the THS4541 output, and the input of the ADC. When the THS4541 and ADC3K share the same PCB, you can eliminate this termination. TI also measured the pulse response of the circuit without the 50-Ω termination at the ADC input and compared the results with the earlier measurements. TI set the pulse width to 250 ns and configured the OPA857 in a gain of 20 kΩ. Figure 31 shows that the unterminated output does not affect the settling performance of the system.

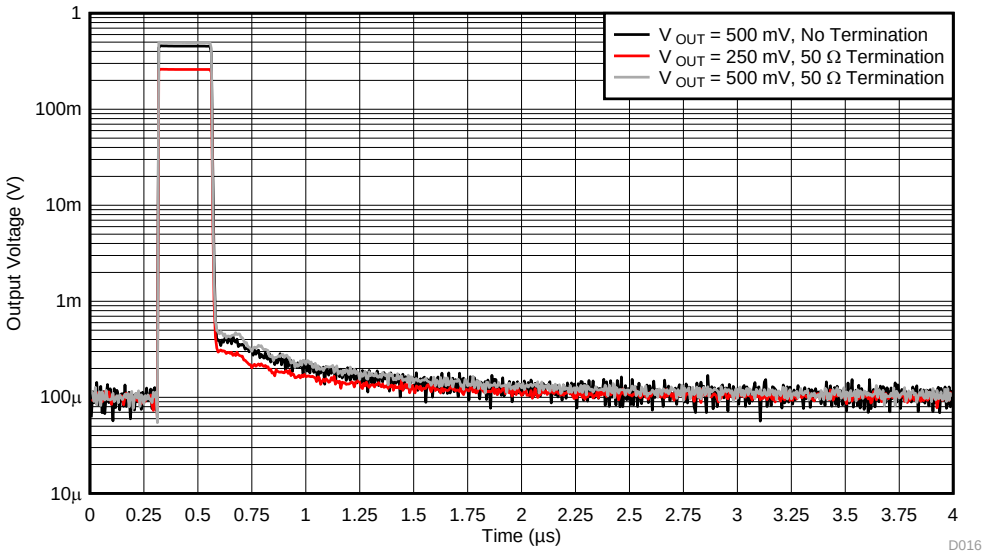

Figure 31. Effect of Output Termination on Settling Performance

6.4 OTDR System Test

Using the principle of Rayleigh scattering, TI used optical time-domain reflectometry (OTDR) to test and characterize optical cables. In a true OTDR system, light from the transmitter (usually a high-power laser) is injected into the optical fiber under test. The backscattered light from the test fiber is collected using a photo detector that converts the optical signal into a current output, which is processed using a low-noise, high-speed signal chain. See Optical Time-Domain Reflectometer Wiki and Guide to Fiber Optics and Premises Cabling for more information on OTDR.

Figure 32 shows a block diagram of a test OTDR system. A 3-port, fiber-optic circulator (for example, see http://www.thorlabs.com/thorproduct.cfm?partnumber=6015-3-FC) is required for the measurement.

1. Couple the output from the laser into port 1 of the circulator.
2. Connect the optical fiber being tested to port 2.
3. Connect port 3 to the photodiode.
4. Allow light from port 1 to enter port 2 with minimal insertion loss while the light from port 1 to port undergoes large attenuation.
5. Allow the back-scattered light from port 2 to enter port 3 with minimal insertion loss but is greatly attenuated at port-1.
6. Attenuate light entering port 3 at port 1 and port 2.

For the tests in this section, the transimpedance gain was 20 kΩ. Based on the results in Section 6.3.4, TI did not terminate the THS4541 with a 50-Ω resistor at the input of the ADC3K. This overall system gain was 20 kΩ × 5 V/V = 100 kΩ.

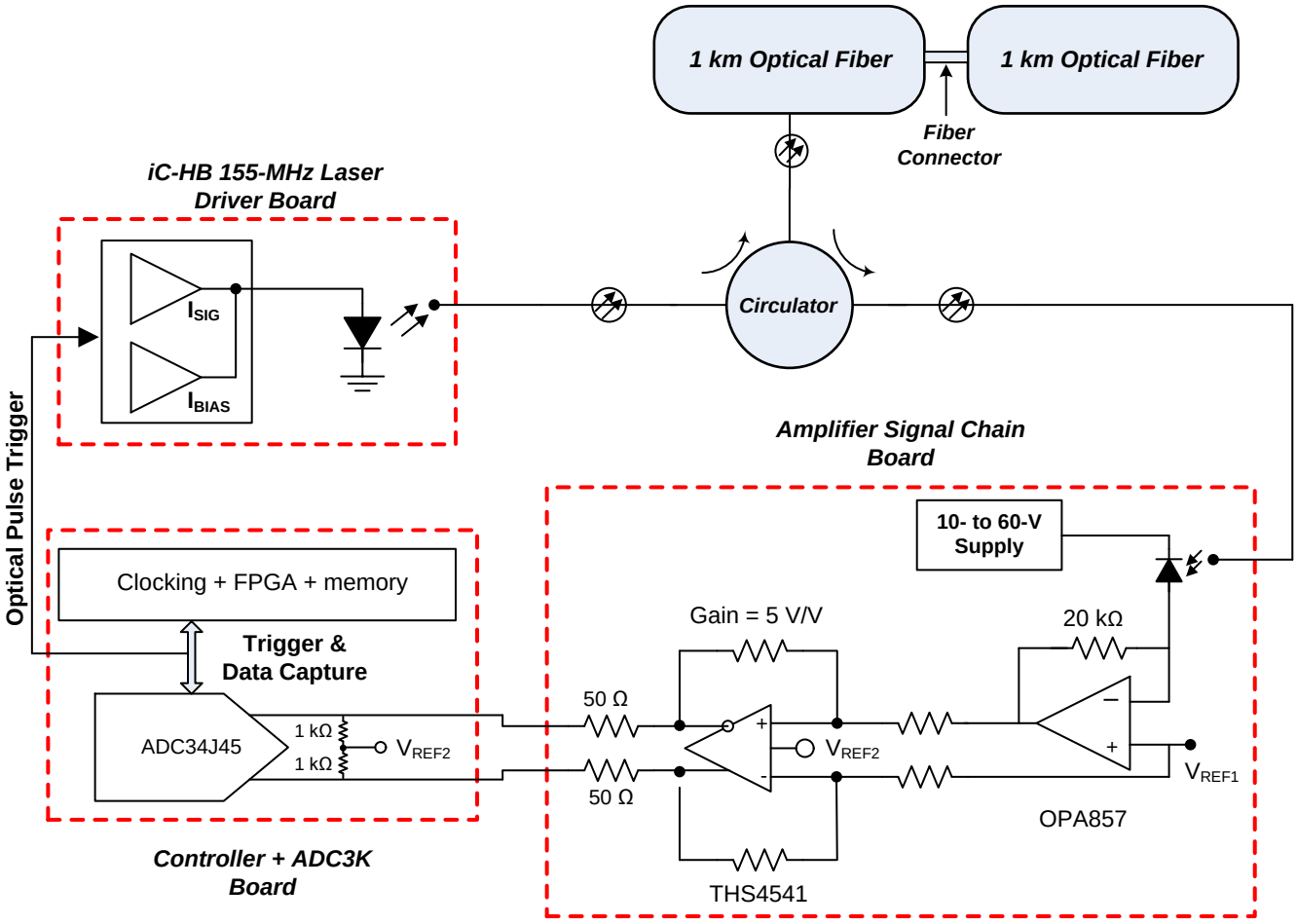

Figure 32. OTDR Block Diagram

TI conducted several OTDR tests by varying the optical pulse-width with the results in figure 33. Increasing the pulse-width increases the amount of backscattered light incident on the photodiode. There are three distinct regions in the output response.

- At t = 0.3 µsec, a discontinuity occurs in the backscatter due to Fresnel reflections occurring at the opto-coupler between the laser diode and the first section of 1-km fiber. Based on the speed of light in fiber (200,000 km/sec), the light takes 10 µsec to travel 1 km and return to the source.
- At t = 10.3 µsec, a second discontinuity occurs in the backscatter due to Fresnel reflections occurring at the opto-coupler between the two 1-km fibers.
- At t = 20.3 µsec, a large reflection occurs when the light encounters the unterminated end of the second fiber.

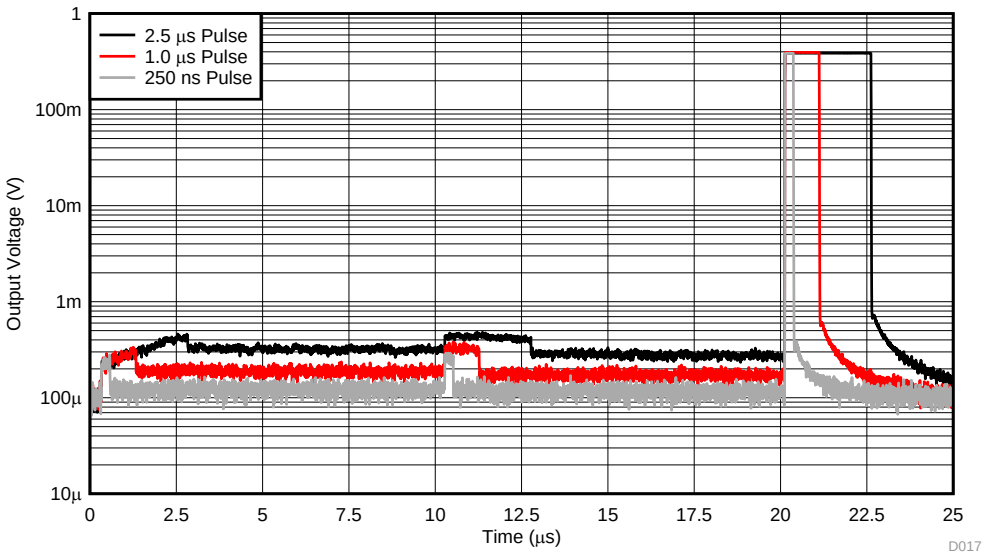

Figure 33. OTDR System Test vs Optical Pulse Width

With the pulse-width set at 2.5 µsec, TI retested the OTDR system. TI bent the second fiber at the coupling between the two fibers. The increased optical attenuation at the fiber bend exists in the droop in backscattered power at 10 µsec and in the reduced reflected power at the unterminated fiber end. See Figure 34 for more information.

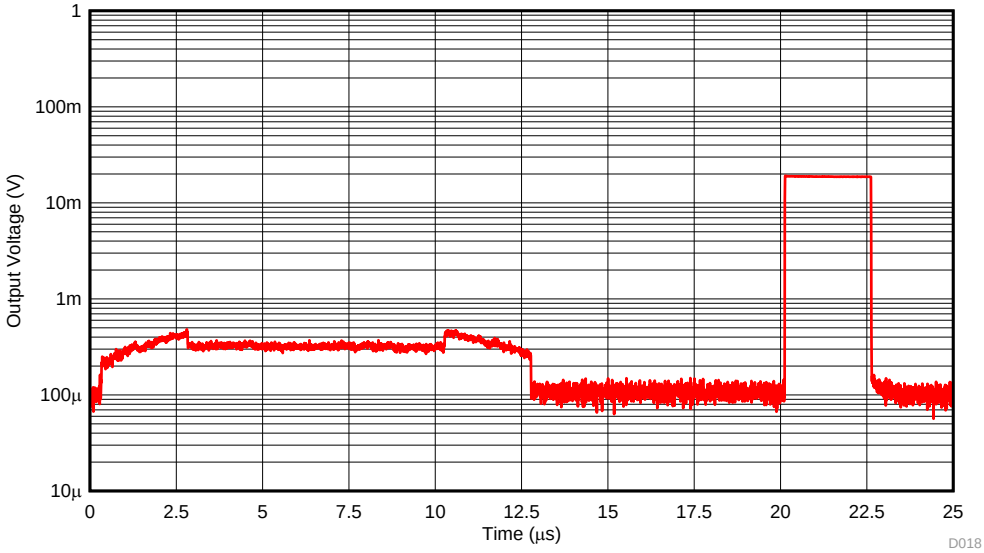

Figure 34. OTDR Response With Bend in Optical Fiber

7 System Enhancements

In this section, TI proposes two different methods of improving the system SNR performance.

7.1 THS4541 Level-Shift Circuit

Depending on the direction of reverse-bias, a photodiode can either source or sink current. The output of the OPA857 swings in a negative direction from its common-mode reference voltage. When this signal is applied to the THS4541, each of its differential outputs swings either higher or lower than its output common-mode (VOCM). Due to this unipolar swing limitation, only half the input range of the ADC is used, which reduces the dynamic range of the system by 6 dB. To overcome this limitation, configure the FDA as shown in Figure 35.

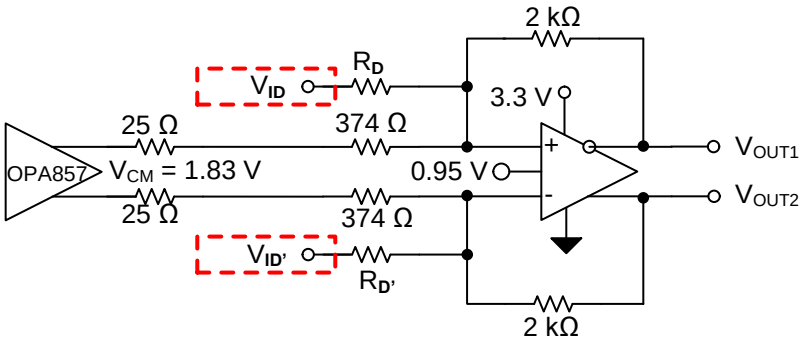

Figure 35. THS4541 Level-Shift Circuit

The ADC3K has a specified maximum differential-input swing of 2 V_{PP} on a 0.95-V common-mode input. This implies that each differential input to the ADC input can swing from 0.45 V to 1.45 V. To level-shift the output of the THS4541 to take advantage of the full dynamic range of the ADC, apply a differential DC input signal ($V_{I\_DIFF} = V_{ID} – V_{ID'}$) to produce a 1-$V_{PP}$ differential output.

Calculate the input common-mode of the THS4541 from the OPA857 output as follows:

$$\frac{1.83 - V_{ICM}}{400\,\Omega} = \frac{V_{ICM} - 0.95}{2\,k\Omega} \quad (2)$$

$$\Rightarrow V_{ICM} = 1.68\,V \quad (3)$$

Calculate the gain of the level-shift circuit as follows:

$$\frac{V_{O\_DIFF}}{V_{I\_DIFF}} = -\frac{R_F}{R_D} \quad (4)$$

To reduce the noise-gain contribution from the level-shift circuit, keep its gain to a minimum. If a level-shift circuit gain of 0 dB is assumed, set $R_D = R_{D'} = 2$ kΩ, $V_{ID} = (1.68\ V + 0.5\ V)$, and $V_{ID'} = (1.68\ V – 0.5\ V)$. Figure 36 shows the simulated output for a 100-mV differential input to the THS4541 circuit. From simulations, the increased noise due to the level-shift circuit is less than 6%.

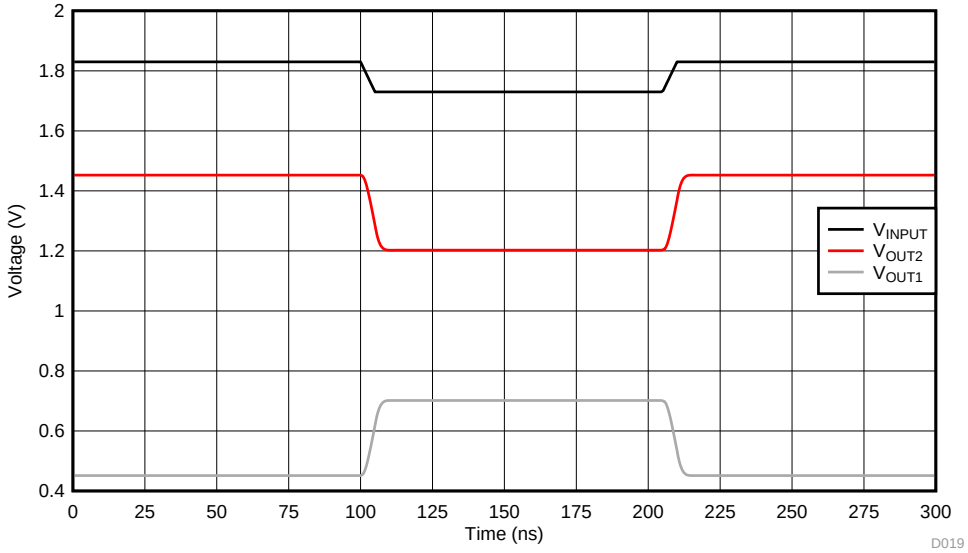

Figure 36. Simulated Output Pulse of Level-Shift Circuit

7.2 Anti-Aliasing Filter

To reduce the total system noise, place a third-order, passive Bessel filter between the THS4541 and ADC3K. Figure 37 shows one such implementation of the filter.

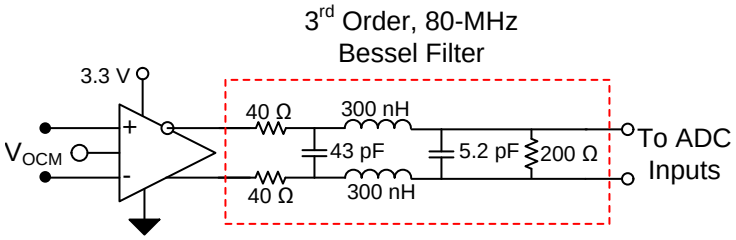

Figure 37. Anti-Alias Filter

The simulated system noise was reduced by 50% when using this anti-alias filter. The final shunt capacitor filter (5.2 pF) must be tuned based on the differential input capacitance of the ADC. The filter introduces a 3-dB insertion loss to the overall system gain.

8 Conclusion

This reference design describes a complete end-to-end optical front-end system and its performance. Various techniques to optimize the SNR performance of the signal chain are also discussed. This reference design provides a flexible platform, letting you change critical system components such as the amplifier chain, ADC, and the optical components.

9 Design Files

To download the design files, see the files at TIDA-00725.

9.1 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00725.

10 References

1. *Optical Time-Domain Reflectometer Wiki*, https://en.wikipedia.org/wiki/Optical_time-domain_reflectometer
2. *Guide to Fiber Optics and Premises Cabling*, http://www.thefoa.org/tech/ref/testing/OTDR/OTDR.html
3. *Laser-Diode Driver, iC-HB* data sheet (https://www.ichaus.de/upload/pdf/HB_datasheet_A4en.pdf)
4. *Laser Diode, LDM5S515* data sheet (https://www.oequest.com/getDatasheet/id/2165-3255cfdc2f98b43.pdf)
5. *Variable Fiber Optical Inline Attenuator*, http://www.fiberstore.com/fc-apc-to-fc-apc-variable-fiber-optic-voa-in-line-attenuator-0-60db-p-13556.html

11 About the Author

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