TI Designs: TIDA-00662
High-Performance Capacitive Sensor Front-End Reference Design

Description

This reference design is a high-performance capacitive sensor front-end reference design. Using an audio codec with programmable mini digital signal processor (DSP) functionality, impedance measurement and phase change detection are realized. The frequency-domain sensing front end is suitable for pressure and flow transmitter applications, as well as any other application that uses capacitive sensor elements.

Resources

TIDA-00662	Design Folder
TLV320AIC3254	Product Folder
MSP430F5529	Product Folder
OPAx376	Product Folder
OPA317	Product Folder
TPS736xx	Product Folder
TPD2E001	Product Folder

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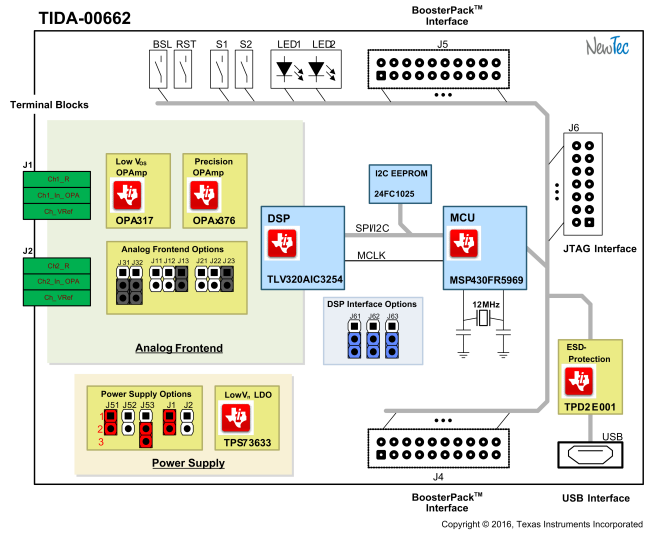
Features

- Frequency-Domain Sensing Extracts Exact Phase Differences to Measure Impedance and Phase Changes
- Suitable for Pressure and Flow Transmitters Using Capacitive Sensors
- Use of Audio Codec miniDSP Functions to Measure Impedance and Phase Change
- Physical Form Factor in BoosterPack™ for Compatibility With Each TI LaunchPad™

Applications

- Sensors and Field Transmitters
- Factory Automation and Process Control



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1 System Description

Monitoring and maintaining process variables at the appropriate levels is extremely critical in industrial automation and process control. A sensor in the industrial environment is either continuously or periodically measuring vital parameters such as temperature, pressure, flow, and so on. The primary challenge of sensing in industrial environments is conditioning low-signal levels in the presence of high-noise and high-surge voltage.

The TI Design TIDA-00662 (see Figure 1) is a sensor front end design enabling the user to easily evaluate the Z-Domain measurement, which is an advanced impedance measurement approach based on the TLV320AIC3254. The TIDA-00662 is suitable for measuring either capacitive or inductive sensors (for example, pressure field transmitters) and measuring complex impedances.

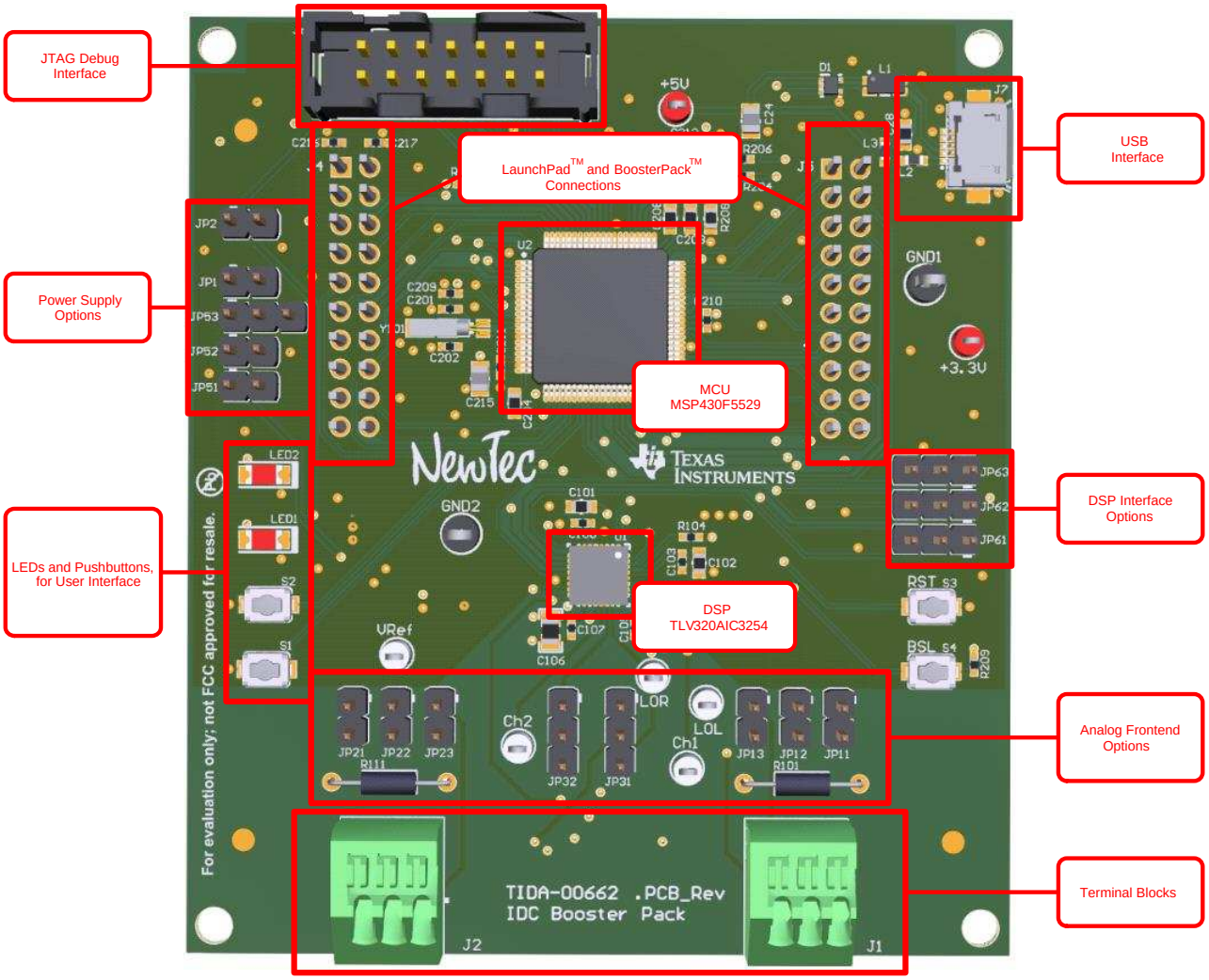

Figure 1. TIDA-00662 Overview

1.1 Key System Specifications

Table 1 lists the key system specifications.

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	MIN	TYP	MAX	UNIT
V_{cc}	Supply voltage range	—	3.3	—	V
T_a	Operating free-air temperature	–40	—	85	°C
F_{system}	Processor frequency (Maximum MCLK frequency)	—	—	12	MHz

2 System Overview

2.1 Block Diagram

The main devices of the TIDA-00662 are components of the AFE: the MSP430™ microcontroller (MCU), TLV320AIC3254 DSP, and external interfaces including the BoosterPack connectors, JTAG, and the USB port (see Figure 2).

The terminal blocks used to connect the sensor elements to the AFE include a jumper collection which offers the possibility of different hardware setups of the Z-Domain measurement. The DSP converts the analog measurement data into digital, and implements the data processing of the Z-Domain measurement method. Because the DSP does not have nonvolatile memory, it is necessary to write the firmware to the DSP after every reset, realized by the MCU which communicates using either I^2C or SPI with the DSP component. Additionally, the MCU reads out and implements the further processing of the measurement data of the DSP. The external interface communication is also managed by the MCU.

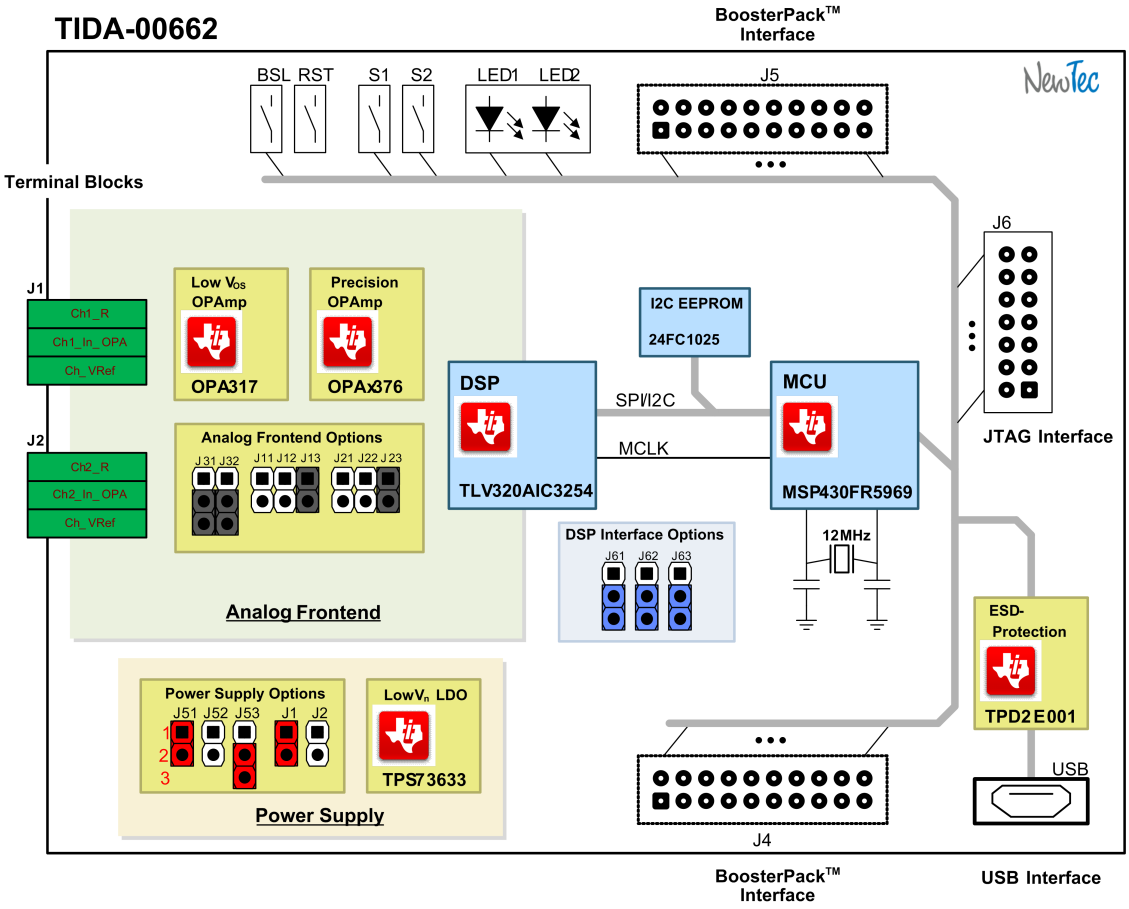

Figure 2. TIDA-00662 Block Diagram

2.2 Highlighted Products

For more information on each of the following devices, see their respective product folders at www.TI.com.

2.2.1 TLV320AIC3254

The TLV320AIC3254 (also referred to as the AIC3254, see Figure 3) is a flexible, low-power, low-voltage dual-channel signal processor with programmable inputs and outputs, PowerTune capabilities, a fully-programmable miniDSP, fixed predefined and parameterizable signal processing blocks, integrated PLL, integrated LDOs, and flexible digital interfaces. The TLV320AIC3254 features two fully-programmable miniDSP cores which support application-specific algorithms. The miniDSP cores are fully software controlled. Target algorithms are loaded into the device after power-up.

The TLV320AIC3254 includes extensive register-based control of power, I/O channel configuration, gains, pin-multiplexing, and clocks, allowing precise targeting of the device to its application. The integrated PowerTune technology allows the device to be tuned to an optimum power-performance trade-off. The voltage supply range for the TLV320AIC3254 is 1.5 to 1.95 V for analog and 1.26 to 1.95 V for digital. To ease system-level design, integrated LDOs generate the appropriate analog or digital supply from input voltages ranging from 1.8 to 3.6 V. The device supports digital I/O voltages in ranges of 1.1 to 3.6 V.

The required internal clock of the TLV320AIC3254 can be derived from multiple sources including: the MCLK pin, BCLK pin, GPIO pin, or the output of the internal PLL where the input to the PLL again can be derived from the MCLK pin, BCLK or GPIO pins. Although using the PLL ensures the availability of a suitable clock signal, PLL use is not recommended for the lowest power settings. The PLL is highly programmable and can accept available input clocks in the range of 512 kHz to 50 MHz.

Features:

- Low supply-voltage range: 3.6 V down to 1.9 V
- Two 32-bit ΔΣ-ADC with 93 dB SNR
- Two 32-bit ΔΣ-DAC with 100 dB SNR
- PowerTune
- Extensive signal processing options
- Embedded miniDSP
- Master clock up to 50 MHz
- Six single-ended or three fully-differential analog inputs
- Two analog outputs
- Digital serial communication interfaces
  - SPI and I^2C
- Programmable PLL
- Integrated LDO
- 5 mm × 5 mm 32-pin QFN package
- Operating temperature –40°C to 85°C

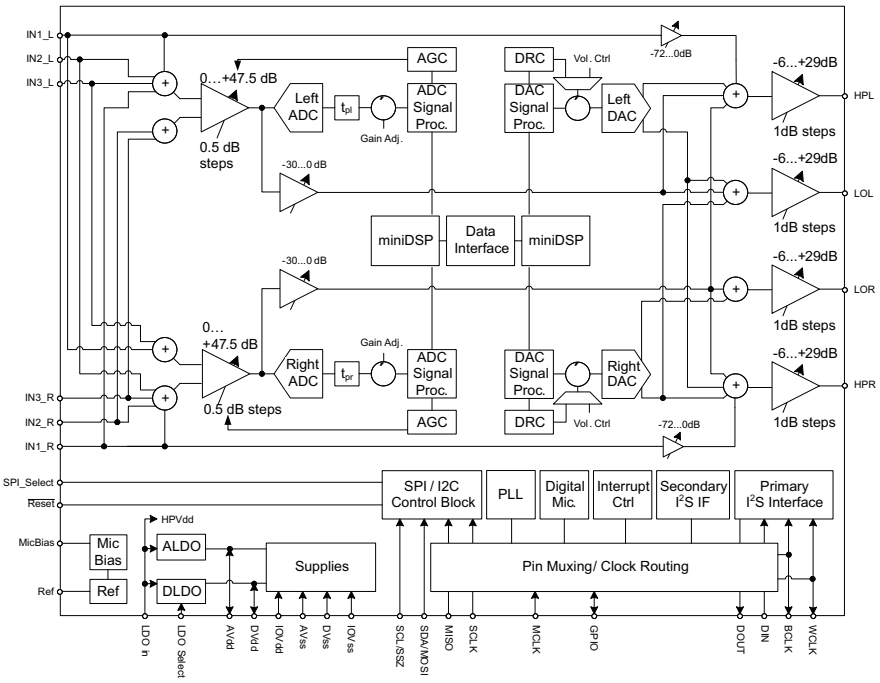

Figure 3. TLV320AIC3254 Block Diagram

2.2.2 MSP430F5529

The Texas Instruments MSP430 family of ultra-low-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in 3.5 μs (typical). The MSP430F5529 is a MCU configuration with integrated USB and PHY supporting USB 2.0, four 16-bit timers, a high performance 12-bit ADC, two universal serial communication interfaces (USCI), hardware multiplier, DMA, real-time clock module with alarm capabilities, and 63 I/O pins (see Figure 4). Typical applications include analog and digital sensor systems, data loggers, and others that require connectivity to various USB hosts.

Features:

- Low supply-voltage range: 3.6 V down to 1.8 V
- Ultra-low-power consumption
  - Active mode (AM):
    - All system clocks active
    - 290 μA/MHz at 8 MHz, 3.0 V, flash program execution (typ)
    - 150 μA/MHz at 8 MHz, 3.0 V, RAM program execution (typ)
  - Standby Mode (LPM3):
    - Real-time clock with crystal, watchdog, and supply supervisor operational, full RAM Retention, fast wake-up: 1.9 μA at 2.2 V, 2.1 μA at 3.0 V (typ)
    - Low-power oscillator (VLO), general-purpose counter, watchdog, and supply supervisor operational, full RAM retention, fast wake-up: 1.4 μA at 3.0 V (typ)
  - Off Mode (LPM4):
    - Full RAM Retention, Supply Supervisor Operational, Fast Wake-up: 1.1 μA at 3.0 V (typ)
  - Shutdown Mode (LPM4.5): 0.18 μA at 3.0 V (typ)
- Wake-up from standby mode in 3.5 μs (typ)

- 16-Bit RISC architecture, extended memory, up to 25-MHz system clock
- Flexible power management system
  - Fully Integrated LDO with programmable regulated core supply voltage
  - Supply voltage supervision, monitoring, and brownout
- Unified Clock System
  - FLL control loop for frequency stabilization
  - Low-power low-frequency internal clock source (VLO)
  - Low-frequency trimmed internal reference source (REFO)
  - 32-kHz watch crystals (XT1)
  - High-frequency crystals up to 32 MHz (XT2)
- 16-Bit Timer TA0, Timer_A with five capture and compare registers
- 16-Bit Timer TA1, Timer_A with three capture and compare registers
- 16-Bit Timer TA2, Timer_A with three capture and compare registers
- 16-Bit Timer TB0, Timer_B with seven capture and compare shadow registers
- Two universal serial communication interfaces
  - USCI_A0 and USCI_A1 each support:
    - Enhanced UART supports auto-baud rate detection
    - IrDA encoder and decoder
    - Synchronous SPI
  - USCI_B0 and USCI_B1 each support:
    - I2CTM
    - Synchronous SPI
  - Full-speed universal serial bus (USB)
    - Integrated USB-PHY
    - Integrated 3.3-V and 1.8-V USB power system
    - Integrated USB-PLL
    - Eight I/O endpoints
  - 12-bit ADC with internal reference, sample-and-hold, and autoscan feature
  - Comparator
  - Hardware multiplier supporting 32-bit operations
  - Serial onboard programming, no external programming voltage needed
  - Three channel internal DMA
  - Basic timer with real-time clock feature

For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

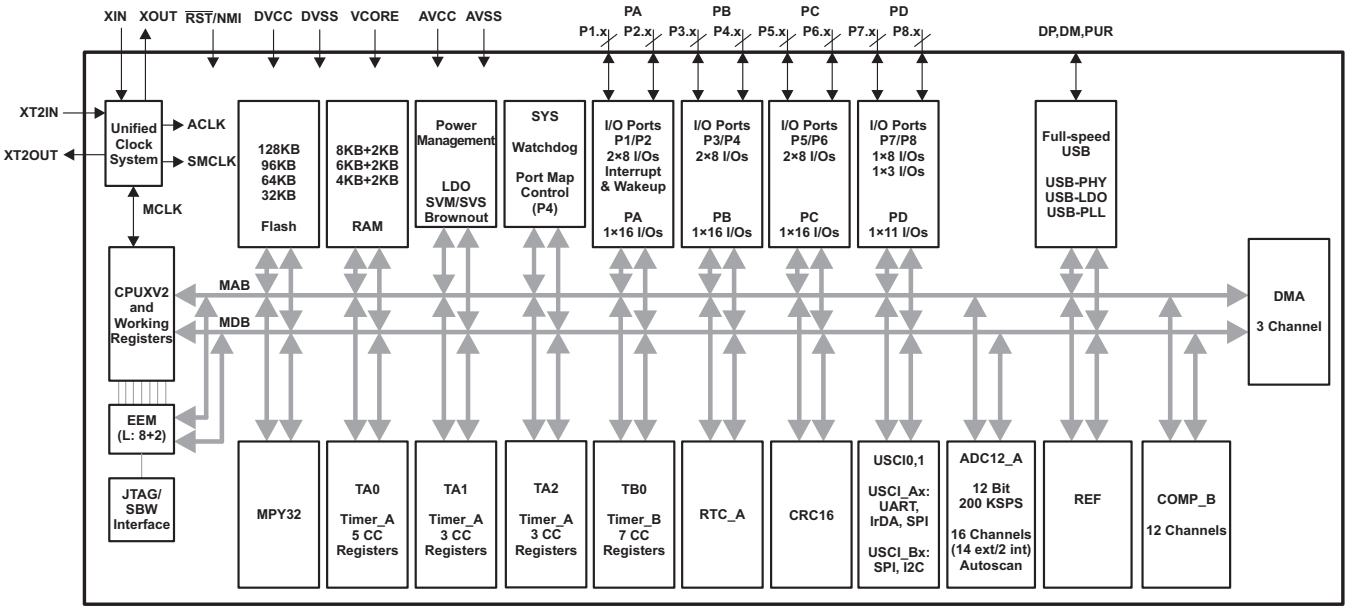

Figure 4. MSP430F5529 Block Diagram

2.2.3 OPA317

The OPA317 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zerø-Drift family of amplifiers that use a proprietary auto-calibration technique to simultaneously provide low offset voltage (90 µV max) and near-zero drift over time and temperature at only 35 µA (max) of quiescent current. The OPA317 family features rail-to-rail input and output in addition to near flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation, as low as +1.8 V (± 0.9 V) and up to +5.5 V (± 2.75 V). The OPA317 (single version) is available in SC70-5, SOT23-5, and SOIC-8 packages. The OPA2317 (dual version) is offered in MSOP-8 and SOIC-8 packages. The OPA4317 is offered in the standard SOIC-14 and TSSOP-14 packages, as well as in the space-saving VQFN-14 package. All versions are specified for operation from –40°C to 125°C.

Features:

- Supply voltage: 1.8 to 5.5 V
- microPackages:
  - Single: SOT23-5, SC-70, SOIC-8
  - Dual: MSOP-8, SOIC-8
  - Quad: SOIC-14, TSSOP-14
- Low offset voltage: 20 µV (typ)
- CMRR: 108 dB (typ)
- Quiescent current: 35 µA (max)
- Gain bandwidth: 300 kHz
- Rail-to-rail I/O
- Internal EMI/RFI filtering

2.2.4 OPAx376

The OPA376 family represents a new generation of low-noise operational amplifiers with e-trim, offering outstanding DC precision and AC performance. Rail-to-rail input and output, low offset (25 μV max), low noise (7.5 nV/√Hz), quiescent current of 950 μA max, and a 5.5 MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it ideal for applications which run directly from batteries without regulation. The OPA376 (single version) is available in MicroSIZE SC70-5, SOT23-5, and SO-8 packages. The OPA2376 (dual) is offered in WCSP-8, MSOP-8, and SO-8 packages. The OPA4376 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to 125°C.

Features:

- Low noise: 7.5 nV/√Hz at 1 kHz
- 0.1 Hz to 10 Hz noise: 0.8 μV_{PP}
- Quiescent current: 760 μA (typ)
- Low offset voltage: 5 μV (typ)
- Gain bandwidth product: 5.5 MHz
- Rail-to-rail I/O
- Single-supply operation
- Supply voltage: 2.2 to 5.5 V
- Space-saving packages:
  - SC-70, SOT23, WCSP, MSOP, and TSSOP

2.2.5 TPD2E001

The TPD2E001 is a two-channel transient voltage suppressor (TVS)-based electrostatic discharge (ESD) protection diode array (see Figure 5). The TPD2E001 is rated dissipate ESD [reword] strikes at the maximum level specified in the IEC 61000-4-2 Level 4 international standard. The DRS package (3.00 mm × 3.00 mm) is also available as a non-magnetic package for medical imaging applications. See also TPD2E2U06DRLR which is P2P compatible to TPD2E001DRLR and offers higher IEC ESD Protection, lower clamping voltage, and eliminates the input capacitor requirement.

Features:

- IEC 61000-4-2 ESD protection (level 4)
  - ±8 kV contact discharge
  - ±15 kV air-gap discharge
- IO capacitance: 1.5 pF (typ)
- Low leakage current: 1 nA (max)
- Low supply current: 1 nA
- 0.9- to 5.5-V supply-voltage range
- Space-saving DRL, DRY and QFN package options
- Alternate 3-, 4-, and 6-channel options available: TPD3E001, TPD4E001, TPD6E001

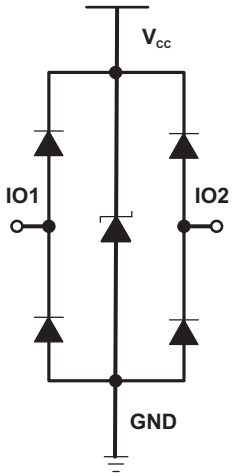

Figure 5. TPD2E001 Block Diagram

2.2.6 TPS736xx

The TPS736xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current. The TPS736xx (see Figure 6) uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 μA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-μF CNR) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Features:

- Stable with no output capacitor, or any value, or type of capacitor
- Input voltage range: 1.7 to 5.5 V
- Ultra-low dropout voltage: 75 mV (typ)
- Excellent load transient response—with or without optional output capacitor
- New NMOS topology delivers low reverse leakage current
- Low noise: 30 μV_{RMS} typical (10 Hz to 100 kHz)
- 0.5% initial accuracy
- 1% overall accuracy over line, load, and temperature
- Less than 1-μA maximum I_Q in shutdown mode
- Thermal shutdown and specified min and max current limit protection
- Available in multiple output voltage versions
  - Fixed outputs of 1.2 to 5.0 V
  - Adjustable output from 1.20 to 5.5 V
  - Custom outputs available

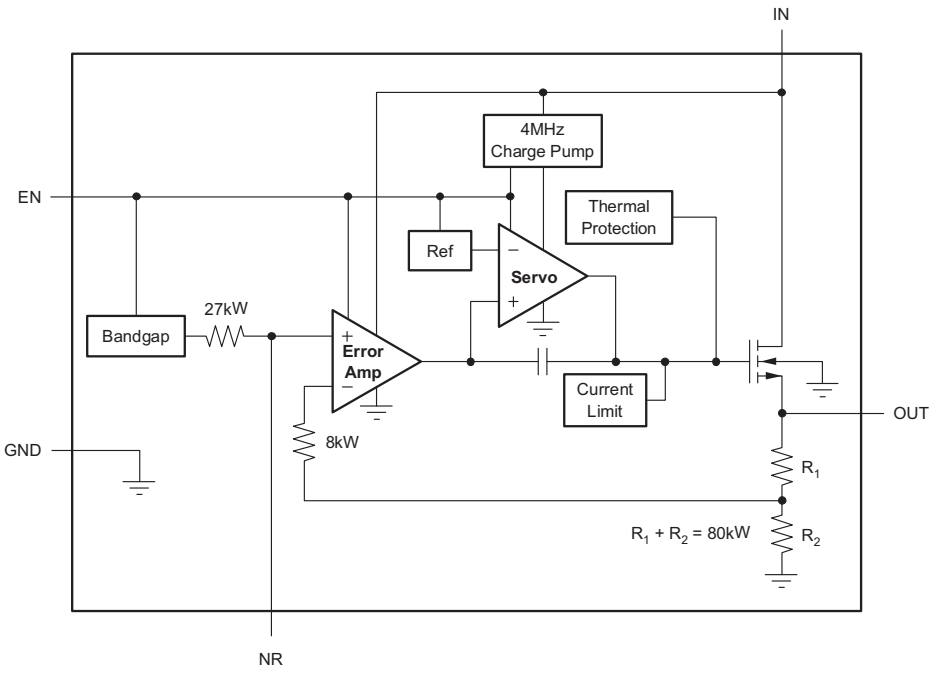

Figure 6. TPS736xx Block Diagram

2.3 System Design Theory

2.3.1 Description of Z-Domain Measurement

The Z-Domain measurement approach is based on a frequency locked system, shown in Figure 7. The system fundamentally consists of a known reference impedance R_{Ref} and a second unknown impedance Z_{Var}. In addition, there is a signal generator which applies a periodic excitation signal with the frequency f0 to the network. The generator signal excites the reference impedance and it also excites the unknown impedance. The measurement method principally relies on the determination of the relative phase shift between these two signals. For this purpose digital samples of the two signals are taken synchronously with a fixed sampling rate fs that is an integer multiple of the excitation frequency. The oversampling ratio defines the number of captured samples per period for each signal and can be rather small.

The determination of the sought impedance is based on calculating the relative phase between the two signals. Therefore, no fixed absolute phase and amplitude relation between the excitation and the sampled signals are necessary. As the calculation of the sought impedance relies on a frequency-locked system, it is necessary to always fulfill the condition that the sampling frequency is an integer multiple of the excitation signal. As a result of the relative measurement, the sampling of the two channels can start at any phase referring to the excitation signal, as long as the sampling of the two channels is synchronous. Because of this characteristic, no sample and hold circuits are required; therefore, one or more high-resolution delta sigma ($\Delta\sum$) ADCs can be used

In addition to the measurement of the capacitance by calculating the relative phase, there is a second method which is based on the ratio of the relative amplitude of the two signals. This method depends on the same fundamental relations and equations such as the relative phase method. An advanced measurement system could include both methods, so that, depending on the conditions, the system could choose between the two methods or even measure complex impedances by combining the two methods.

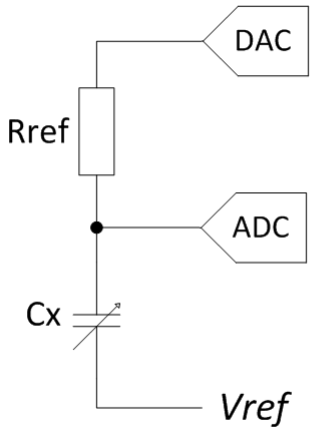

Figure 7. Simplified Measurement Setup

2.3.2 Description of DSP (AIC3254)

The TLV320AIC3254 is an integrated codec which was originally designed for audio applications, especially in portable devices. The TLV320AIC3254 features two ADCs, two DACs, and further configurable inputs and outputs. Outstanding features are the two programmable DSP cores. Because it can be adapted using different DSP algorithms, the TLV320AIC3254 is very flexible for many applications.

The internal memory of the TLV320AIC3254 is volatile and its purpose is to implement the data processing of the Z-Domain measurement method, which contains, among other things, the following tasks:

- Convert the respective signals to analog or digital
- Process of the measured data
- Generate the voltage reference
- Generate the sinusoidal excitation signal

2.3.3 Description of MCU (MSP430)

The MCU can be programmed individually by the user, depending on the requirements of their specific application. A typical implementation includes the following functions:

- Writing DSP firmware using SPI or I^2C to the DSP after reset
- Reading measurement data of the DSP using SPI or I^2C periodically (for example, approximately 1 ms)
- Implementing further processing of the measured data
- Generating the MCLK for the DSP (using an external crystal, 12 MHz)
- Individual data processing like scaling and linearization algorithms
- Management of the BoosterPack Interfaces (SPI, I^2C, UART)
- USB communication to run the Z-Domain BoosterPack as a standalone application
- JTAG debug interface
- External EEPROM available for additional data memory

Furthermore users can configure two buttons (S1 and S2) and two LEDs (LED1 and LED2) appropriate to their needs. The crystal XTAL1 with a frequency of 32.768 kHz can be used for real time applications.

2.3.4 Internal Interface: DSP to MCU

The internal serial interfaces serve to connect the DSP (slave) with the MCU (master). The TLV320AIC3254 provides either I^2C or SPI as the communication interface. The preferred interface can be selected using three jumpers. Because the internal memory of the TLV320AIC3254 is volatile, it must be reprogrammed by the MCU after each power up. The serial interface unit allows for programming the codec during system start-up and configuring and controlling the codec while the application is running. The SPI_SELECT pin is one of two fixed-function pins of the TLV320AIC3254. Depending on the state of this hardware-control pin, the pins SCL, SDA, GPO1 and GPI1 are configured for either I^2C or SPI protocol. SPI_SELECT must be tied high to select SPI, and SPI_SELECT must be tied low for I^2C. TI does not recommend changing the state of SPI_SELECT during device operation.

2.3.4.1 SPI Control

In the SPI control mode, the TLV320AIC3254 uses the pins SCL/SS as SS, SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI and a standard SPI port with a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, or serial communication between the host processor MSP430 (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave device, in this case the TLV320AIC3254, depends on a master to start and synchronize transmissions. A transmission begins when initiated by the SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register (see Figure 8).

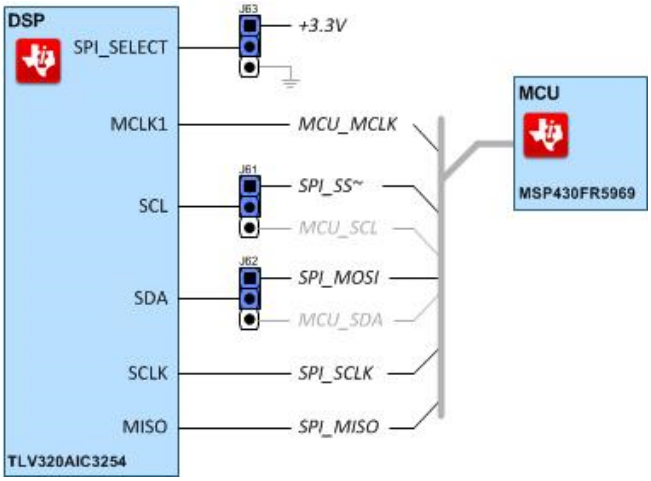

Figure 8. SPI

2.3.4.2 I²C Control

The TLV320AIC3254 supports the I²C control protocol and responds to the I²C address of 0011000. I²C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus (see Figure 9). Devices on the I²C bus only drive the bus lines low by connecting them to ground. They never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are high when no device is driving them low. This circuit prevents two devices from conflicting. If two devices drive the bus simultaneously, there is no driver contention.

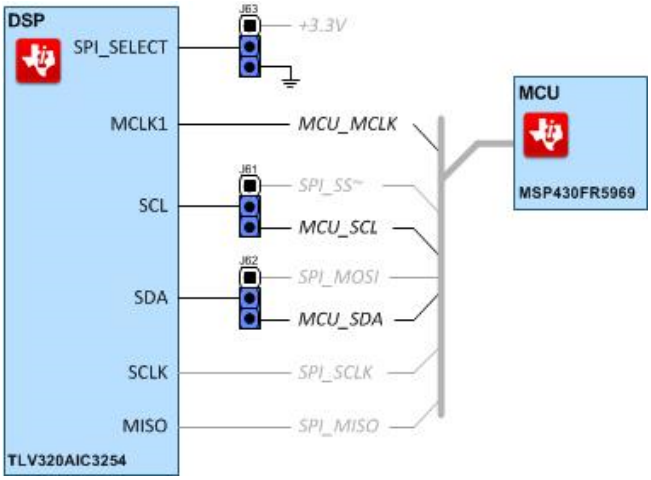

Figure 9. I²C Interface

2.3.4.3 DSP to MCU Interface Jumper Positions

Table 2. DSP to MCU Interface Jumper Positions

SELECTED INTERFACE	JP61	JP62	JP63
SPI	1-2	1-2	1-2
I^2C	2-3	2-3	2-3

2.3.5 External Interfaces

2.3.5.1 BoosterPack Interface

To minimize the time to market for new industrial sensor systems, TI developed the LaunchPad Development Kit Ecosystem, which offers customers an easy way to connect TI industrial reference designs in a modular construction system. To provide this modular construction system, the mechanical dimensions, interfaces, and electrical properties of these reference designs are defined in the BoosterPack Pinout Standard (see Figure 11).

Each reference design implements the functionality of a sub-system of an industrial field transmitter or process instrumentation. By stacking interface, front end, power, and various other reference designs, it is possible to build a fully functional demonstrator system of an industrial field transmitter. As a part of the number of reference designs of industrial field transmitters belonging to the TI LaunchPad Ecosystem, the TIDA-00662 is compatible with all TI LaunchPads. The TIDA-00662 evaluation board has the functionality of measuring impedances and can either be combined with other BoosterPacks and LaunchPads, or it can be used as a stand alone system (see Figure 10).

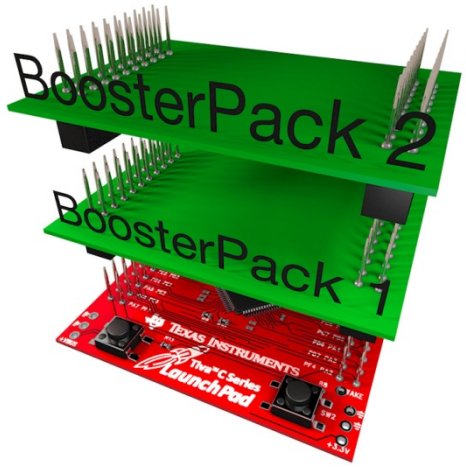

Figure 10. LaunchPad Ecosystem

BoosterPacks are plug-in modules that fit on top of LaunchPads. These innovative tools plug into a consistent and standardized connector on the LaunchPad and allow developers to explore different applications enabled by a TI microcontroller. These options are also offered by the TIDA-00662.

Figure 11 shows the BoosterPack Pinout Standard.

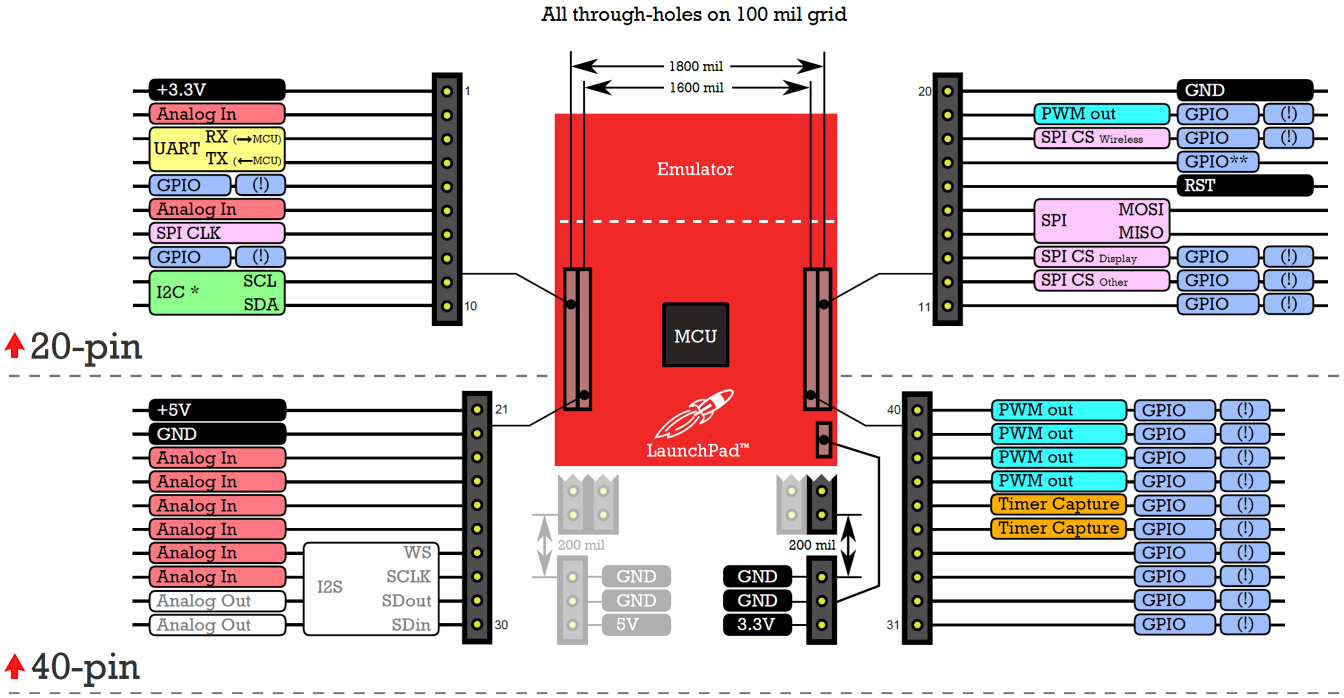

Figure 11. BoosterPack Connector Pinout Standard

Table 3 lists how this standard is implemented specifically for the TIDA-00662. Table 3 contains the exact interface pin connections between the BoosterPack connectors and the MCU.

Table 3. Interface Booster Pack to MCU

SIGNAL	MCU PIN
BP_Analog_In_1	P6.5 / A5
BP_UART_RX	P4.6 / PM_NONE
BP_UART_TX	P4.7 / PM_NONE
BP_IO_1	P1.6
BP_Analog_In_2	P6.6 / A6
BP_SPI_CLK	P4.0 / PM_UCA1CLK
BP_IO_2	P1.4
BP_I2C_SCL	P4.2 / PM_UCB1SCL
BP_I2C_SDA	P4.1 / PM_UCB1SDA
BP_IO_3	P8.1
BP_SPI_CS	P4.3 / PM_UCA1STE
BP_SPI_CS_Disp	P2.6
BP_SPI_MISO	P4.5 / PM_UCA1SOMI
BP_SPI_MOSI	P4.4 / PM_UCA1SIMO
MCU_RST	RST~
BP_IO_4	P5.6
BP_SPI_CS_W	P2.2
BP_PWM_Out_1	P2.0 / TA1.1
BP_Analog_In_3	P6.0 / A0
BP_Analog_In_4	P6.1 / A1
BP_Analog_In_5	P6.2 / A2
BP_Analog_In_6	P6.3 / A3
BP_Analog_In_7	P6.4 / A4
BP_Analog_In_8	P6.7 / A7
BP_IO_9	P1.2
BP_IO_10	P1.3
BP_IO_5	P8.2
BP_IO_6	P3.5
BP_IO_7	P3.6
BP_IO_8	P3.7
BP_TC_1	P2.4 / TA2.1
BP_TC_2	P2.5 / TA2.2
BP_PWM_Out_2	P5.7 / TB0.1
BP_PWM_Out_3	P7.4 / TB0.2
BP_PWM_Out_4	P7.5 / TB0.3
BP_PWM_Out_5	P7.6 / TB0.4

2.3.5.2 JTAG Interface

The JTAG interface is used to program and debug the MSP430. Figure 12 shows the implemented design of the interface JTAG to the TIDA-00662 MCU.

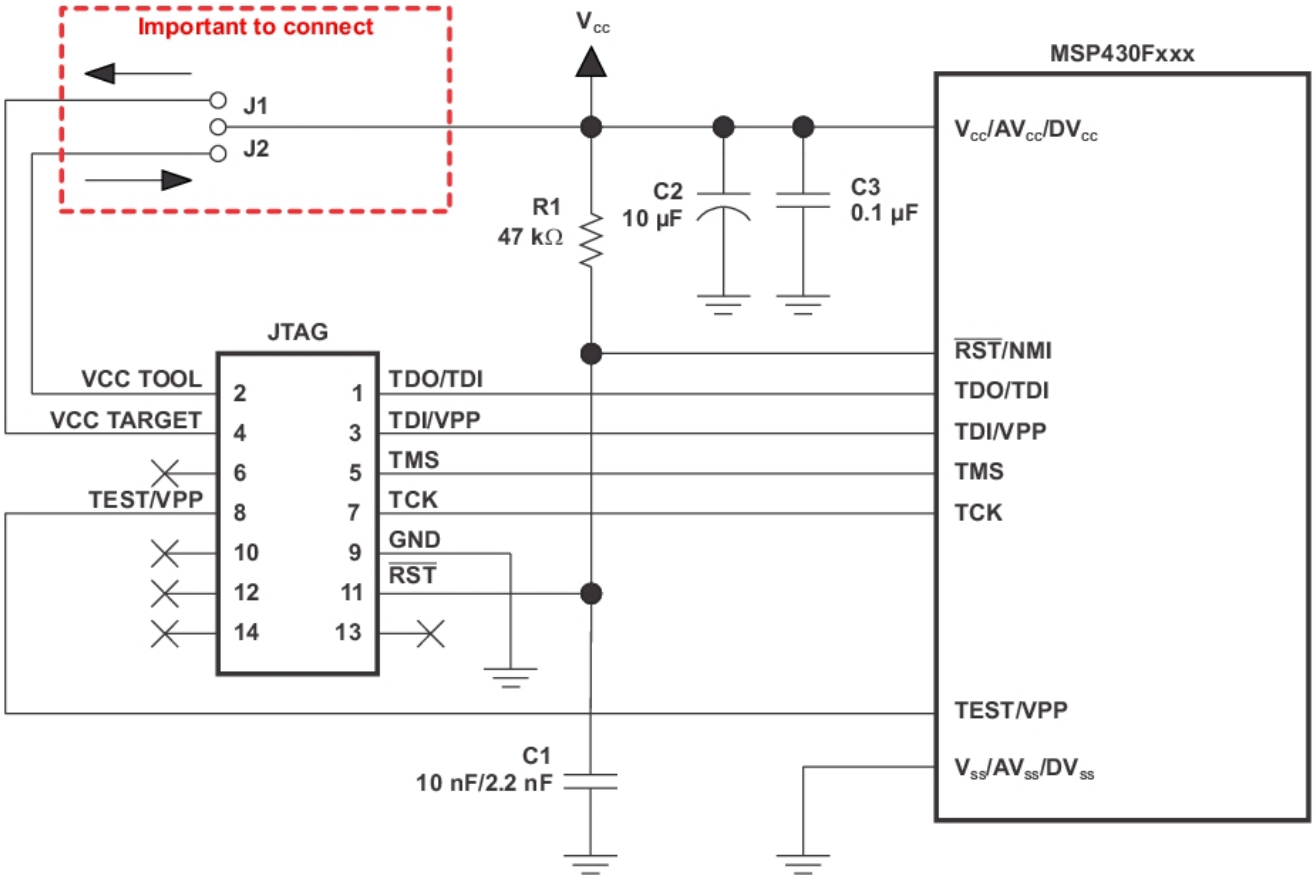

Figure 12. JTAG Interface Reference Design

2.3.5.3 USB Interface

The TIDA-00662 provides a USB interface, so that, for instance the TIDA-00662 can be used as a CDC device. CDC interfaces generate a virtual COM port on the host. Therefore, the example application of the TIDA-00662 is designed to interface with a general-purpose *terminal* application.

2.3.5.3.1 USB Bootstrap Loader Button

Like the vast majority of MSP430 derivatives, the F5529 has an on-chip bootstrap loader (BSL). The BSL is a program which is in a protected location in the flash memory of the MCU that facilitates communication with an external host. Like tools with JTAG access, the BSL can read and write the flash memory of the MCU. But unlike JTAG tools, the BSL cannot be used to emulate code. The interface to the BSL is often a UART or sometimes I^2C. On USB-equipped derivatives, the interface of the BSL is USB. In situations where JTAG access is not available, the BSL plays an important role in accessing the device.

For example, the BSL can be used to recover the device when something has corrupted the internal flash. The BSL is often used for products in the field, when there is no JTAG access. Because of its use in the field, the BSL is password-protected, which prevents unwanted access to proprietary application software. To serve its role in updating the MSP430 flash memory, the BSL must be invoked, meaning that execution must be transferred to it. This invocation can happen in a few different ways, but on the USB BSL, one way is to pull the PUR pin high immediately after a BOR reset.

2.3.5.3.2 Electrostatic Discharge Protection for USB

The TPD2E001 is a unidirectional electrostatic discharge (ESD) protection device with low capacitance (see Figure 13). The device is constructed with a central ESD clamp that features two hiding diodes per line to reduce the capacitive loading. This central ESD clamp is also connected to VCC to provide protection for the VCC line. Each I/O line is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 level 4 international standard. The low loading capacitance of the TPD2E001 makes it ideal for protecting high-speed signal terminals.

The TPD2E001 is a passive integrated circuit which activates whenever voltages above V_{BR} or below the lower diodes $V_{forward}$ (–0.6 V) are present on the circuit being protected. During ESD events, voltages as high as ±15 kV can be directed to ground and VCC through the internal diode network. When the voltages on the protected lines fall below the trigger voltage of the TPD2E001 (usually within tenths of a nano-second) the device reverts back to a high impedance state.

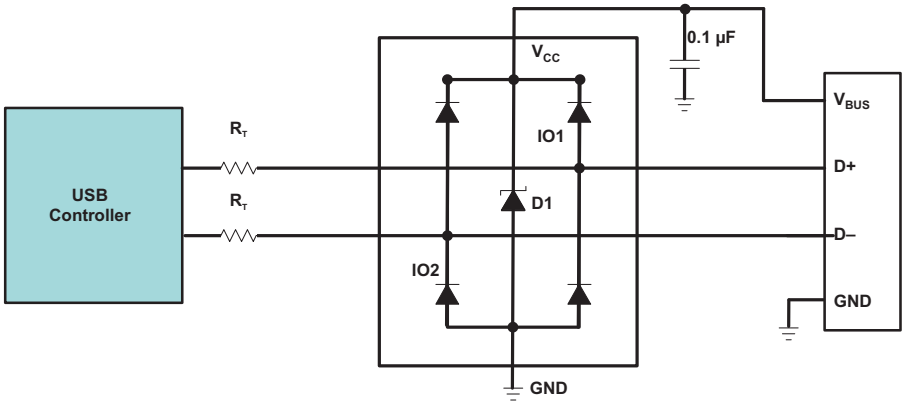

Figure 13. TPD2E001 ESD Protection

2.3.6 Description of Analog Front End

The analog front end (AFE) implements the Z-Domain measurement (only one channel), as shown in Figure 7. The impedance, which shall be measured, is connected to the TIDA-00662 through the terminal block (J1 or J2). The sinusoidal excitation signal is generated by the DSP and then converted to an analog signal by the DAC of the DSP. The signal is connected to the impedance through the reference resistor of the AFE. For further processing of the results, the measurement data is converted to digital by the ADC of the DSP. The measurement requires a voltage reference.

2.3.6.1 Analog I/O Functions of DSP

Table 4 lists the inputs and outputs of the DSP and their functions which are used for the AFE.

Table 4. Analog I/O Pin Functions of DSP

DESIGNATOR	TYPE	PRIMARY FUNCTION	SECOND FUNCTION (OPTION)
LOL	Output	Excitation signal channel 1	Excitation signal channel 2
LOR	Output	Excitation signal channel 2	Reference voltage output
IN2L	Input	Positive input channel 1	—
IN2R	Input	Negative input channel 1	—
IN3R	Input	Positive input channel 2	—
IN3L	Input	Negative input channel 2	—
REF	Output	Reference voltage output for filtering	—

2.3.6.2 Configuration Options of AFE

Based on the simple measurement setup (see Figure 13) the AFE provides different hardware setups for the Z-Domain measurement, which can be configured by several jumpers. It is possible to evaluate the measurement of two impedances at the same time. The terminal blocks J1 and J2 are used to connect the impedances with the measurement channels 1 and 2.

2.3.6.2.1 Selection of Reference Resistor

A set of jumpers allows the user to select the reference resistor for the measurement of each channel. Furthermore, an external resistor can be connected to the sensor connectors J1 and J2. The resistor selection consists of the two fixed resistors R102 and R103, with the values of 100 kΩ and 200 kΩ. There is also additional space for the THT resistor R101, which is not fixed and can be selected by the user. The same applies to the resistor selection of connector J2 (see Figure 14).

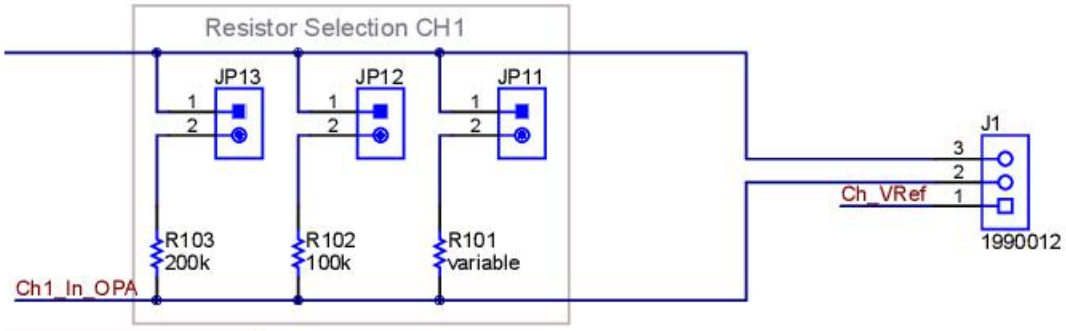

Figure 14. Reference Resistor Selection Channel 1

Table 5. Resistance Values of AFE Resistor Selection

JUMPER	RESISTANCE VALUE
JP11 / JP21	THT Resistor, selected by the user
JP12 / JP22	100 kΩ
JP13 / JP23	200 kΩ

2.3.6.2.2 Voltage Reference Selection

The voltage reference of the Z-Domain measurement method can be selected between the reference voltage V_{Ref} and the DC output of LOR (see Figure 15). If the jumper JP31 is set to position 1-2 V_{Ref}, generated by the Ref output of the TLV320AIC3254, is selected as reference voltage. If the position is changed to 2-3, the signal LOR is used as reference voltage. The selection applies to both channels.

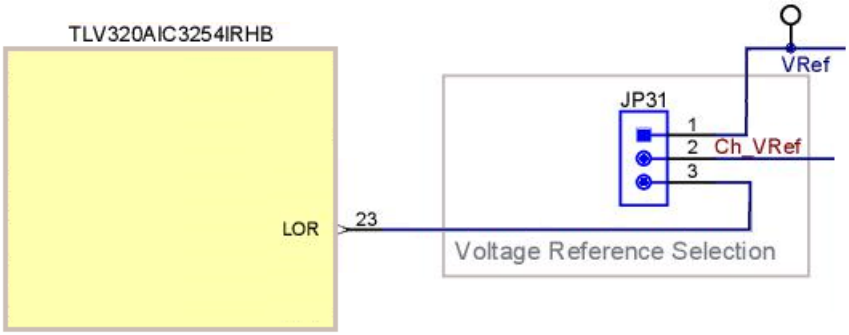

Figure 15. Voltage Reference Selection

The TLV320AIC3254 has a built-in bandgap used to generate reference voltage V_{REF} of the device. To achieve high SNR, the reference voltage on REF should be filtered using an external capacitor (minimum 1 µF) from REF terminal to ground. Because it is not allowed to connect loads to the REF terminal, an amplifier circuit is used to generate the reference voltage of the TIDA-00662 (see Figure 16).

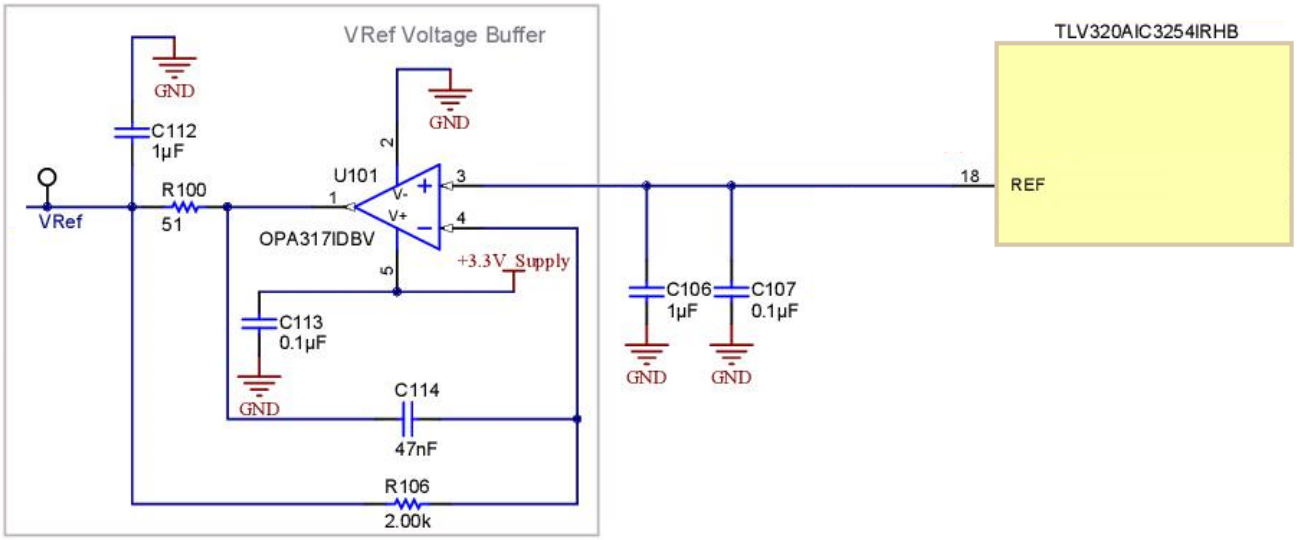

Figure 16. Reference Voltage Output for Filtering

2.3.6.2.3 Single and Dual Excitation Selection

The AFE provides two different excitation modes. In single channel configuration the two channels are excited by a separate signal. For this configuration the jumper JP32 must be set to position 2-3. In this case the impedance C1 is excited by LOL and the impedance C2 is excited by LOR. This mode is only available if the jumper JP31 is in position 1-2, so that not LOR, but V_{Ref} is used as the reference voltage. In the dual channel mode both impedances, C1 and C2, are excited by LOL. To use this mode the jumper position of JP32 has to be changed to the pins 1-2 (see Figure 17).

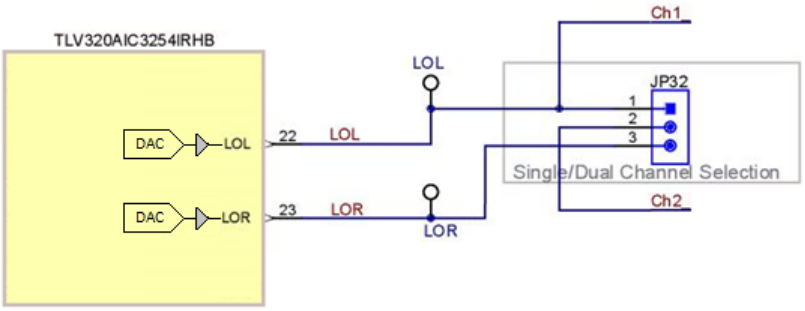

Figure 17. Single and Dual Excitation Selection

2.3.6.2.4 AFE Voltage Reference and Excitation Selections

Table 6. AFE Voltage Reference and Excitation Selections

DESCRIPTION	JP31	JP32
V_{REF} is used as voltage reference Both channels are excited by LOL	1-2	1-2
V_{REF} is used as voltage reference Channel 1 is excited by LOL Channel 2 is excited by LOR	1-2	2-3
LOR is used as voltage reference Both channels are excited by LOL	2-3	1-2
Jumper combination is not allowed	2-3	2-3

2.3.7 Power Supply

All sub-components of the TIDA-00662 can be powered from a single +3.3 V-supply rail. There are three different voltage sources provided by the evaluation module. Through the power supply jumper selection, the user can choose between the JTAG debugger (+3.3 V), another connected BoosterPack (+3.3 V), and the USB interface (+5 V). If the USB serves as the power source, a TPS73633 LDO is used to generate the appropriate +3.3 V supply from the +5 V. The integrated LDOs of the TLV320AIC3254 ensure that the digital and analog parts are supplied with +1.8 V. If the power source is selected and a jumper is set on the respective header, the glowing power LED indicates that the TIDA-00662 is supplied. Figure 18 shows an overview of the power distribution concept.

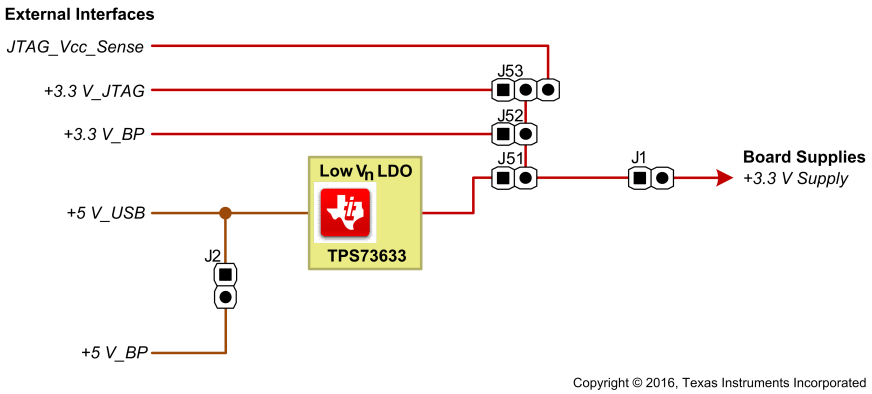

Figure 18. Power Distribution Concept

JP1 provides an easy way of measuring the current of the TIDA-00662, using a standard current probe. Therefore, the header must be connected with a conductor, which can be enclosed by the current probe. Either a jumper or a conductor must be plugged on the header JP1 to power the TIDA-00662. Figure 19, Figure 20 and Figure 21 show the different power options of the TIDA-00662 and their respective jumper positions.

2.3.7.1 JTAG as Power Source

If the jumper JP53 is in the position 1-2, the supply output of the JTAG debugger is connected to the TIDA-00662, so the JTAG is the power source of the evaluation board. If the PCB is powered by another source the jumper JP53 should be set to position 2-3, so that the V_{CC} target of the JTAG debugger is connected. V_{CC} target is an input line of the debugger, which is used to sense the level of the JTAG signals. If required, the levels of the sensed lines are adjusted, so they do not exceed or fall below the voltage range specification (see Figure 19).

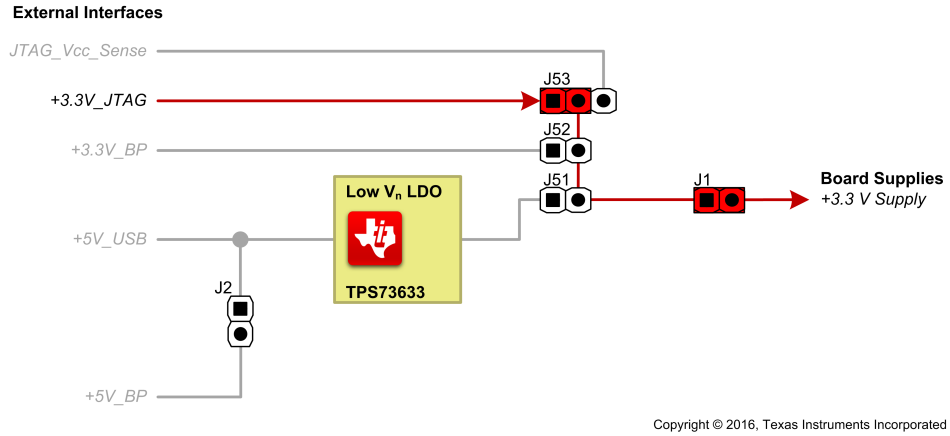

Figure 19. JTAG as Voltage Source

2.3.7.2 BoosterPack as Power Source

If a connected BoosterPack or LaunchPad is used as a power source, it is necessary to install the jumper JP52 (see Figure 20).

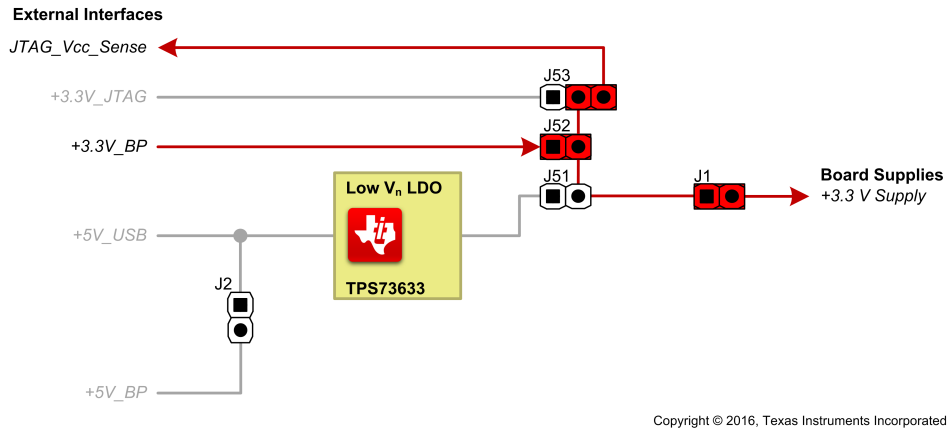

Figure 20. BoosterPack Connector as Voltage Source

2.3.7.3 USB as Power Source

The jumper JP51 must be installed if the USB is selected as the power source. The +5 V voltage is converted +3.3 V by the LDO. If another BoosterPack is connected to the TIDA-00662 and the USB interface is chosen as the power source, it is possible to power the BoosterPack as a stand alone system using the +3.3 V and +5 V supply outputs. If so, jumpers must be plugged on the headers JP52 and JP2, too (see Figure 21).

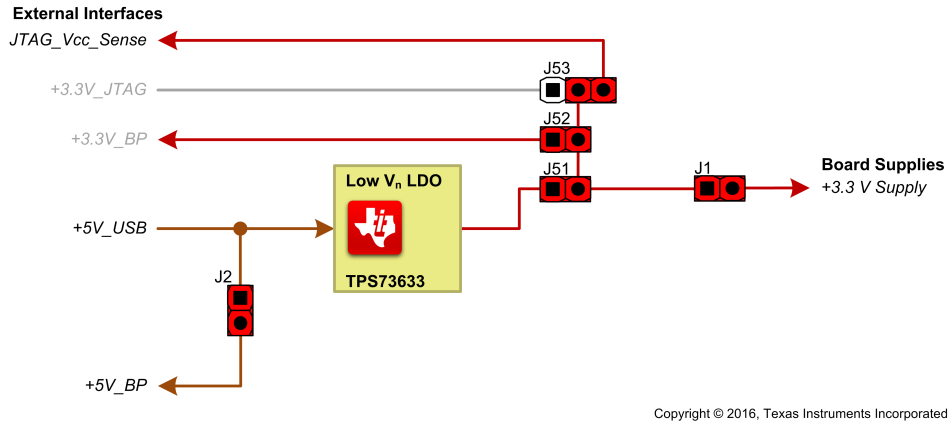

Figure 21. USB as Voltage Source

Table 7 lists the power supply jumper positions.

Table 7. Power Supply Jumper Positions

VOLTAGE SOURCE	JP51	JP52	JP53	JP2	JP1
JTAG	Open	Open	1-2	Open	Installed
BoosterPack	Open	Installed	2-3	Open	Installed
USB	Installed	Installed	2-3	Installed	Installed

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

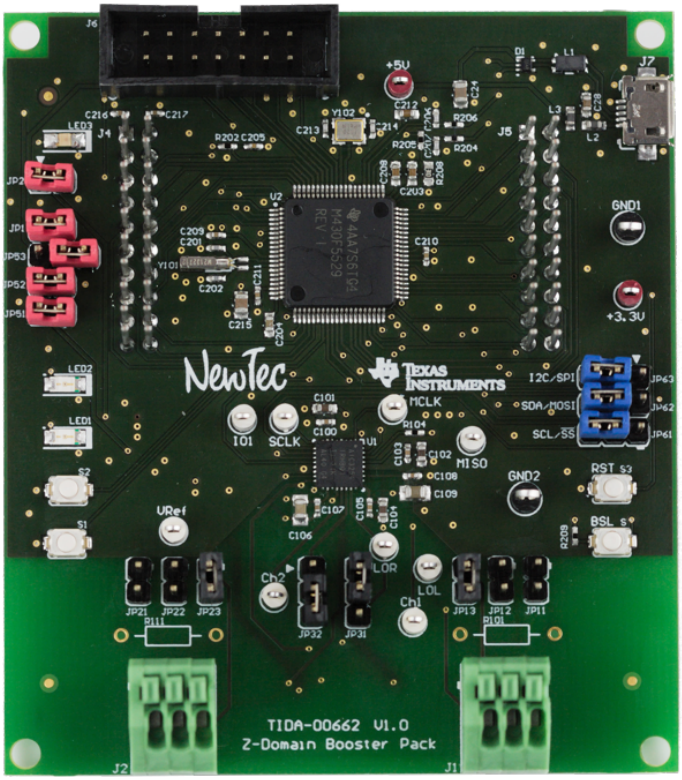

Figure 22. TIDA-00662 Board Overview

1. Check that the jumpers are in the right default position. Table 8 shows the necessary settings of the jumpers for starting the example code. The positions can be compared to the jumper positions in Figure 22, also.

Table 8. Default Jumper Positions

DESIGNATOR	DEFAULT POSITION	DESCRIPTION	SELECTED FUNCTION
JP1	Installed	Current measurement	Must always be installed to power the board
JP2	Open	+5-V BoosterPack connect	—
JP11	Open	R1x connect	—
JP12	Open	R11 connect	—
JP13	Installed	R12 connect	200-kΩ reference resistor
JP21	Open	R2x connect	—
JP22	Open	R21 connect	—
JP23	Installed	R22 connect	200-kΩ reference resistor
JP31	1-2	Voltage reference selection	V_{Ref} selected as voltage reference
JP32	2-3	Single and dual channel selection	Dual channel selected
JP51	Installed	+3.3-V source selection-USB	USB selected as power source
JP52	Open	+3.3-V source selection-BoosterPack	—
JP53	2-3	+3.3-V source selection-JTAG	JTAG $V_{CC_}$Sense

Table 8. Default Jumper Positions (continued)

DESIGNATOR	DEFAULT POSITION	DESCRIPTION	SELECTED FUNCTION
JP61	2-3	SPI/I^{2}C Selection between /SS and SCL	I^{2}C: SCL selected
JP62	2-3	SPI/I^{2}C Selection between MOSI and SDA	I^{2}C: SDA selected
JP63	2-3	SPI/I^{2}C Selection between +3.3 V and GND	I^{2}C selected (connected to GND)

2. Connect the capacitive sensor element with a capacitance of 50 to 150 pF to channel 1 of the TIDA-00662. The element must be connected to the pins 1 (V_{REF}) and 2 (operational amplifier, connected to analog input pin IN2_L of the AIC3254), which are the left and the middle pins of the terminal block J1.
3. Connect the USB to the TIDA-00662 to power the evaluation board.

3.1.2 Software

3.1.2.1 Software Setup

1. Ensure to complete the steps in Section 3.
2. Install the Code Composer Studio™ (CCS) software. For the development of the sample code, version 6.1.2.00015 was used.
3. If not done already, connect the TIDA-00662 to the USB (additional power supply options are described in Section 2.3.7).
4. The following procedure applies when using a Windows® operating system. After connecting to the PC, the TIDA-00662 should be recognized automatically as a USB device called *MSP430-USB Example*, without a valid driver (see Figure 23).

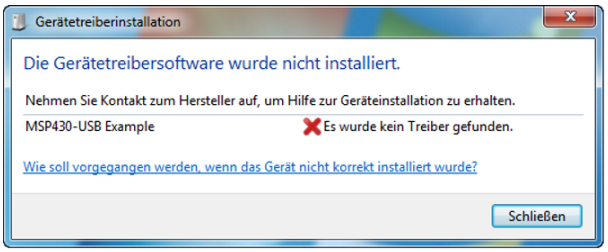

Figure 23. Driver Not Available

5. To use the sample code delivering measured values instantly to a terminal program (for example, Putty) users must install the USB drivers provided with the CCS-Project. With these drivers the TIDA-00662 is recognized as a Communication Device Class (CDC), which generates a virtual COM-port. To do so, follow this excerpt of TI's examples guide *MSP430 USB API Stack* (pages 20 to 29).

3.1.2.1.1 CDC Interfaces on Windows: INF Files and Device Installation

On the Linux® and MacOS®, CDC interfaces load silently, meaning no user action is required; a COM port simply becomes available. The same is true for HID and MSC interfaces on the Windows, Linux, and MacOS. However, the first time a particular device containing a CDC interface is attached to Windows, a device installation process is required. All Windows drivers require an INF file to associate the binaries of a driver with a given device. For the HID and MSC drivers, these INF files are contained within the Windows installation. For the CDC driver, unfortunately it is not, which means it must be provided somehow by the user.

The USB Descriptor Tool of the MSP430 generates the INF file, customized for the exact interface set of the device and VID/PID. Each example contains a TI signed INF file along with the catalog file, in the *\USB_config* directory. Steps for installing this INF file on Windows 7, and Windows 8 are described in the following sub-sections. But first, the concept of driver signing must be addressed.

3.1.2.1.1.1 INF Signing

Microsoft® requires device drivers be signed. Signing requires submission to Microsoft. Although the CDC driver binaries (usbser.sys) are native to Windows and are not changed by the OEM, the INF file contains the VID and PID for the product of the vendor, which does change. Microsoft interprets this VID/PID change as a custom driver and requires it be re-signed. Since each OEM is intended to have a slightly different INF file (with its own VID/PID), it's difficult for TI to solve this problem for its customers.

If the INF file has not been signed, Windows 7 still accepts it, after the user approves the installation of an unsigned driver. Windows 8 does not accept it, unless the user has taken special, unusual actions to allow it, described in Section 3.1.2.1.1.3. The result of the signing process is a CAT file. Including this file in the same directory as the INF file and referencing it within the INF file causes Windows to bypass asking the user to approve installation of an unsigned driver.

3.1.2.1.1.2 Installing a CDC Interface on Windows 7

When users build and run a CDC example for the first time, Windows 7 does not display a dialog box for installing the INF file. Instead, a bubble in the system tray may appear, indicating that drivers were not installed.

1. To install the INF file, launch the Device Manager. The USB CDC examples appear in the Device Manager as *MSP430-USB Example*. If a driver is not properly installed, it appears with a yellow exclamation point on its icon, sometimes referred to as a *yellow bang*. Right-click on that item (see Figure 24).

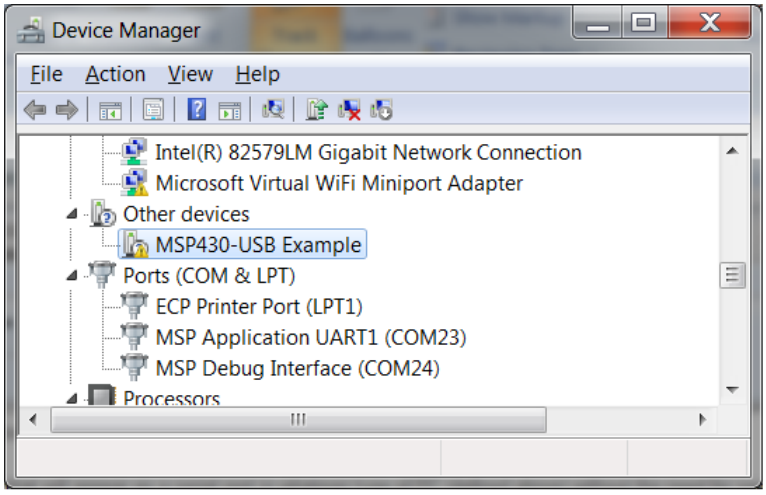

Figure 24. Device Manager Showing CDC Driver Not Installed

2. From the resulting contextual menu, select *Update Driver Software* (see Figure 25).

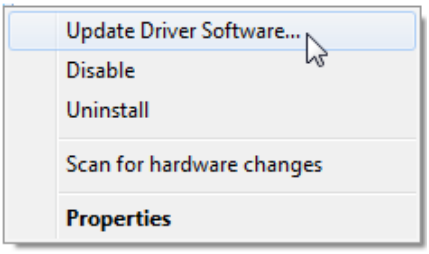

Figure 25. Update Driver Software Option

3. Choose the *Browse My Computer for Driver Software* option (see Figure 26).

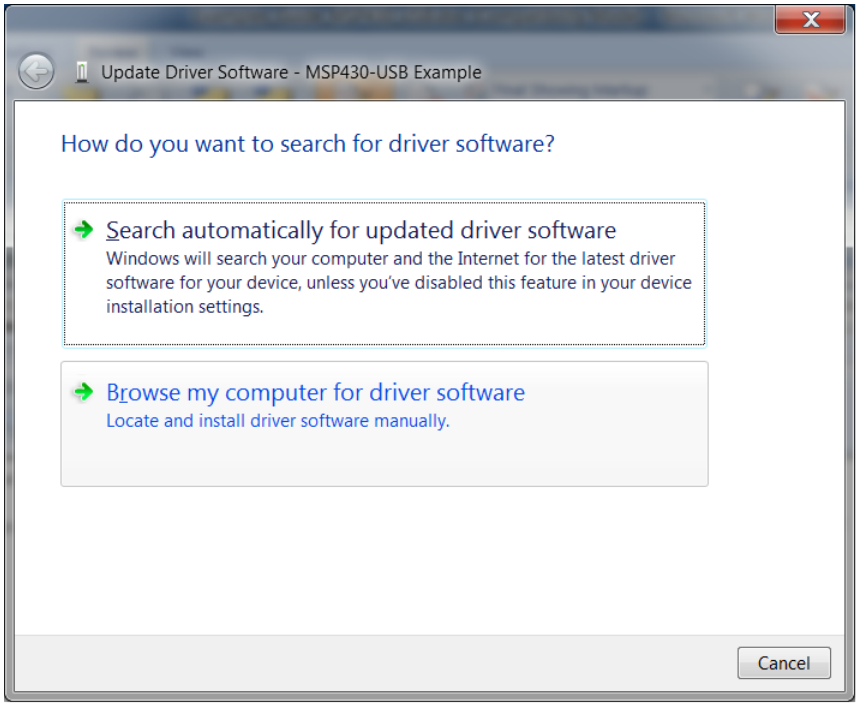

Figure 26. Update Driver Software Window

4. Navigate to the *\USB_config* directory for the CDC example in question (see Figure 27). Be sure to select the right folder for the example. Then, click the *OK* button.

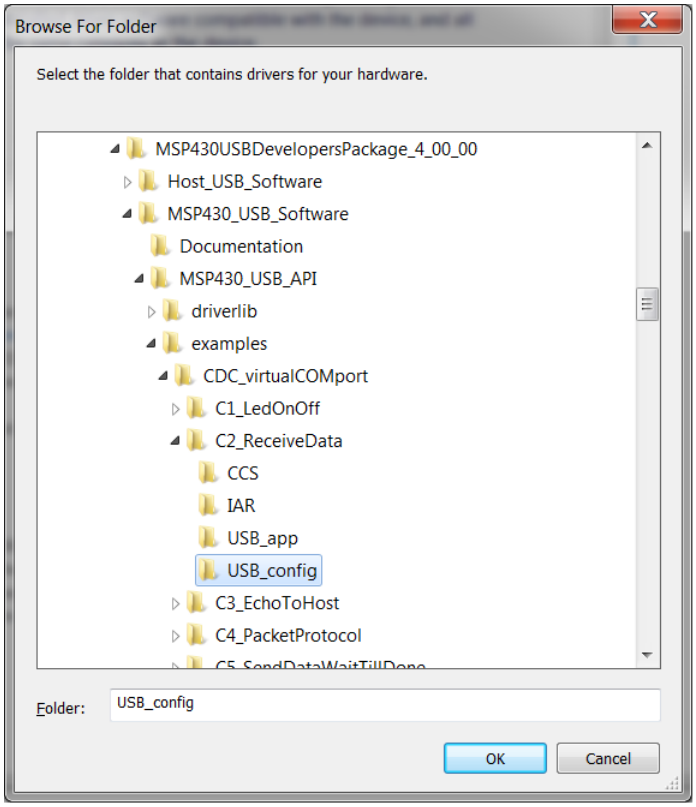

Figure 27. Project Content With USB_Config

5. Windows 7 displays the Windows Security message shown in Figure 28. Click the *Install* button.

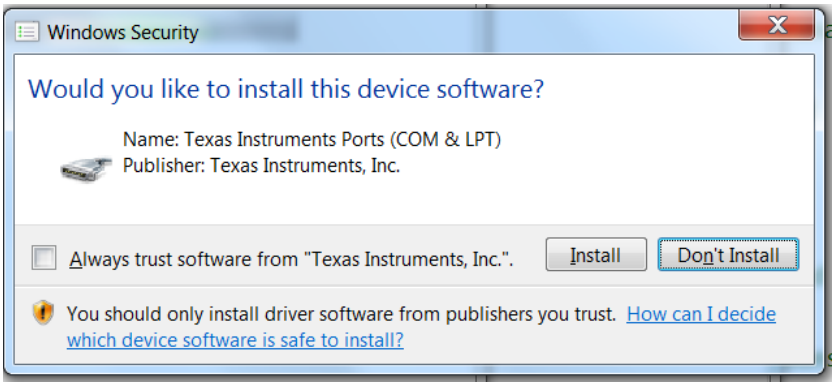

Figure 28. Windows Security Dialog Box

The Device Manager now shows the device without the yellow exclamation point icon, with an assigned COM port number (see Figure 29).

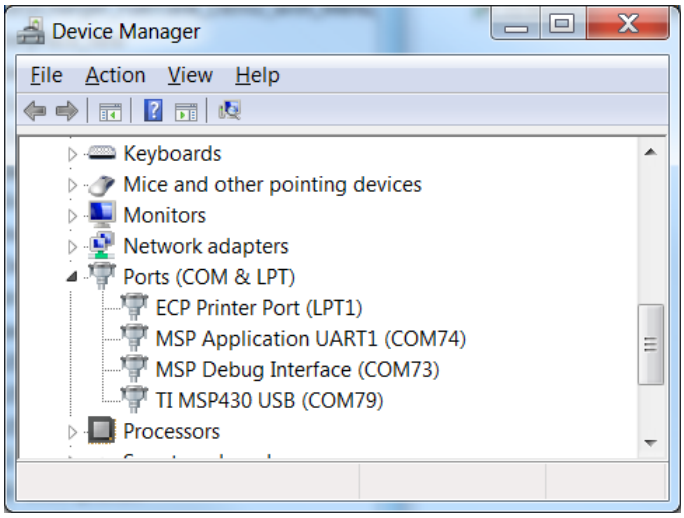

Figure 29. Device Manager With Fully-Installed CDC Interface

NOTE: If the Device Manager lists the COM port as anything greater than nine, verify that the general purpose *terminal* application such as HyperTerminal® being used supports COM ports greater than nine.

3.1.2.1.1.3 Installing a CDC Interface on Windows 8

Unlike Windows 7, which allows installation of an unsigned driver (or INF file) if the user grants permission, Windows 8 does not, under normal conditions. However, in implementing this restriction, Microsoft still provided a means of turning it off to allow driver development, because a driver can not be signed until after it is completed. Under normal conditions, attaching a device with a CDC interface, for which no signed INF was pre-installed, results in this dialog box shown in Figure 30.

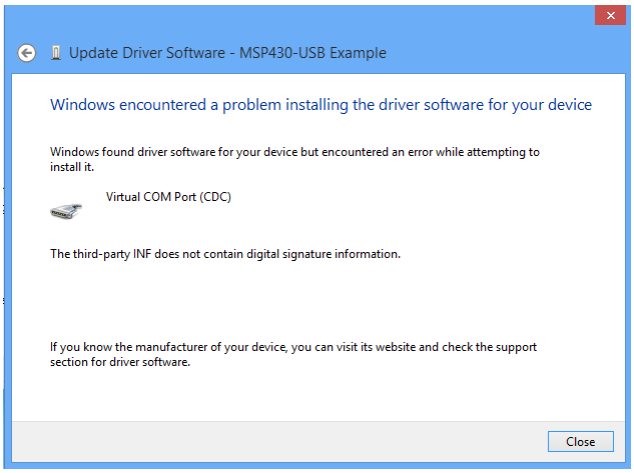

Figure 30. Windows 8 Response to Attaching CDC Device, Without Pre-Installed Signed INF

The solution Microsoft provides is a relatively hidden means of disabling enforcement of driver signage. The disabling is effective until the next reboot. The device/INF can be installed during that boot session and then during subsequent boot sessions, Windows 8 sees the installed driver and does not generate the dialog box previously shown. To enable this mode:

1. Simultaneously press the Windows key and R key to launch the *Run* window.
2. Type *shutdown.exe /r /o /f /t 00* in the Open field, then press the *OK* button (see Figure 31). A reboot occurs and the advanced startup menu is displayed (see Figure 32).

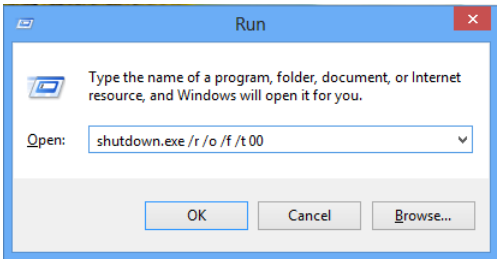

Figure 31. Step 1: Disable Windows 8 Driver Enforcement

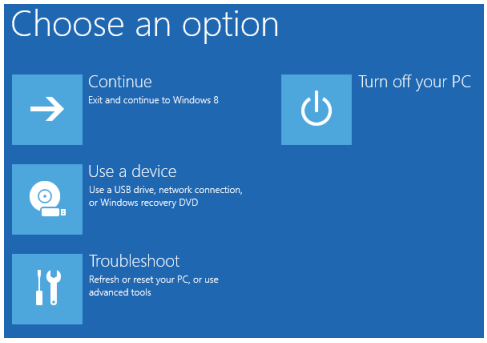

Figure 32. Step 2: Disable Windows 8 Driver Enforcement

3. Select *Troubleshoot → Advanced Options → Startup Settings*.

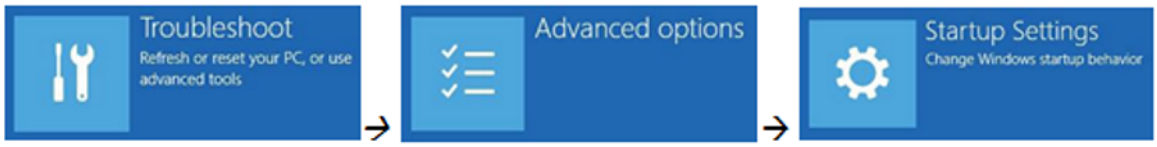

Figure 33. Step 3: Disable Windows 8 Driver Enforcement

4. Select the *Restart* button in the bottom right corner and wait for the reboot.

Figure 34. Step 4: Disable Windows 8 Driver Enforcement

5. When the computer restarts, select the option *Disable driver signature enforcement*.

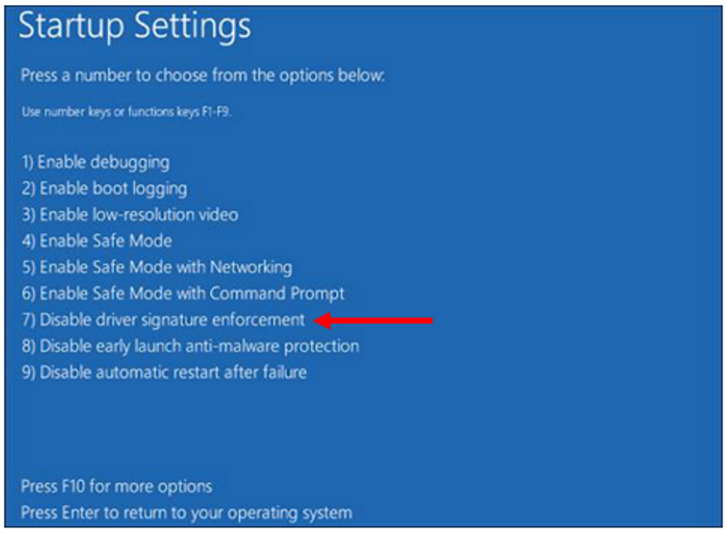

Figure 35. Step 5: Disable Windows 8 Driver Enforcement

6. When the driver finally boots into the operating system, users can manually install the unsigned driver. The message in Figure 36 appears, select the *Install this driver software anyway* option.

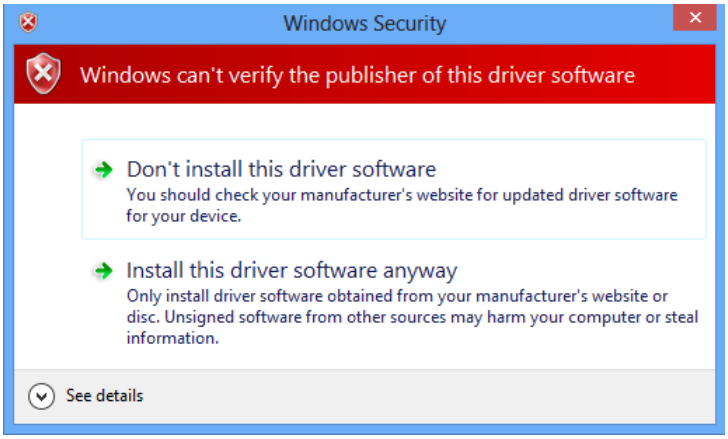

Figure 36. Install Driver After Disabling Enforcement

The disabling lasts for one boot session. In the next reboot, enforcement of driver signage resumes.

3.1.2.1.1.4 Using Caution When Changing VIDs/PIDs

When running the examples, it is recommended to not change the VIDs/PIDs (configured in *descriptors.h* with the Descriptor Tool). This recommendation allows the USB host to properly keep track of the device information associated with each VID/PID. If the host PC encounters a VID/PID it has seen previously, it assumes the descriptor set has not changed. If the descriptor set has in fact changed, the host gets confused. In the event you decide to create your own USB programs, a group of PIDs is provided for you to assign to them. This is the *User experimentation area*, at the bottom of the table. If you change USB descriptors during your development, be sure to use a new PID, to ensure that the host saves new information for that VID/PID. For a complete discussion on how USB VIDs/PIDs work, see the *Programmer's Guide*.

In each example, the VID is the one owned by TI MSP430: 0x2047. Some PIDs are shared by multiple examples which all share the same set of USB interfaces and descriptor sets. For example, all single-interface CDC examples use PID 0x0300. Other examples have unique PIDs. Each HID-Traditional example has a unique PID, because each has a different HID report format. Similarly, the MSC examples have unique PIDs, not necessarily because of different USB descriptors, but because the host may choose to record information about the storage volume of the device, which is different between the examples. If there is any doubt, it is always safest to provide a unique VID/PID to the host from the *User experimentation area*. This VID/PID is a set of 30 PIDs that neither TI nor anyone to whom we license our VID (through our VID-sharing program (see http://www.ti.com/msp430usb) ever uses for a product. As such, there should be no risk that these PIDs have been encountered by any host machine unless its owner or developer was the one who caused it.

3.1.2.2 Display Measured Values

1. Install and open PuTTY.
2. Select Connection type: *Serial* (see Figure 37).
3. Enter Serial line: *COM***. Users can find which COM-port is used in the Windows Device Manager – Ports (COM and LPT). See TI's *Examples Guide: MSP430 USB API Stack*.
4. The baud rate, start and stop bits, and flow control settings on the host software do not matter. This COM port is a virtual one and there is no actual UART to configure these settings on. The host operating system allows the user to configure them, but it will not have any effect on these examples.
5. Click the *Open* button.

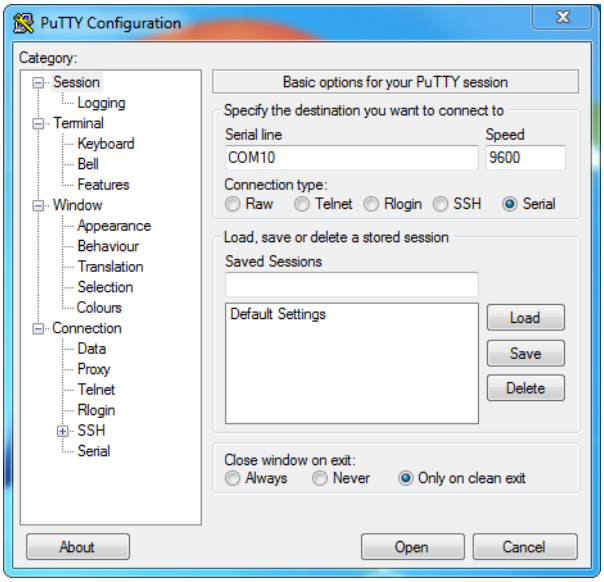

Figure 37. PuTTY Configuration

3.2 Test Setup

The test setup of the capacitance measurement with the TIDA-00662 is similar to the description in Section 3.1.1:

- The USB is used for the data output and serves as power source.
- I^2C is selected for the communication between the AIC3254 and the MSP430.
- The excitation mode is set to dual channel mode by the jumpers.
- V_{REF} is selected as voltage reference by the jumpers.
- The used reference resistor is 200 kΩ.
- Channel 1 is selected to measure the test capacitances.
- The excitation is a 12-kHz sine signal from the LOL output of the AIC3254.
- The sampling rate is set to 48 kHz.
- Each measurement includes 48 samples.

The TIDA-00662 is connected through micro USB to the PC, where the measurement results are shown on an installed USB terminal (PuTTY). To qualify the measurement results, reference measurements of the capacitances have been captured with the LCR-meter GW Instek LCR-6100.

The calibration of the phase offset and the capacitances is necessary before the test measurement can be started:

1. Measure the phase offset by shorting the reference resistance (pin 2 and pin 3 of terminal Block J1).
2. Connect the first capacitance to channel one. On the USB terminal, the input value can be entered and the respective measurement result is saved (C_{Input1}, C_{Meas1}).

3. Repeat the same procedure with the second capacitance (C_{Input2}, C_{Meas2}).

Once the calibration values are captured and saved, the measurement starts and the capacitances within the calibration range are tested. In order to correct the measurement values, the MSP430 performs a two-point calibration with the saved values of the calibration using Equation 1:

$$C_{Corrected} = C_{Input1} + \frac{C_{Input2} - C_{Input1}}{C_{Meas2} - C_{Meas1}} \times \left(C_{Measured} - C_{Meas1}\right) \quad (1)$$

3.3 Test Data

The TIDA-00662 is tested with capacitances from 0 to 150 pF. Two test series were made with two different calibration ranges. The first one includes the area from approximately 5 to 80 pF and the second one from to 75 to 150 pF.

The following figures show the test results, including the measurement characteristic, the absolute deviation, and a selection of histograms for each of the two different measurements. The bigger the calibration range, the greater the absolute deviation becomes. Therefore, the values of the capacitances for the calibration should be adapted specifically to the respective application to get the best measurement results.

3.3.1 Calibration Range: 5 to 80 pF

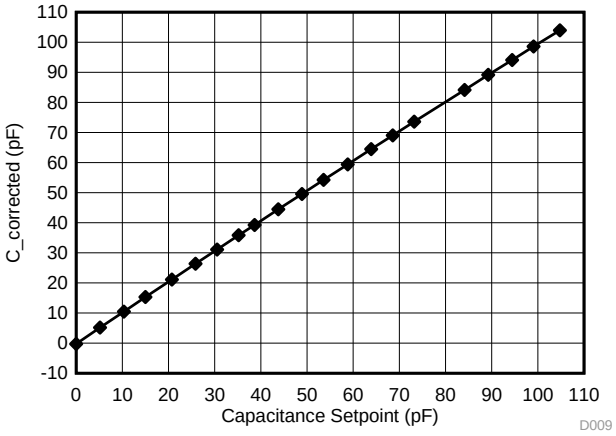

Figure 38. Measurement Characteristic 1

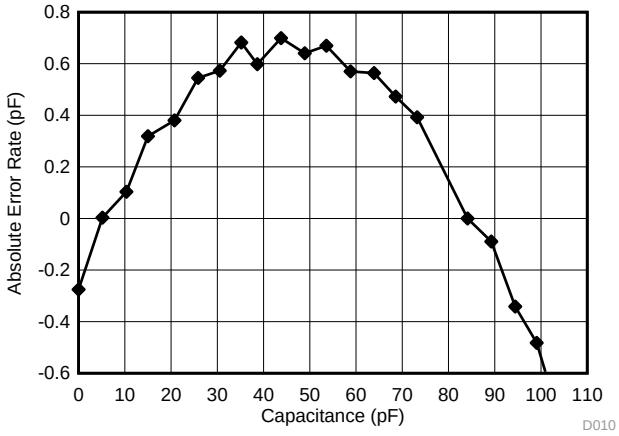

Figure 39. Absolute Error 1

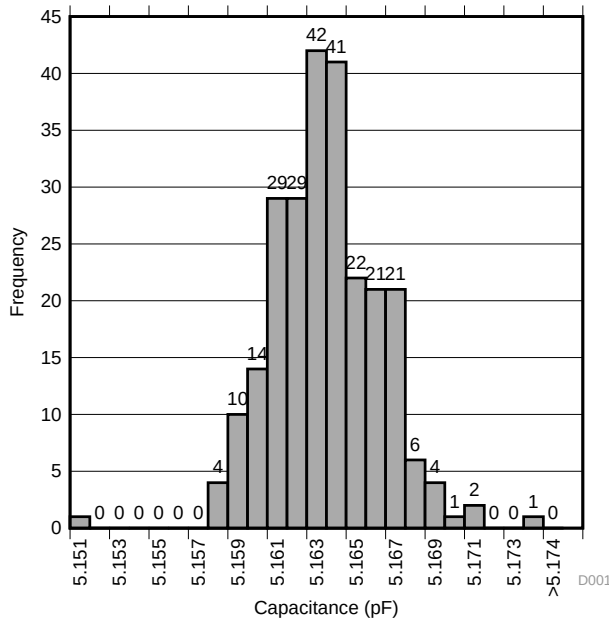

Figure 40. Histogram Value of 5.16 pF

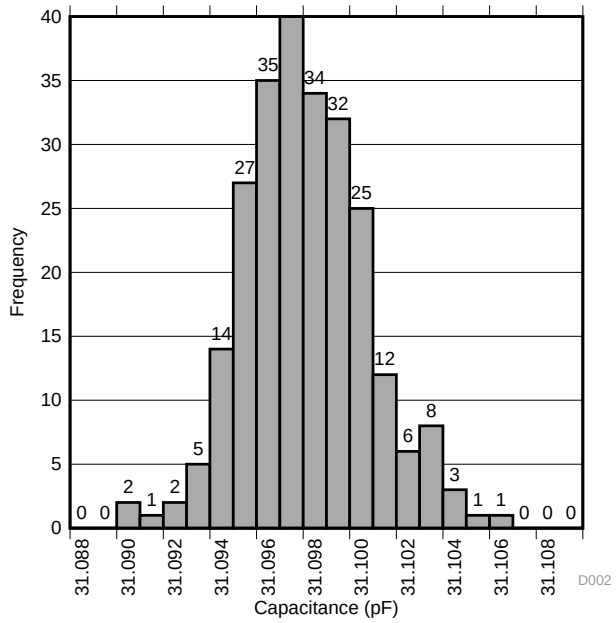

Figure 41. Histogram Value of 30.52 pF

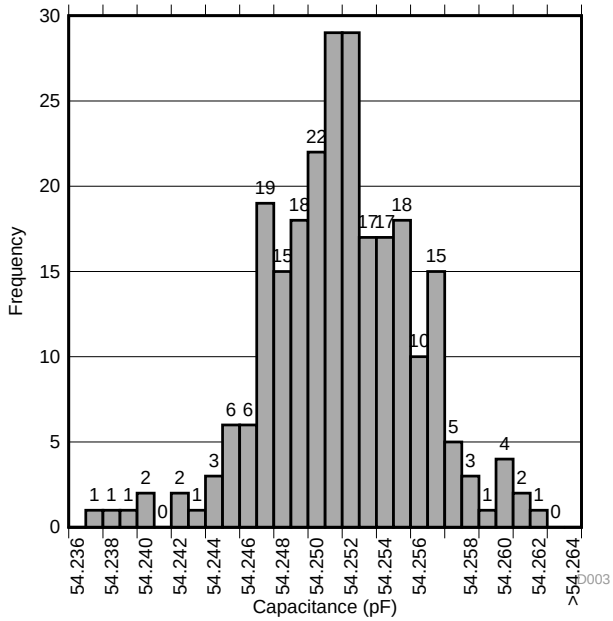

Figure 42. Histogram Value of 53.58 pF

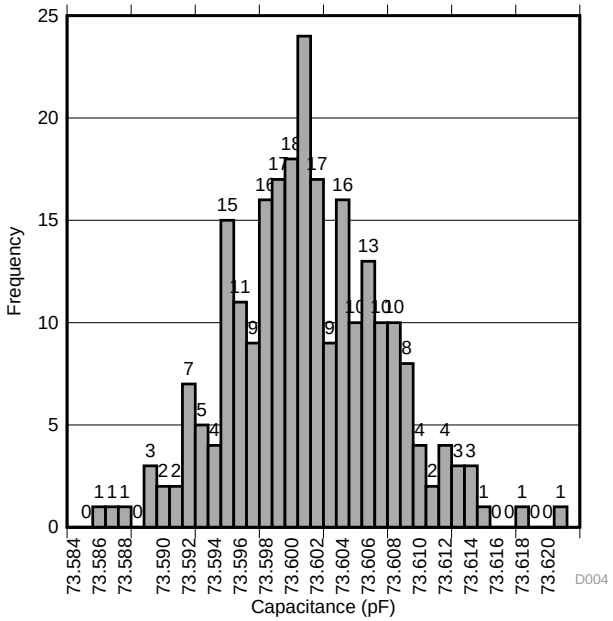

Figure 43. Histogram Value of 73.21 pF

3.3.2 Calibration Range: 75 to 150 pF

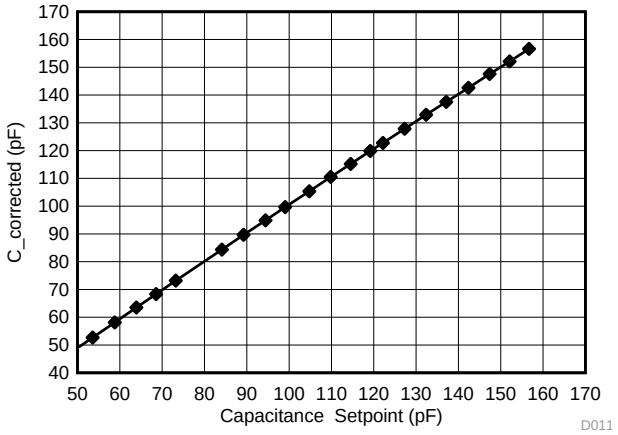

Figure 44. Measurement Characteristic 2

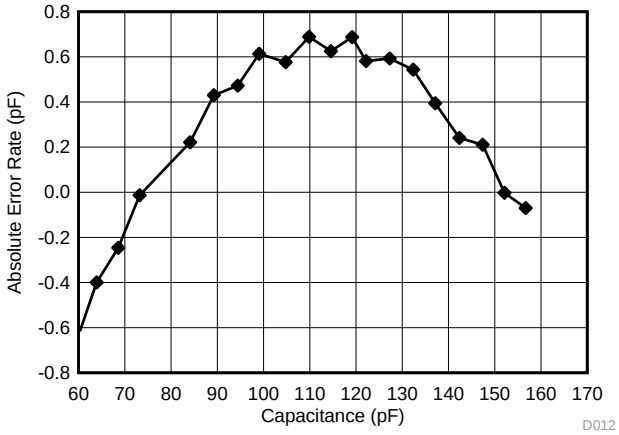

Figure 45. Absolute Error 2

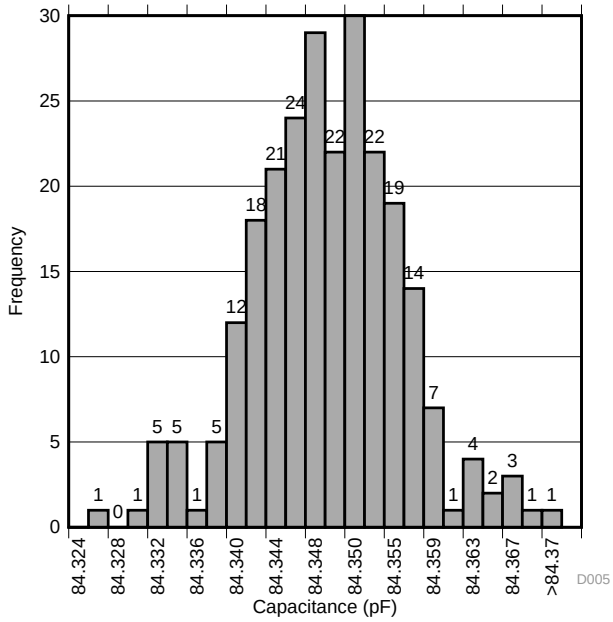

Figure 46. Histogram Value of 84.127 pF

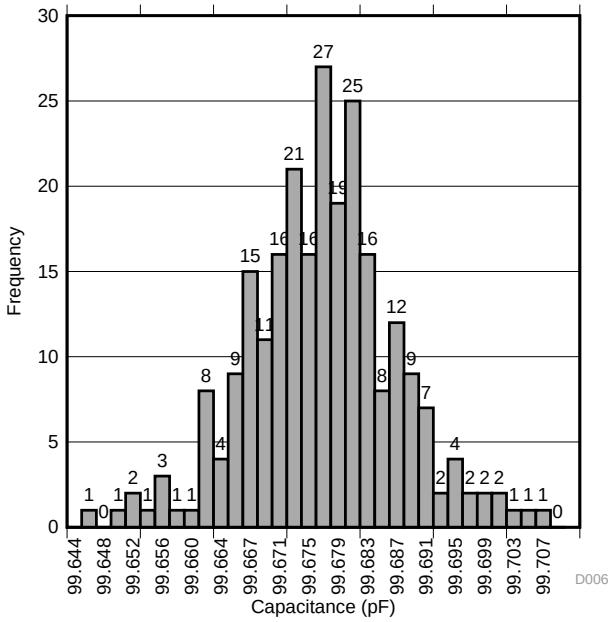

Figure 47. Histogram Value of 99.063 pF

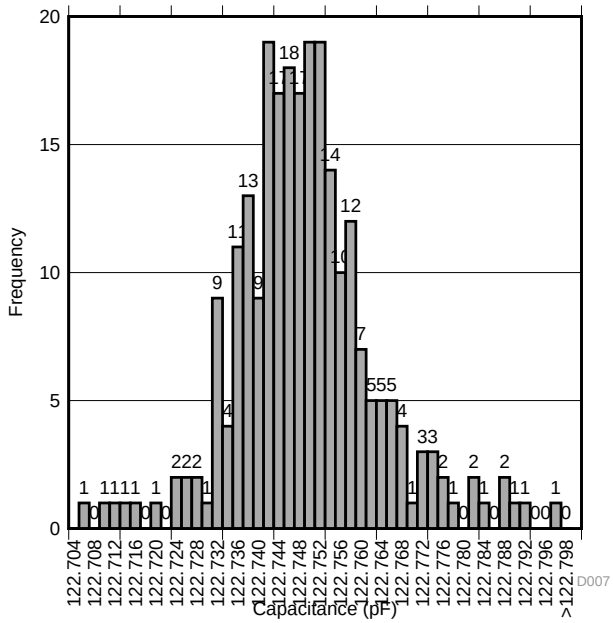

Figure 48. Histogram Value of 122.167 pF

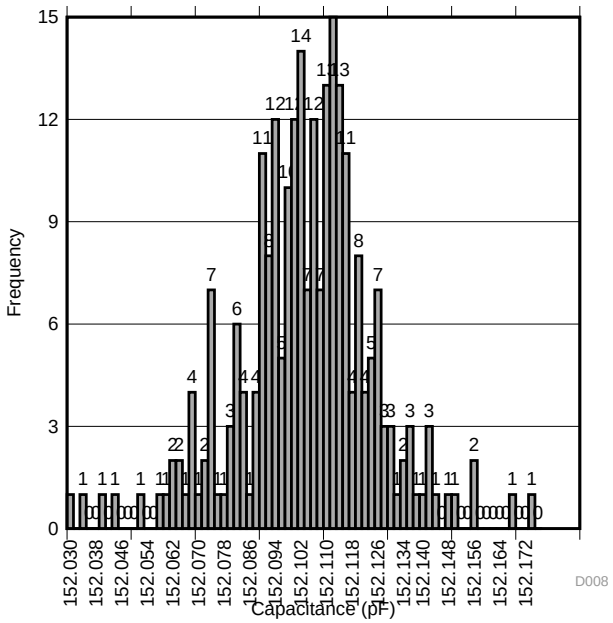

Figure 49. Histogram Value of 152.105 pF

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00662.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00662.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00662.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00662.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00662.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00662.

5 Software Files

To download the software files, see the design files at TIDA-00662.

6 Related Documentation

1. Texas Instruments, *Reference Design for Reinforced Isolation Three-Phase Inverter With Current, Voltage, and Temp Protection*, TIDA-00366 Design Guide (TIDUBX1)
2. Texas Instruments, *TLV320AIC3254 Ultra Low Power Stereo Audio Codec with Embedded miniDSP*, TLV320AIC3254 Datasheet (SLAS549)
3. Texas Instruments, *TLV320AIC3254 Application Reference Guide* (SLAA408)
4. Texas Instruments, *MSP430F552x, MSP430F551x Mixed Signal Microcontroller,* , Datasheet (SLAS590)
5. Texas Instruments, *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208)
6. Texas Instruments, *Starting a USB Design Using MSP430™ MCUs*, Application Report (SLAA457)
7. Texas Instruments, *TPD2E001 Low-Capacitance 2-Channel ESD-Protection for High-Speed Data Interfaces*, TPD2E001 Datasheet (SLLS684)
8. Texas Instruments, *MSP430 Hardware Tools User's Guide* (SLAU278)
9. Texas Instruments, *Voltage-Reference Filters*, Application Note (SBVA002)
10. Texas Instruments, *Field Transmitters and Process Instrumentation Solution Guide* (SLYY043)
11. Texas Instruments, *TPS736xx Cap-Free, NMOS, 400-mA Low-Dropout Regulator with Reverse Current Protection*, User's Guide (SBVS038)

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7 About the Authors

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Founded in 1986, NewTec looks back on more than three decades of project experience in developing complex hardware and software systems with a focus on functional safety and embedded security. NewTec aims to ensure the safety-relevant functionality of a system at all times as well as to protect embedded systems from sabotage attacks and manipulations from the outside. Today, NewTec has more than 160 employees at four locations in Pfaffenhofen/Roth, Freiburg, Mannheim, Friedrichshafen and Bremen. For more information about NewTec, visit www.newtec.de.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2016) to B Revision	Page
• Changed structure to fit current design guide template	1
• Added Section 3.2: Test Setup	33
• Changed Section 3.3: Test Data with new results and graphs	35
• Added NewTec information in Section 7	39
• Added Thomas Mack to Section 7	39

Changes from Original (August 2016) to A Revision	Page
• Changed from preview design	1

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