K2G Industrial Communications Engine (K2G ICE)

1 Introduction

This technical user's guide describes the hardware architecture of the 66AK2G02 Industrial Communications Engine (K2GICE). The 66AK2G02 is a KeyStone™ II-based DSP + ARM System-on-Chip (SoC). This chapter provides an introduction to the K2G ICE, along with the key features and block diagram.

1.1 Key Features

The K2G ICE is a high-performance, cost-efficient, standalone development platform that enables users to evaluate and develop industrial applications for the Texas Instrument's Keystone II System-on-Chip (SoC) 66AK2G02.

The K2G SoC (66AK2G02) is the new device from TI's Keystone II architecture with:

- ARM® Cortex®-A15 Microprocessor Unit (ARM A15) Subsystem at up to 600 MHz
- C66x Fixed- and Floating-Point VLIW DSP Subsystem at up to 600 MHz
- Two Programmable Real-Time Unit and Industrial Communication Subsystems (PRU-ICSS)
- Multicore Shared Memory Controller (MSMC) with 1024KB of Shared L2 RAM
- Up to 36-Bit DDR3 External Memory Interface (EMIF) with ECC (32-Bit Data + 4-Bit ECC)
- PCI-Express® 2.0 Port with Integrated PHY
- Three Multichannel Audio Serial Port (McASP) Peripherals
- Multichannel Buffered Serial Port (McBSP)
- Six Enhanced High-Resolution Pulse Width Modulation (eHRPWM) Modules
- Three Inter-Integrated Circuit (I2C) Interfaces, Three UART Interfaces, and Four Serial Peripheral Interfaces (SPI)
- Seven 64-Bit Timers
- Secure Device – Supports High Secure Boot Option
- 21 × 21 mm^2 0.8-mm pitch WBBGA

The key features of the EVM are:

- Based on the KeyStone II architecture with ARM® Cortex®-A15 @600 MHz and C66x DSP @600 MHz
- 2× PRU-ICSS, supporting multi-protocol industrial Ethernet with up to 4 ports
- 512 MByte of DDR3L
- 256 Mbit of QSPI Flash
- 32 kByte of I2C EEPROM
- Micro SD-Card slot
- 1× Gigabit Ethernet port supporting 10/100/1000 Mbps data rate on RJ45 connector
- PCIe ×1 card edge connector
- LCD display
- Expansion connector with industrial interface signals for customer designs
- On-board XDS100 JTAG Emulator Circuit
- 20-pin JTAG header to support all types of external emulator
- RoHS compliant design
- Powered by DC power-wall adaptor (24 V / 2.5 A) or PCIE Edge Connector
- 8-bit digital output LEDs
- Industrial Ethernet LEDs
- Rotary switch input
- Boot media selection using DIP switches
- Discrete Board Power Solution

CAUTION

Operation my result in high temperatures for some components. Be cautious when handling during operation.

CAUTION

Components installed on this product are sensitive to Electrostatic Discharge (ESD). Take precautions before handling this product.

1.2 REACH Compliance

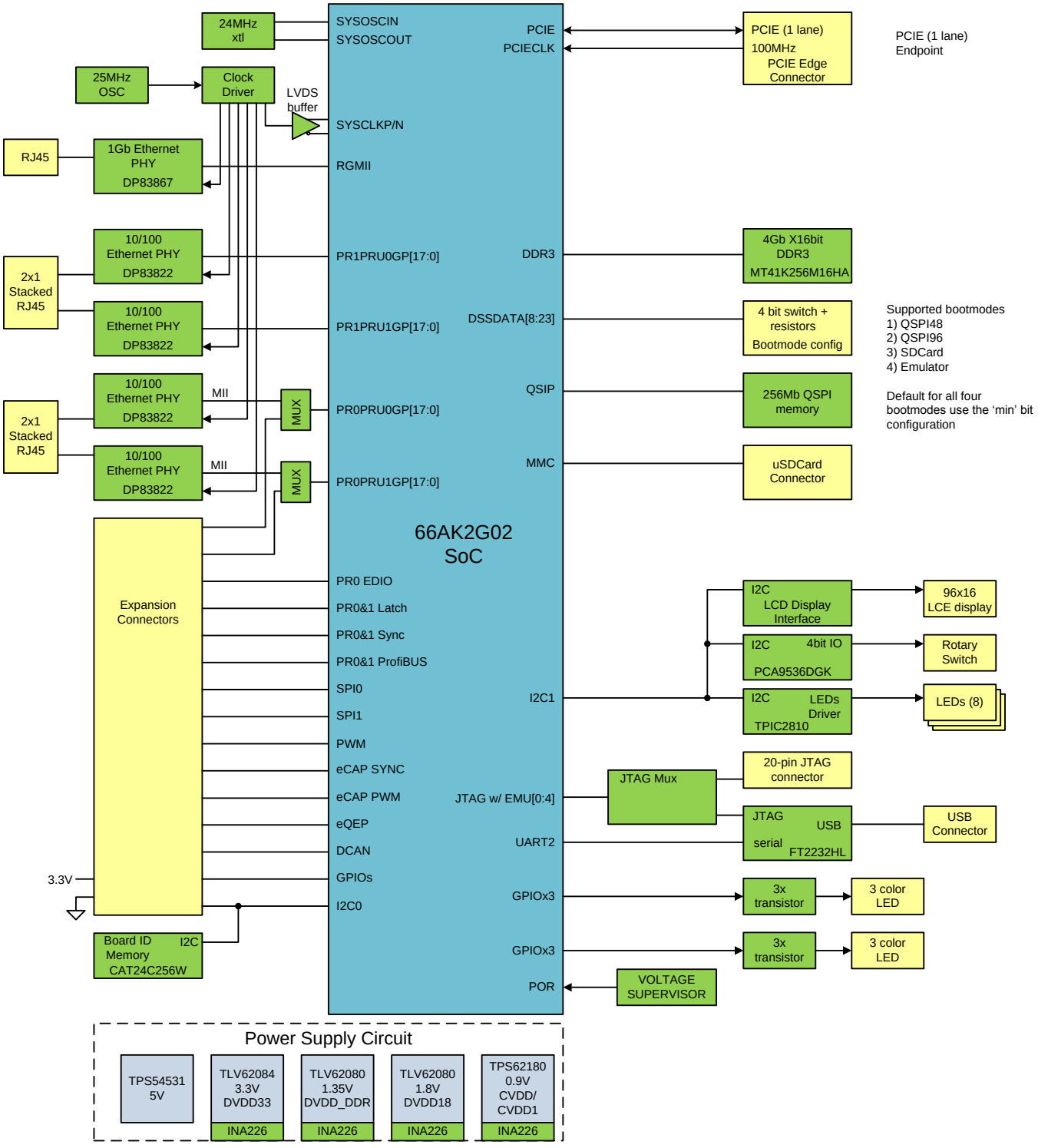
CAUTION

In compliance with the Article 33 provision of the EU REACH regulation, we are notifying you that this module includes crystals (ABM3-25.000MHz-B2-T, ABM3-12.000MHz-D2Y-T) from Abracon LLC that contains two Substance of Very High Concern (SVHC) above 0.1%. These uses from Texas Instruments do not exceed 1 ton per year. The SVHC's are Diboron trioxide CAS# 1303-86-2 and Lead Oxide CAS# 1317-36-8.

1.3 Functional Block Diagram

The functional block diagram of the K2G ICE is shown in Figure 1.

Figure 1. Functional Block Diagram



1.4 Basic Operation

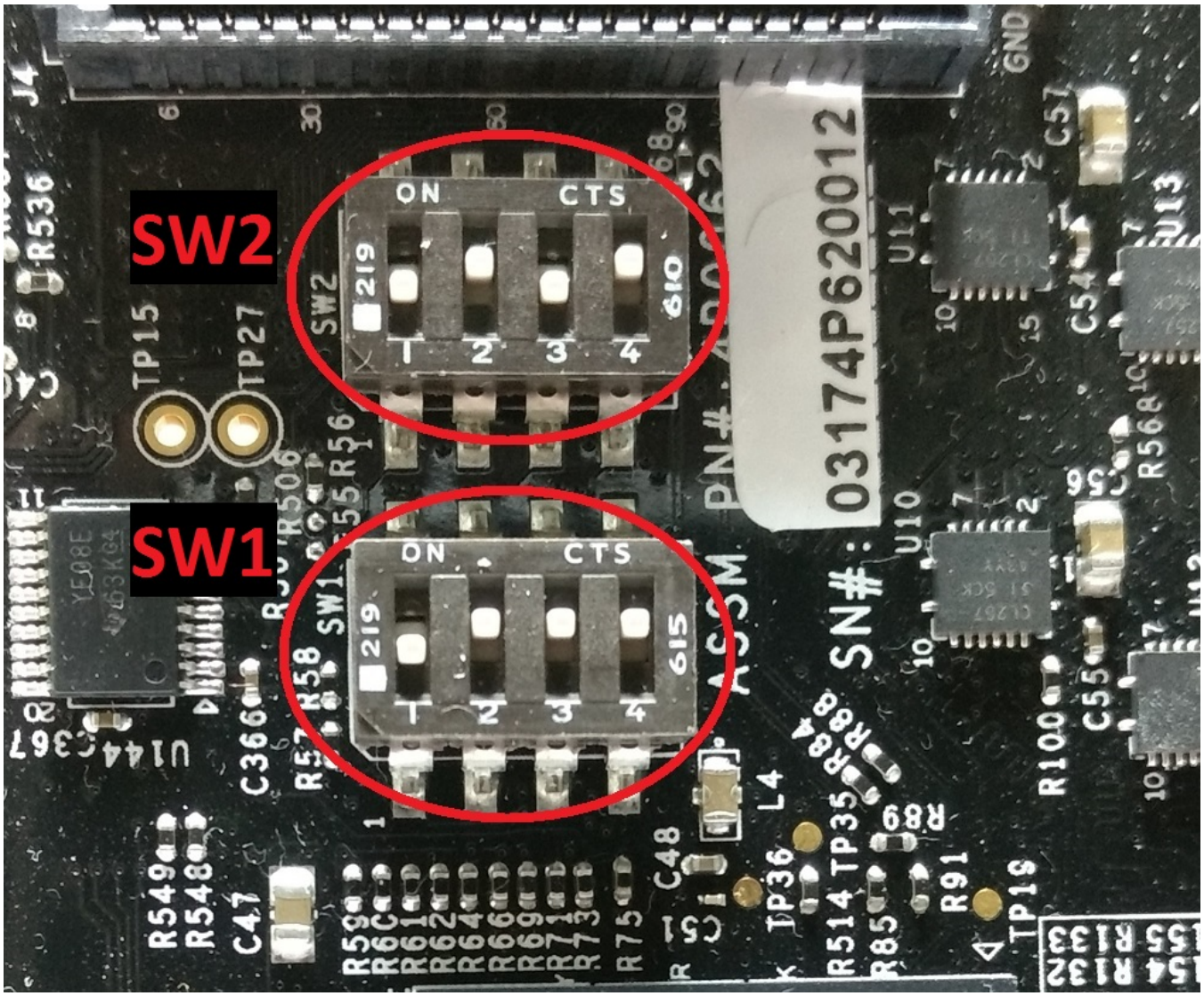
This guide provides the steps to setup and run the EtherCAT slave demo on K2G ICE. The EtherCAT slave demo is delivered with the K2G ICE board on the provided micron SDcard. Refer to this link for more details on TI's PRU-ICSS EtherCAT industrial software package.

An online version of these instructions can be found at http://processors.wiki.ti.com/index.php/Configuring_TwinCAT_For_K2GICE_EtherCAT_Slave.

1.4.1 Running the EtherCAT Slave Demo on K2G ICE

1. Confirm the boot switches are set to SD boot. Deliver the K2G ICE with the switches in this configuration, as shown in Figure 2:
   - SW1 – OFF ON ON ON
   - SW2 – OFF ON OFF ON

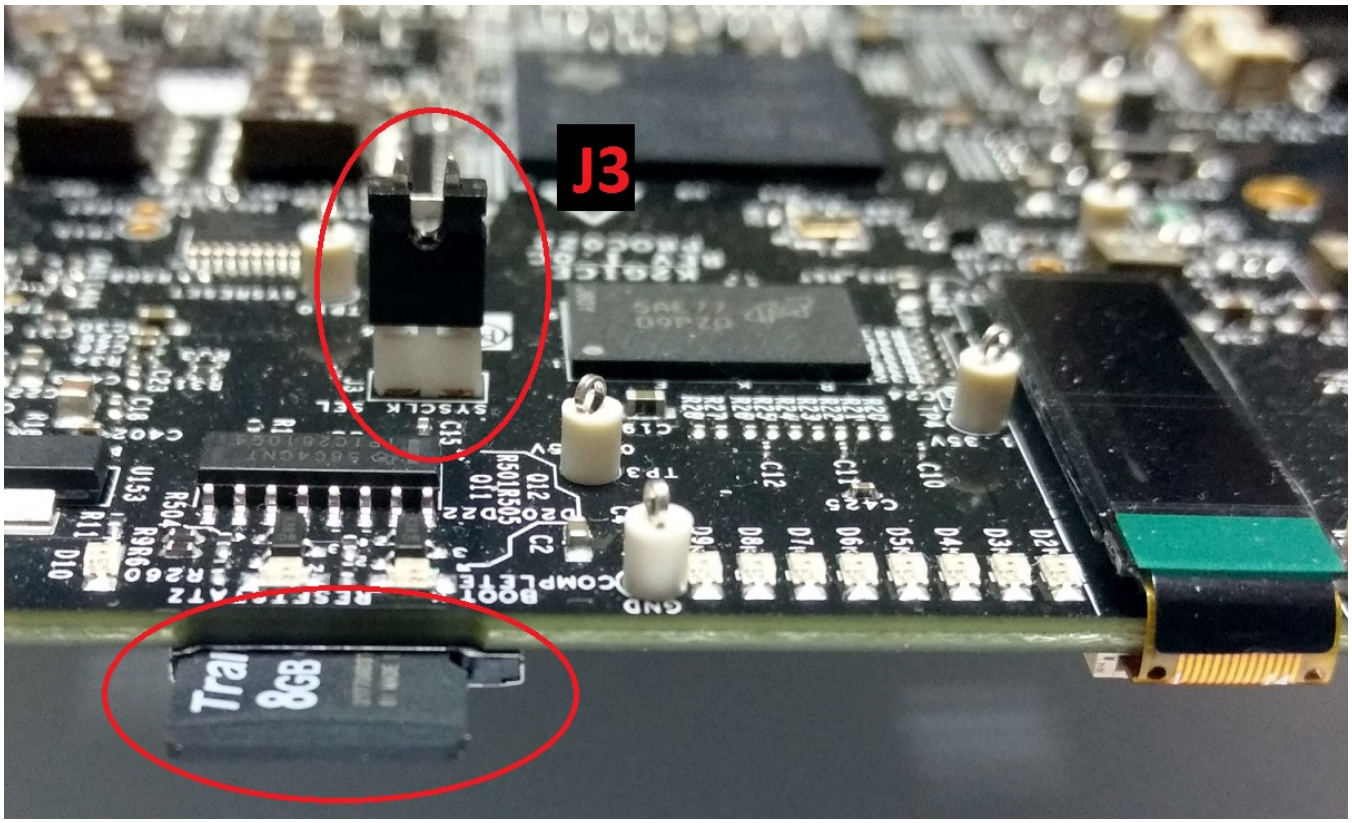
Figure 2. Switch Configuration



2. Insert the microSD card with the EtherCAT slave demo binaries into the microSD slot (bottom side of the board).

3. Select the 24-MHz crystal as the clock source for the K2G by shorting the pins jumper J3, using the shunt provided, as shown in Figure 3. The K2G ICE should be delivered with the shunt installed.

Figure 3. Short J3 Pin

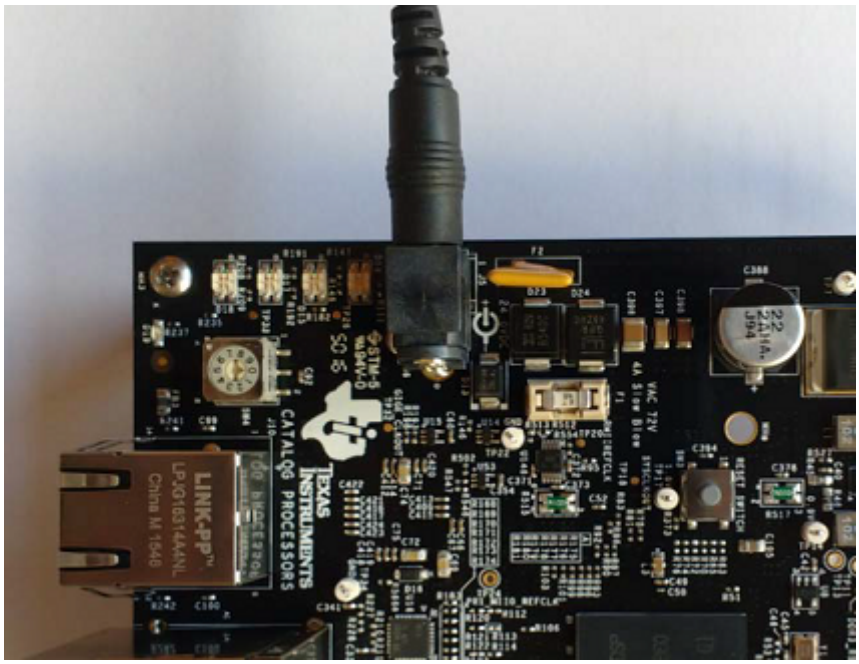


4. Connect the Ethernet cable between the K2G ICE EtherCAT IN/Port0 (J8, lower RJ-45 port) and the PC with the TwinCAT installation, as shown in Figure 4.

Figure 4. Connect Ethernet Cable

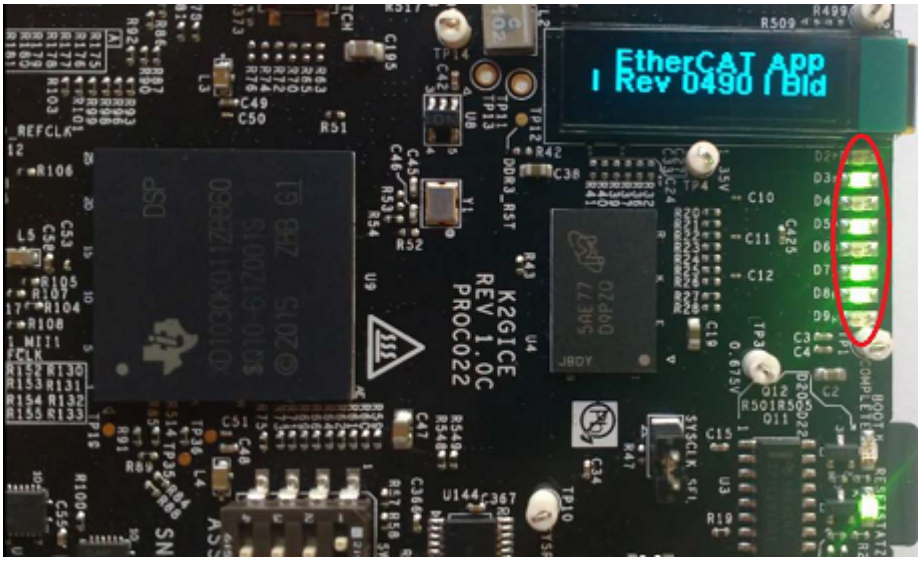
5. Apply +24 V to the K2G ICE with either a bench power supply or with a +24-V power supply purchased separately, as shown in Figure 5.

Figure 5. Apply +24 V to K2G ICE



6. Observe that the message 'EtherCAT APP' appears on the OLED display. Also observe the LEDs for the pattern shown in Figure 6 to confirm that EtherCAT application has started.

Figure 6. LED Pattern



The K2G ICE is now acting as an EtherCAT slave, and the industrial LEDs can be lit using instructions from an EtherCAT master using the TwinCAT application. Instructions for installing and operating the TwinCAT application can be found in the K2G ICE User's Guide.

1.4.2 Setting Up the TwinCAT Application

1. Download and install the PRU-ICSS EtherCAT Industrial software package from http://software-dl.ti.com/processor-industrial-sw/esd/PRU_ICSS_EtherCAT_Slave/latest/index_FDS.html. Refer to the documentation under *{EtherCAT_package_install_path}\docs* for more details on PRU-ICSS EtherCAT industrial software package.
2. TwinCAT software setup:
   a. Install TwinCAT (evaluation version is available for download from http://www.beckhoff.co.in/english.asp?download/tc3-download-xae.htm. Select PLC mode for installation and check the IO drivers box).
   b. For EtherCAT Slave Demo application: copy *{EtherCAT_package_install_path}\examples\ethercat_slave\esi\TiEtherCATLib.xml* to the *<Drive>:\TwinCAT\Io\EtherCAT* folder. If using TwinCAT 3.1, the folder path is *<Drive>:\TwinCAT\3.1\Config\Io\EtherCAT*.
   c. For EtherCAT Slave Full Mode application: copy *{EtherCAT_package_install_path}\protocols\ethercat_slave\ecat_appl\esi\TI_ESC.xml* to the *<Drive>:\TwinCAT\Io\EtherCAT* folder. If you are using TwinCAT 3.1, the folder path is *<Drive>:\TwinCAT\3.1\Config\Io\EtherCAT*.
3. Start TwinCAT XAE (VS 2010) from the Start menu. Create a new TwinCAT XAE Project (XML format), as shown in Figure 7 and Figure 8.

Figure 7. Create New Project

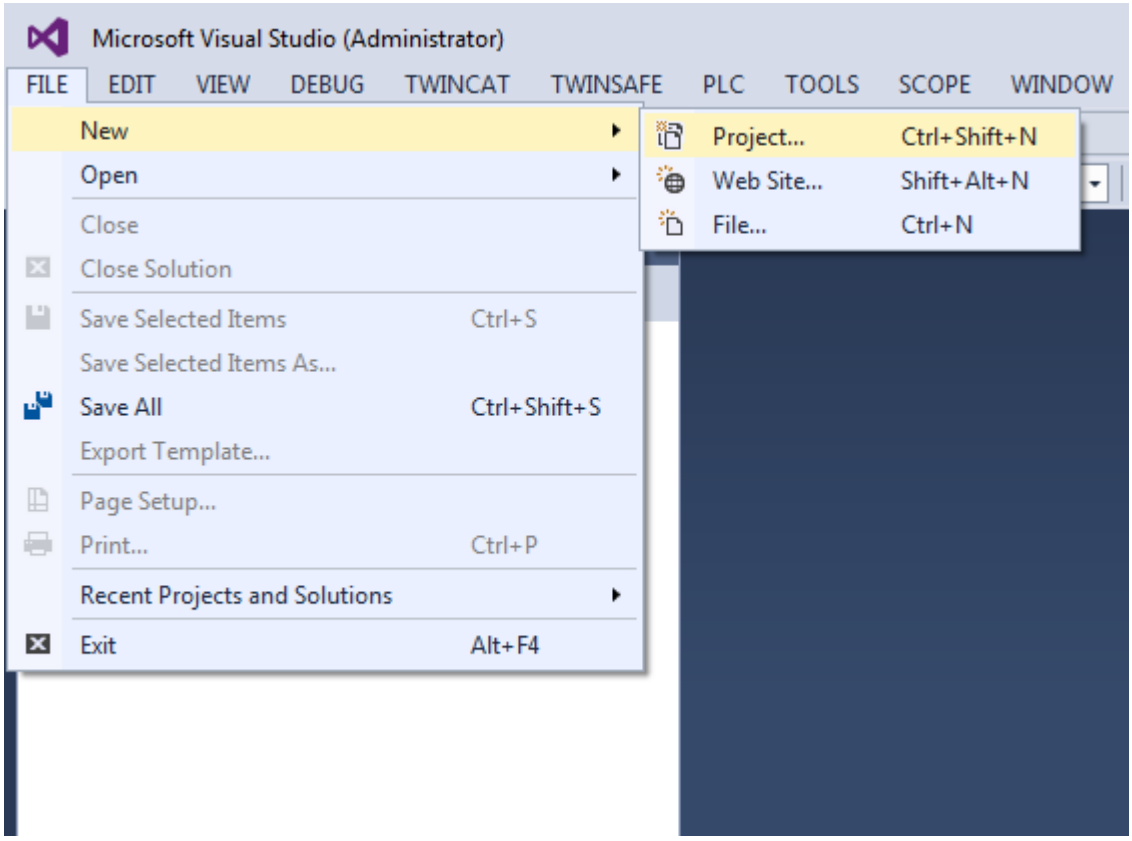
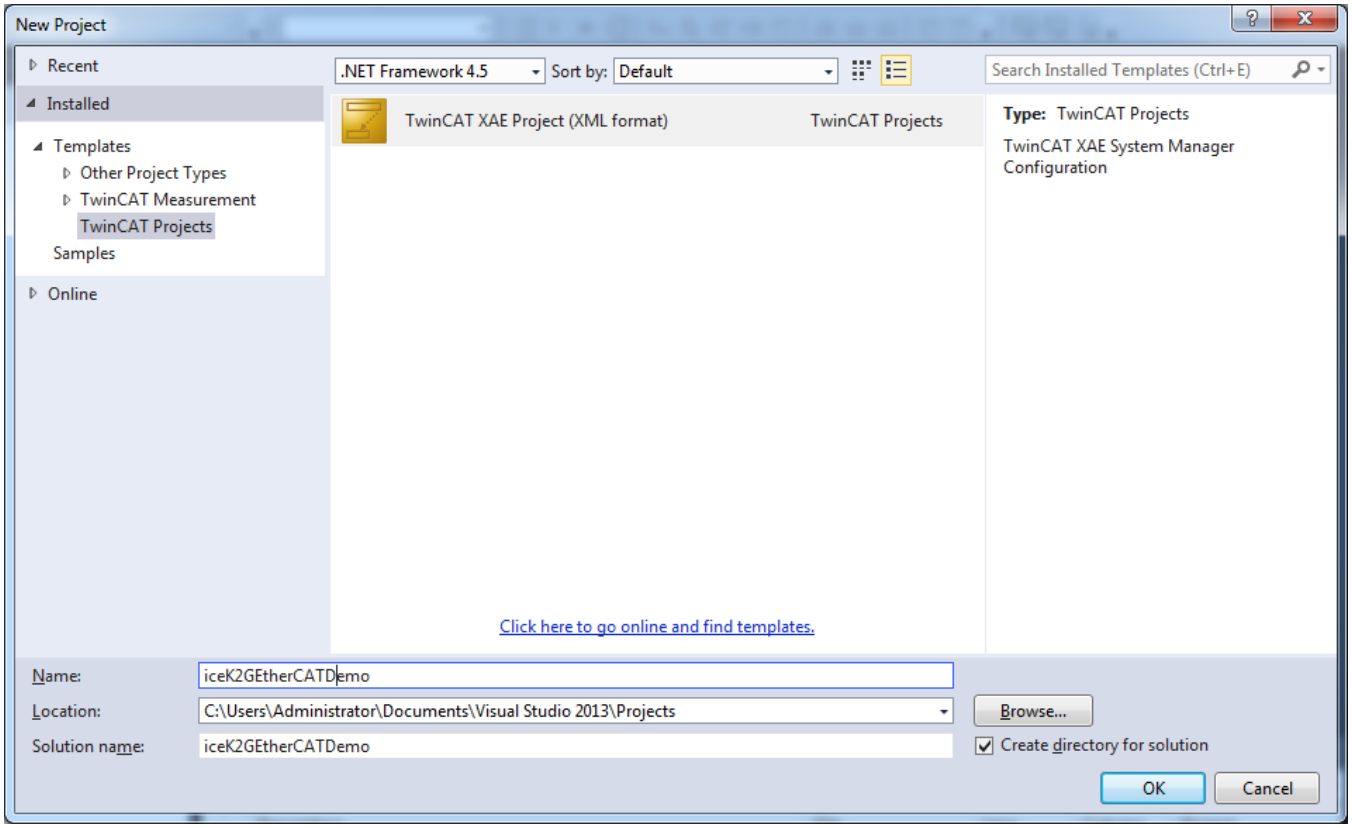
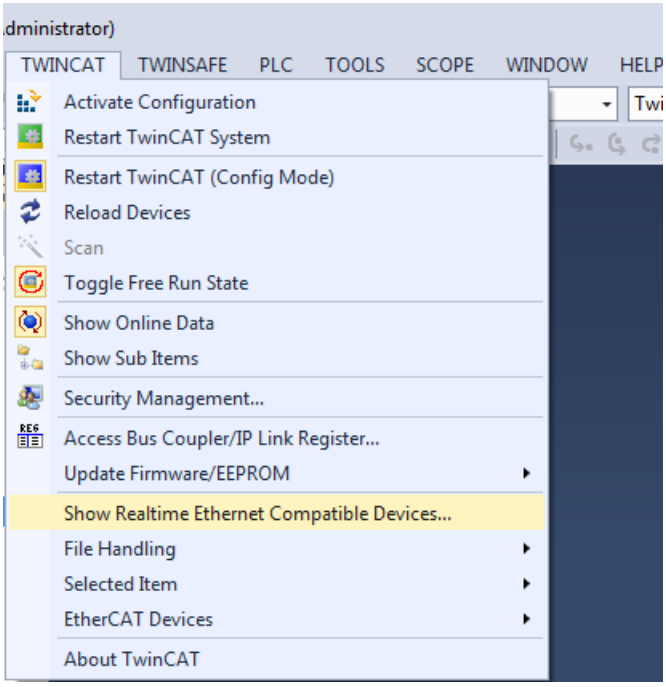


Figure 8. New TwinCAT XAE Project



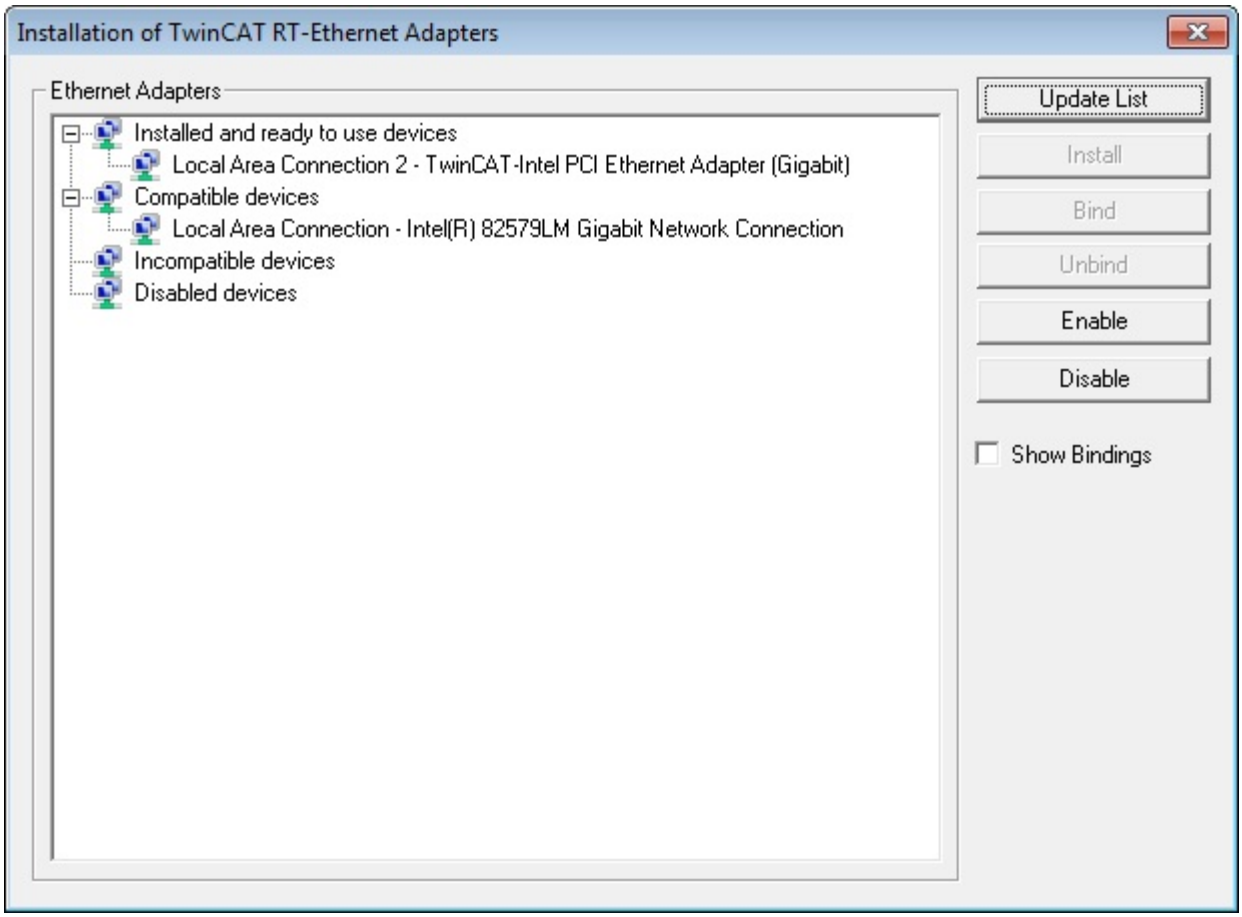
4. On first occurance, the user must set the PC's Ethernet port, which is used as the EtherCAT port. Go to TwinCAT > Show Realtime Ethernet Compatible Devices, as shown in Figure 9.

Figure 9. Show Realtime Ethernet Compatible Devices



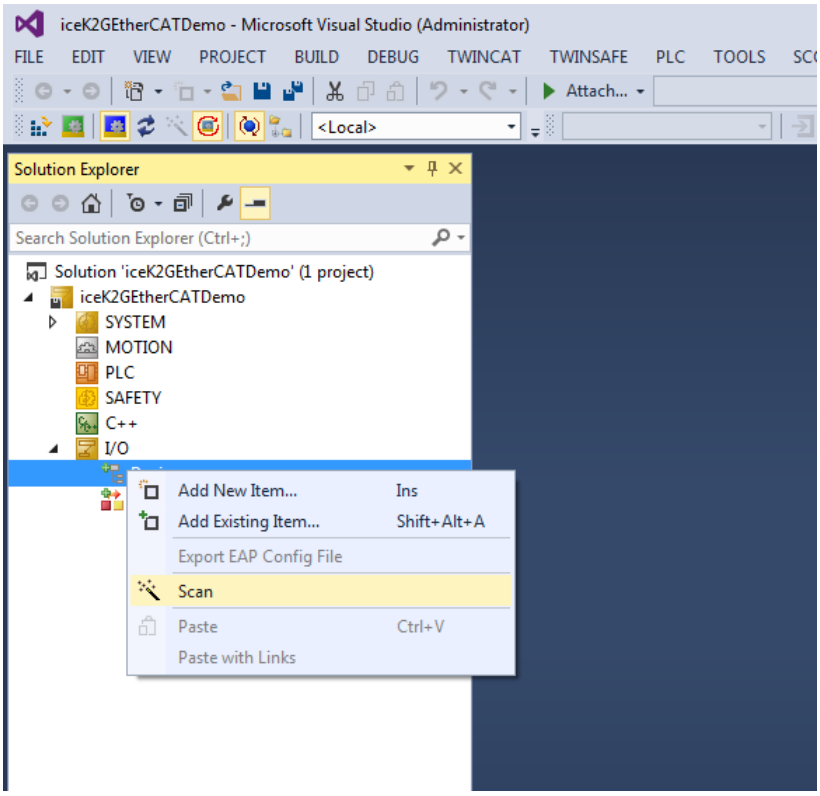
5. Select the Ethernet port from the list of compatible devices, and press Install. This installs a Beckhoff EtherCAT driver. When installed, the Ethernet port appears in Installed and ready to use devices, as shown in Figure 10.

Figure 10. Installed and Ready to Use Devices



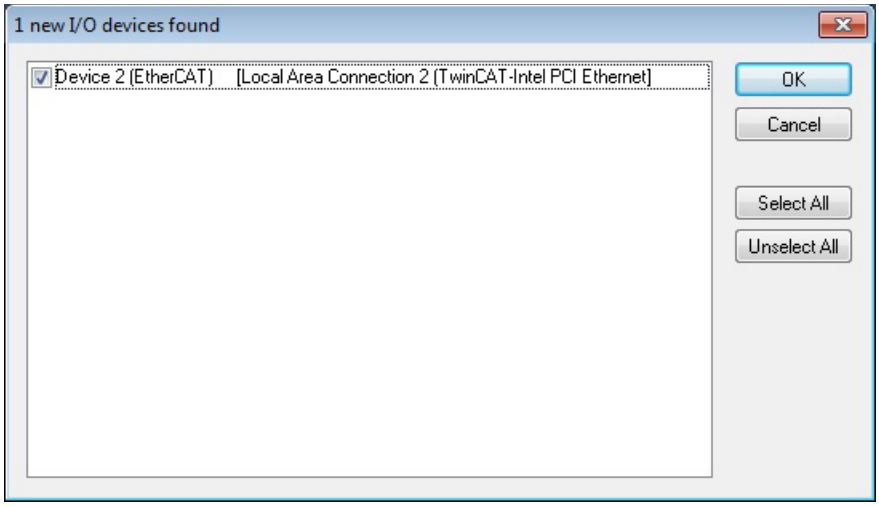
6. In Solution Explorer, go to the new *TwinCAT project > I/0 > right click on Devices*, and select Scan as shown in Figure 11. Press OK in the next dialog to start scanning for EtherCAT devices. If Scan Boxes is grayed out, select TWINCAT > Restart TwinCAT (Config Mode).

Figure 11. Select Scan



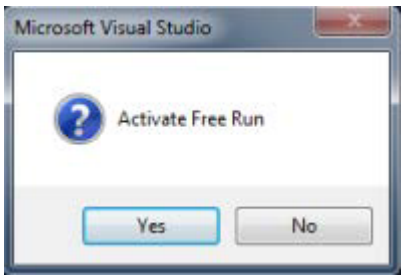
7. When an EtherCAT compatible device has been detected on this Ethernet port, the dialog shown in Figure 12 appears. There is a tick mark next to the adapter to which the K2G ICE board is connected. Press OK and confirm to start Scan for boxes.

Figure 12. I/O Devices Found



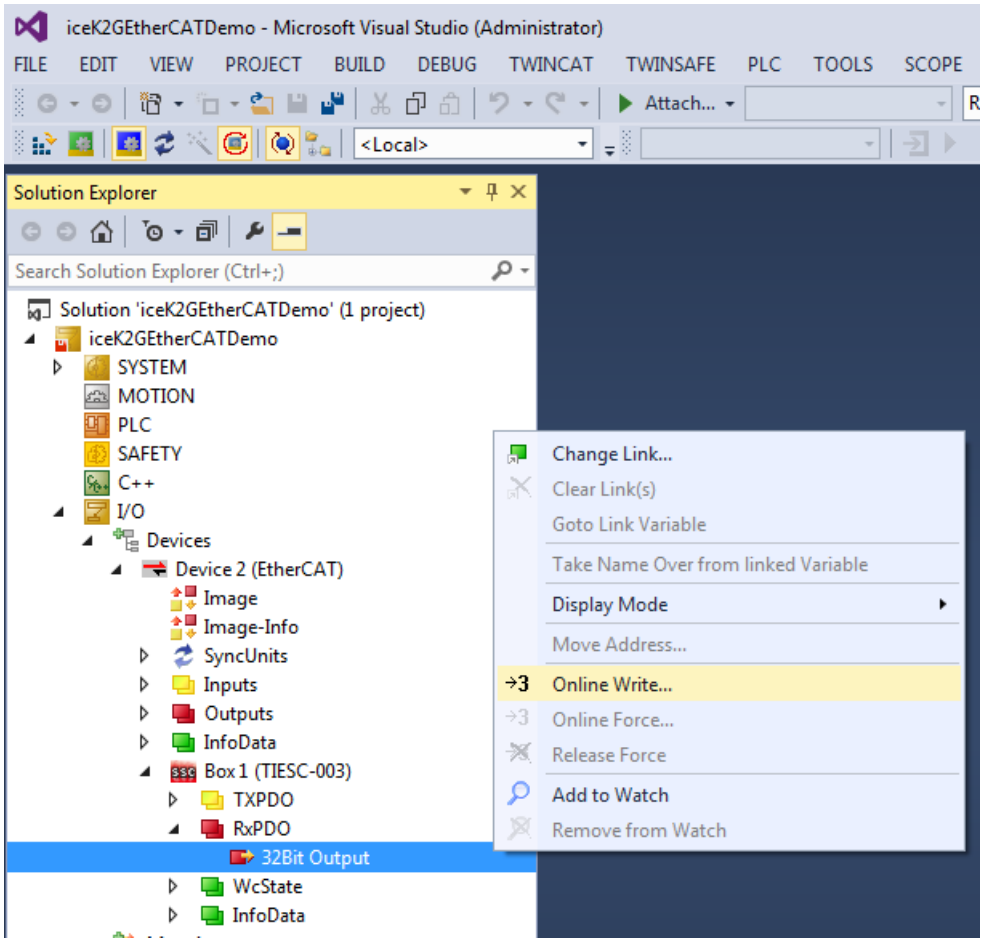
8. The TI device is listed Box n (TIESC-003). Press Yes to activate Free Run, as shown in Figure 13.

Figure 13. Activate Free Run



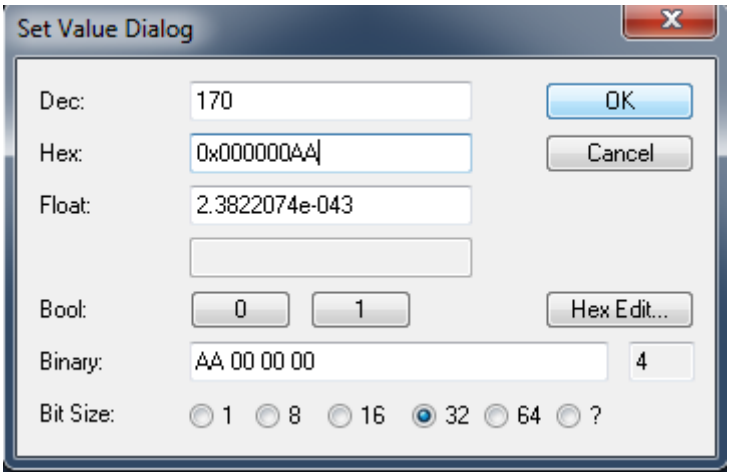
9. Expand the box to see Process Data Inputs (PDI) and Outputs (PDO). Right-click *Box n* > *RxPDO* > *32Bit Output* and select Online Write, as shown in Figure 14.

Figure 14. Online Write



10. Enter the value in hexadecimal format, where each bit in the LSB represents an output, as shown in Figure 15.

Figure 15. Set Value Dialog



11. Changing the LED value sets and clears the appropriate industrial LEDs on the K2G ICE board.

1.5 System Overview

The top and the bottom pictorial views of the K2G ICE are shown in Figure 16 and Figure 17. The side view identifies the position of the Ethernet connectors.

Figure 16. Top View

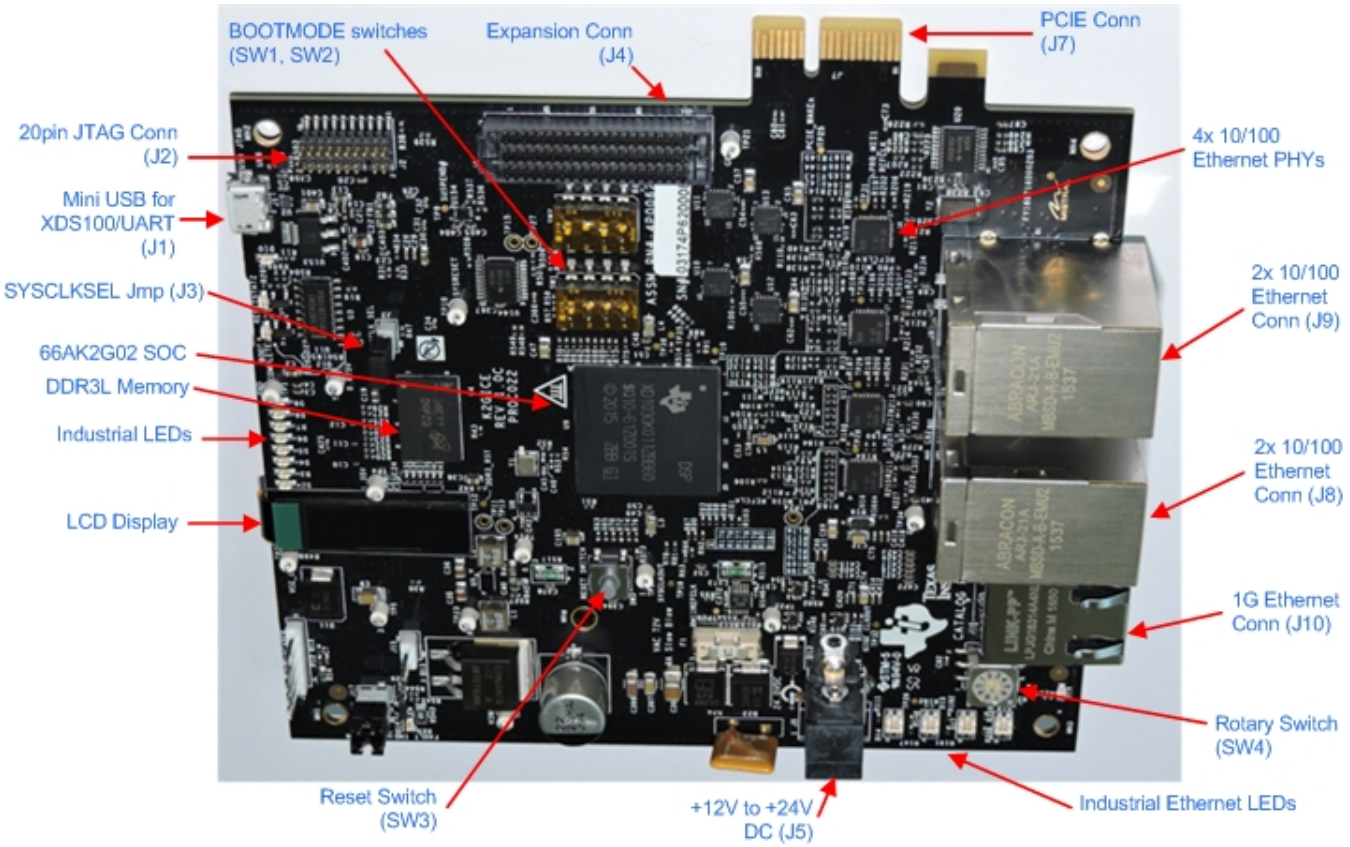


Figure 17. Bottom View

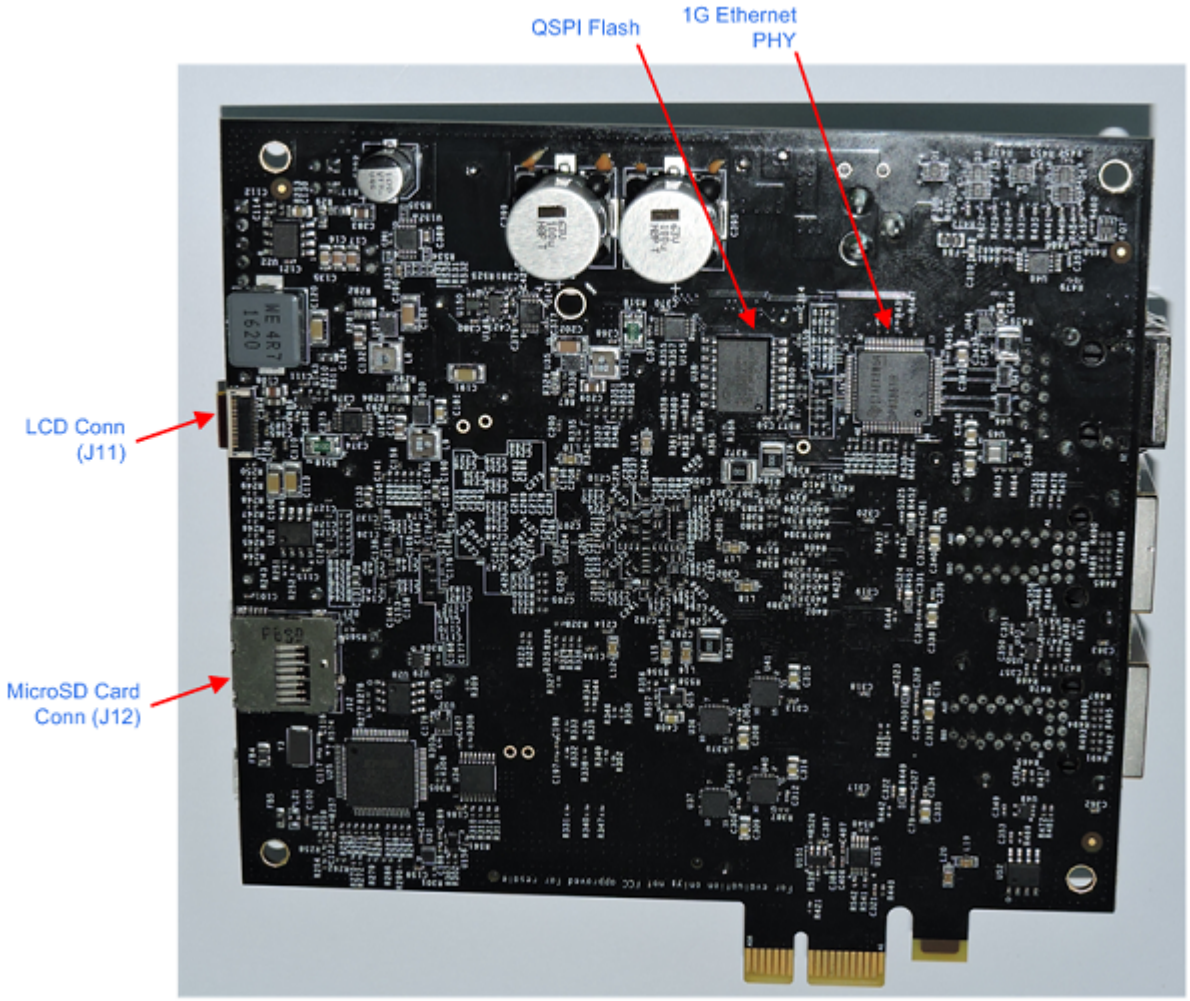
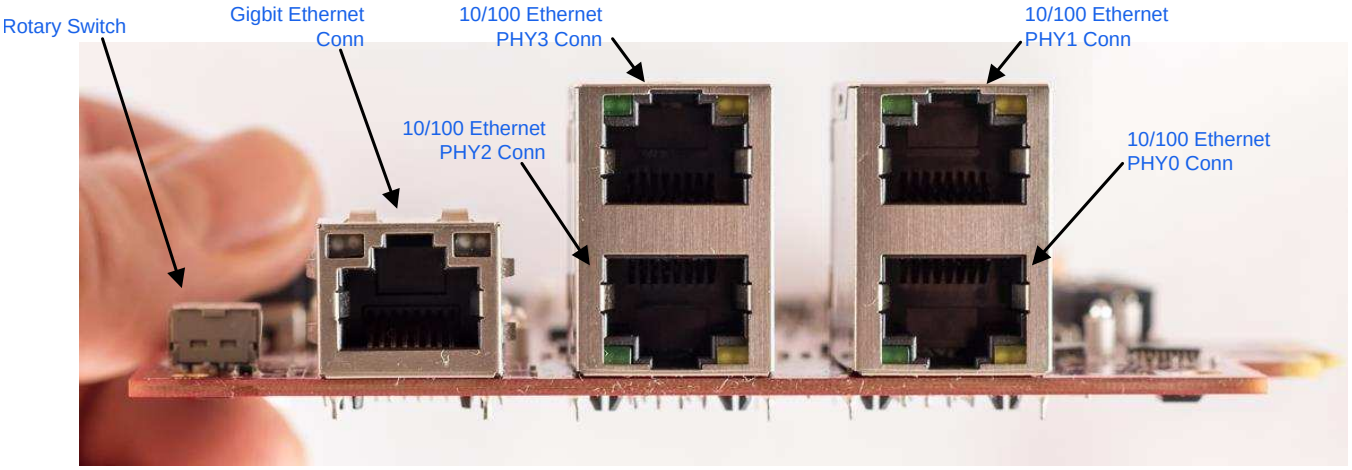


Figure 18. Side View



1.6 Power Supply

The K2G ICE can be powered from one of two sources: a single external power supply connected to the DC power jack (J6), or the 12-V supply pins on the PCIE edge connector. The power supply circuit is designed to allow the use of either a +24-V / 2.5-A DC (60-W) external power supply or a +12-V / 5-A DC (60-W) external power supply. A power ANDing circuit is included in the design, which prevents damage if a +24-V external supply is connected while the board is installed in a PCIE backplane. The +24-V supply is used to power the board in that condition.

Due to regulatory requirements, Texas Instruments cannot provide an external power supply. The K2G ICE has been tested with the CUI SDI65-24-U-P5 +24-V and the CUI SDI65-12-U-P5 +12-V power supplies, which can be purchased from distributors. Links to the supplies are shown below. A power cable can be used with a laboratory supply.

CUI SDI65-12-U-P5

http://www.digikey.com/product-detail/en/cui-inc/SDI65-12-U-P5/102-3417-ND/5277850

CUI SDI65-24-U-P5

http://www.digikey.com/product-detail/en/cui-inc/SDI65-24-U-P5/102-3418-ND/5277851

The input voltage is converted into required voltage levels using individual DC-DC converters. These are shown in Table 1.

Table 1. Voltage Rail Power Supplies

Regulator	Purpose
TPS54531	5V Generation
TLV62084	3V3 Generation
TLV62084	1V8 Generation
TLV62080	1V35 Generation
LP2996A	DDR3 VTT Generation
TPS62180	0V9 Generation
TPS22945	LCD Backlight

1.7 Instructions for Mechanical Assembly

The K2G ICE can be used with or without the mechanical standoffs provided with the board. Standoff mounting is described in the K2G ICE Mechanical Accessories Mounting Instructions.

2 Overview of the K2G ICE

This chapter provides an overview of the different interfaces and circuits on the K2G ICE.

2.1 Voltage Protection Circuit

The voltage protection circuit on the K2G ICE protects the board from overvoltage, undervoltage, transient voltage, and reverse voltage input cases. The safe operation input voltage range is 11 V to 13 V. Any voltage not in this range is considered as fault, and the voltage protection circuit isolates the board from this input. A wide input voltage range is accepted to accommodate both the 24-V input and the 12-V PCIE supply voltage. LED D25 indicates if the DC input applied to board is in a safe input range.

Figure 19. Overvoltage Protection Circuit

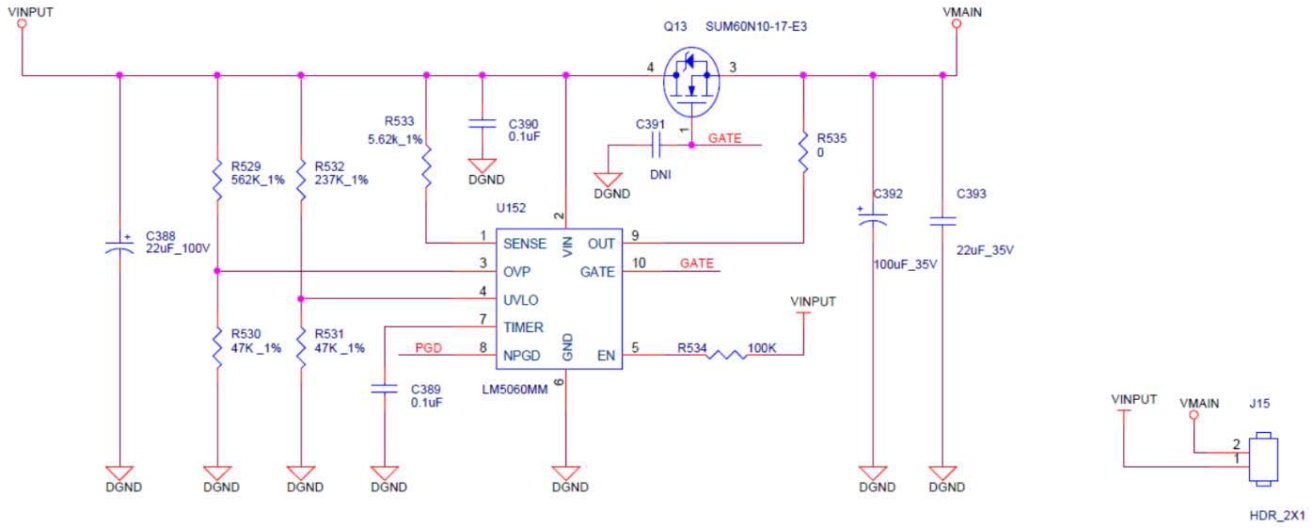
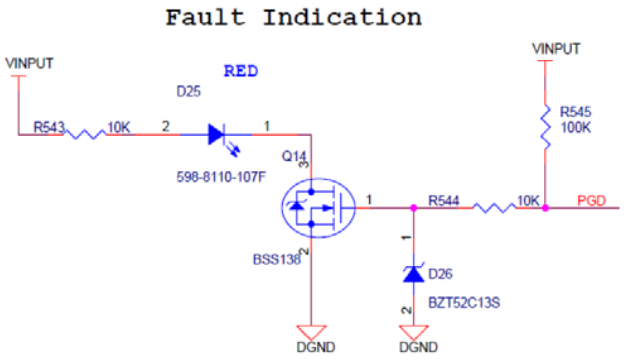


Figure 20. Overvoltage Fault Indicator

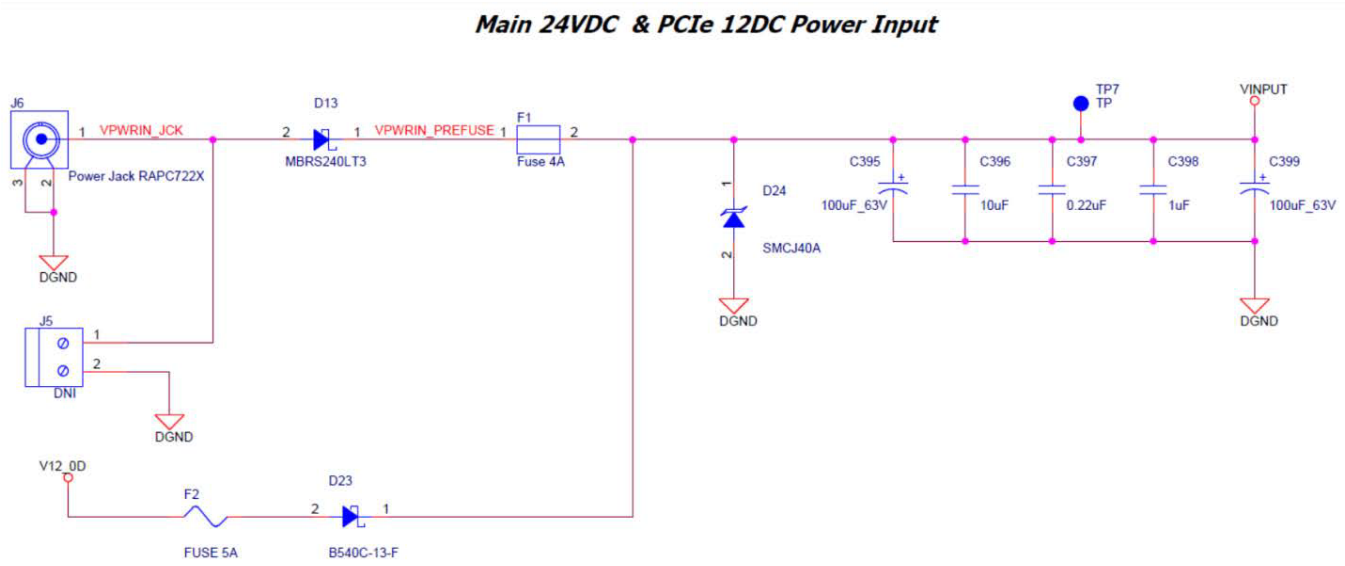


Condition	LED Status (D25)
VINPUT between 11 to 26V	OFF
VINPUT above 26V or below 11V	ON

2.2 Voltage ANDing Circuit

Although it is not recommended, both the 12 V from the PCIE connector and 24 V from the power input may be present at the same time. To protect the board from power supply conflicts, the voltage ANDing circuit was included. If only the 12 V from the PCIE edge connector is present, D23 is forward biased, allowing current to flow. If 24 V is provided to J6, D13 is forward biased. If both 24 V on J6 and 12 V on the PCIE edge connector are both present. D13 is forward biased and D23 is reversed biased, allowing the 24 V to take precedence, and blocking any current flow back to the PCIE connector.

Figure 21. Voltage ANDing Circuit



2.3 Clocking

The K2G ICE EVM derives all internal clocks, with the exception of the PCIE_CLK, from a single clock input. That clock input can be either the internal oscillator using crystal Y1, or an external clock generator connected to SYS_CLK_P/N. The PCIE clock is only present if the K2G EVM is inserted into a PCIE backplane. Software should not attempt to access the PCIE subsystem unless the PCIECLK is present.

The source for the system clock can be sourced from the 24-MHz crystal connected to the SYSOSC pins, or from the 25 MHz provided by the CDCE937PW clock generator. J3 determine which clock is used as the source for the system clock. If a jumper is installed on J3, then SYSCLKSEL is low and the 24-Mhz crystal is used. If the jumper is not installed, then SYSCLKSEL is high and the 25-Mhz SYSCLKP/N input is used. PLL settings for all PLLs must be modified based on the system clock selected.

The DDR clock input to the DDR PLL is derived from the system clock selected, thus no clock is connected to the DDRCLK pins. The AUDOSC, USBOX0, USBOX1, and CPTS_REFCLK clock inputs are not used in this design.

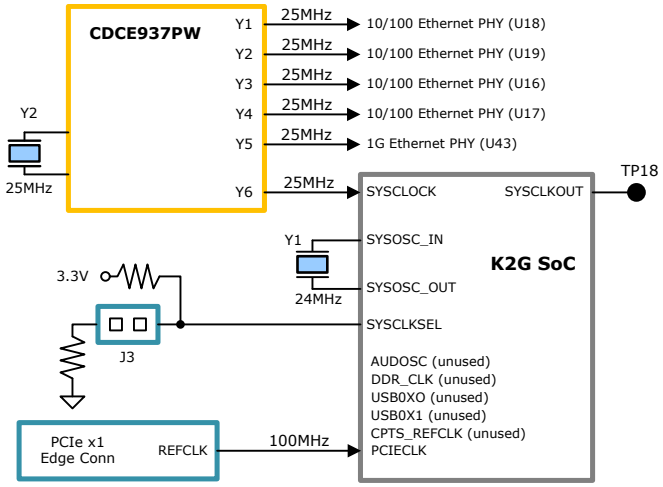
Crystals:

- Y1 – 24-MHz system clock
- Y2 – 25 MHz to CDCE937PW clock generator

Clock generator outputs:

- Y1 – 25-MHz PR0 MII0 PDP83822 10/100 Ethernet PHY
- Y2 – 25-MHz PR0 MII1 PDP83822 10/100 Ethernet PHY
- Y3 – 25-MHz PR1 MII0 PDP83822 10/100 Ethernet PHY
- Y4 – 25-MHz PR1 MII1 PDP83822 10/100 Ethernet PHY
- Y5 – 25-MHz RMII DP83867 Gbit Ethernet PHY
- Y6 – 25-MHz K2G SYS_CLK_P/N clock input

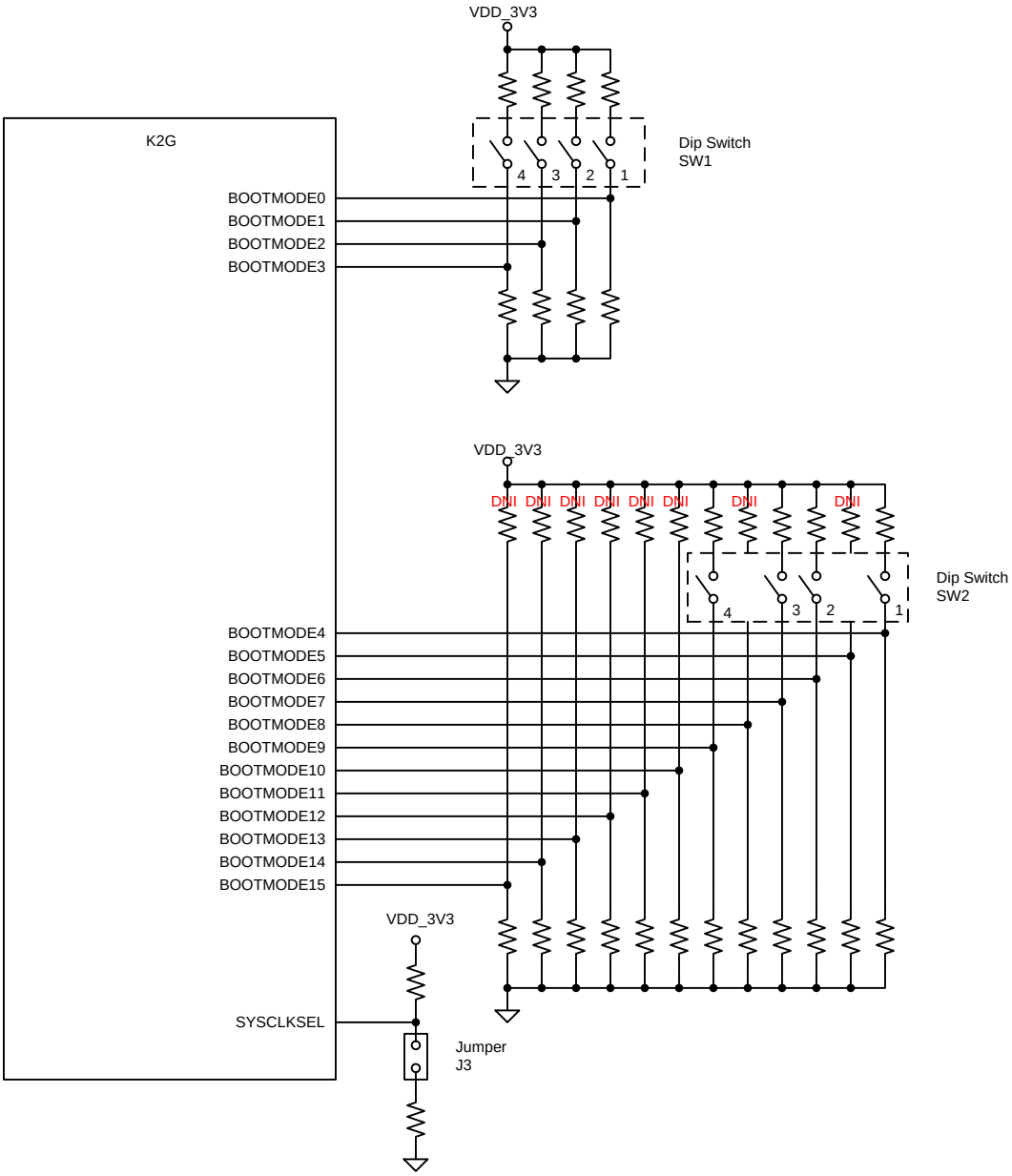
Figure 22. Clock Inputs



2.4 Bootmode Switches

The K2G ICE includes two dip switches, each with four individual switches. These are connected to eight of the sixteen bootmode signals. The K2G ICE is not designed to support all bootmodes available to the K2G, although all bootmodes may be selected with the available switches. Only the bootmodes defined in Table 2 have been tested with the K2G ICE. In addition to the bootmode bits, switches are provided for four additional bootmode pins used to defined specific conditions for each of the bootmodes available. For more information, see the BOOTMODE Pins Description section in the K2G TRM.

Figure 23. Bootmode Selection Switches Schematic



The dip switches are located just above the expansion connector, as shown in Figure 24. Bootmode switches should be set before any expansion board is installed.

Figure 24. Bootmode Selection Switches

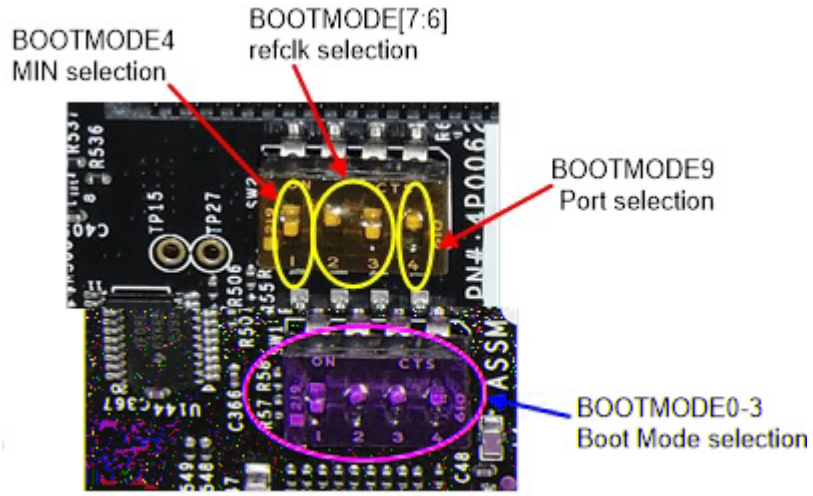


Table 2. Supported Bootmodes

Bootmode	Clock	SW2				SW1				J3	BOOTMODE value
		4	3	2	1	4	3	2	1		
No Boot/Emulation	24MHz	off	off	on	off	off	off	off	off	short	0000000001000000
No Boot/Emulation	25MHz	off	on	off	off	off	off	off	off	open	0000000010000000
PCIE endpoint	24MHz	off	off	on	off	off	off	off	on	short	0000000001000001
PCIE endpoint	25MHz	off	on	off	off	off	off	off	on	open	0000000010000001
QSPI as 48MHz	24MHz	off	off	on	off	on	off	off	off	short	0000000001001000
QSPI as 48MHz	25MHz	off	on	off	off	on	off	off	off	open	0000000010001000
QSPI as 96MHz	24MHz	off	off	on	off	on	off	off	on	short	0000000001001001
QSPI as 96MHz	25MHz	off	on	off	off	on	off	off	on	open	0000000010001001
SDcard	24MHz	on	off	on	off	on	on	on	off	short	0000001001001110
SDcard	25MHz	on	on	off	off	on	on	on	off	open	0000001010001110
UART	24MHz	off	off	on	off	on	on	on	on	short	0000000001001111
UART	25MHz	off	on	off	off	on	on	on	on	open	0000000010001111

2.5 UART and JTAG Emulation Circuit

The K2G ICE provides support for two emulation solutions. An XDS100 circuit is included in the design of the board, which provides emulation capability without the use of external emulation pod. The XDS100 circuit connects directly to a computer using USB.

In addition, a compact TI 20-pin connector is included in the design. An external emulator pod may be connected to the 20-pin connector as an alternative method of JTAG connectivity. Connecting an external pod automatically disables the on-board XDS100 circuit.

More information on JTAG connections may be found on the JTAG Connectors page on TI.com.

2.5.1 2.5.1 XDS100 Circuit

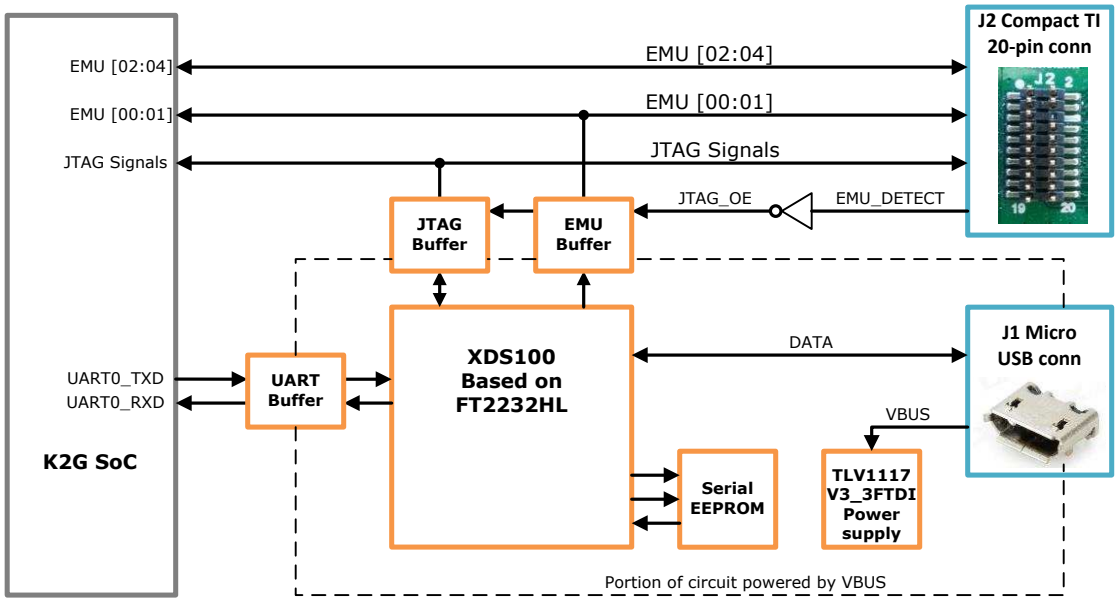
The XDS100 emulation circuit is based on the FTDI dual high-speed USB to multipurpose IO device. The serial EEPROM contains the XDS100 configuration, which supports the JTAG emulation on one port and a UART connection on the second port. Connecting a USB cable between the computer and J1 allows a JTAG connection to Code Composer Studio and a UART connection using VCP. More information on the XDS100 can be found here.

The XDS100 section of the circuit is powered by the VBUS voltage provided by USB. Connection to both the JTAG and the UART is maintained even if the source voltage for the K2G ICE has been removed.

2.5.2 UART

The second port of the FT2232HL is used for a UART-to-USB interface. When the K2G ICE is connected to a computer using the provided USB cable, the computer can establish a Virtual Com Port which can be used with a terminal emulation program. The FT2232HL is powered from the VBUS voltage present on the USB connector. The UART remains connected even if the power is removed from the K2G ICE. The FT2232HL is connected to the K2G UART0 port through a voltage converter buffer.

Figure 25. JTAG Circuit

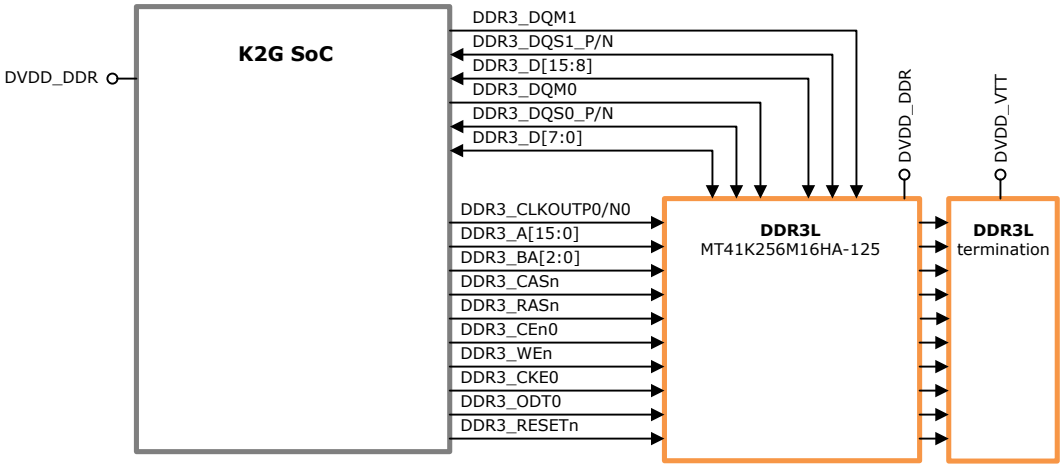


2.6 DDR3 Memory

K2G SoC supports x36 bit (32-bit data + 4-bit ECC) DDR3L; however, the K2G ICE uses 16-bit data. A single 4Gbit (256Mx16) DDR3L chip MT41K256M16HA from Micron is used to obtain a memory size of 512MByte.

The DDR3L chip is routed as a point-to-point connection with VTT termination for the data lines, as shown in Figure 26.

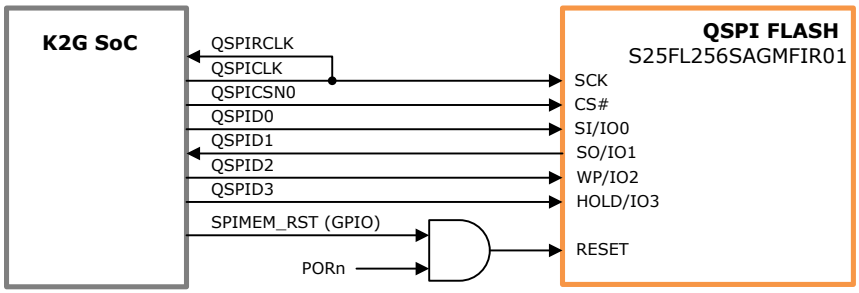
Figure 26. DDR3 Memory Circuit



2.7 QSPI Flash

The K2G QSPI interface is connected to a Spansion S25FL256SAGMFIR01 flash memory component. QSPI CS0 is used to access this device. The QSPI flash reset signal is connected to the output of an AND gate. The AND gate inputs are connected to the PORn signal and a GPIO from the K2G. The GPIO is pulled high, allowing the QSPI flash to exit reset when the PORn signal goes high. This allows the QSPI flash to be used as a boot device. The GPIO connected to the second AND input allows the K2G to reset the QSPI flash if a forced reset is needed during operation.

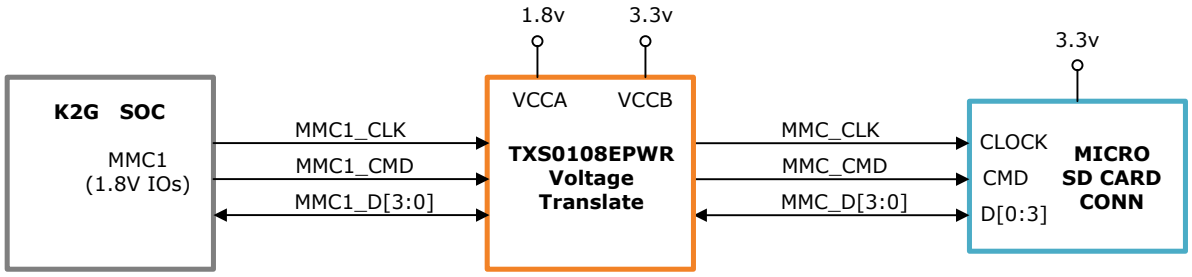
Figure 27. QSPI Flash Memory Interface



2.8 SD Memory Card

The K2G ICE includes a microSD card slot connected to the MMC1 interface of the K2G. MMC1 uses 1.8-V I/Os, while the microSD card operates at 3.3 V. A voltage translator is included to transition the signals between the two voltage domains. While the K2G includes the MMC0 interface, which uses 3.3-V I/Os, it is shared with the outputs of the industrial PRU, which is used in this design.

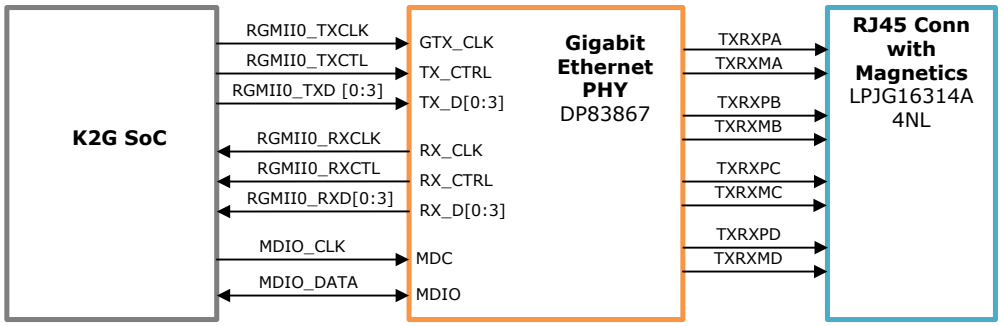
Figure 28. microSD Memory Card Interface



2.9 Gigabit Ethernet

The K2G ICE includes an RGMII connection between the DP83867 Gigabit Ethernet PHY and the network subsystem (NSS) of the SoC using RGMII0. The default configuration of the DP83867 is determined using a number of resistor value pull-ups and pull-downs on specific pins of the PHY.

Figure 29. Gigabit Ethernet Interface



2.9.1 Gigabit Ethernet PHY Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. A configuration pin or groups of configuration pins are used to set the configuration of the PHY after it is released from reset. Configuration settings differ depending on the package type selected for the PHY. The K2G ICE uses the 64-pin QFP package, designated with the PAP suffix, which supports both the GMII and RGMII interface. A 48-pin QFN package, designated with the RGZ suffix and which only supports RGMII, is also available.

2.9.2 Gigabit Ethernet Resistor Strapping

The DP83867 PHY use a four-level configuration based on resistor strappings, which generate four distinct voltage ranges. These resistors are connected to the RX data and control pins, which are normally driven by the PHY and are inputs to the K2G. When 3.3-v I/O voltages are selected, the voltage ranges are shown below.

Mode 1 – 0 V to 0.3234 V

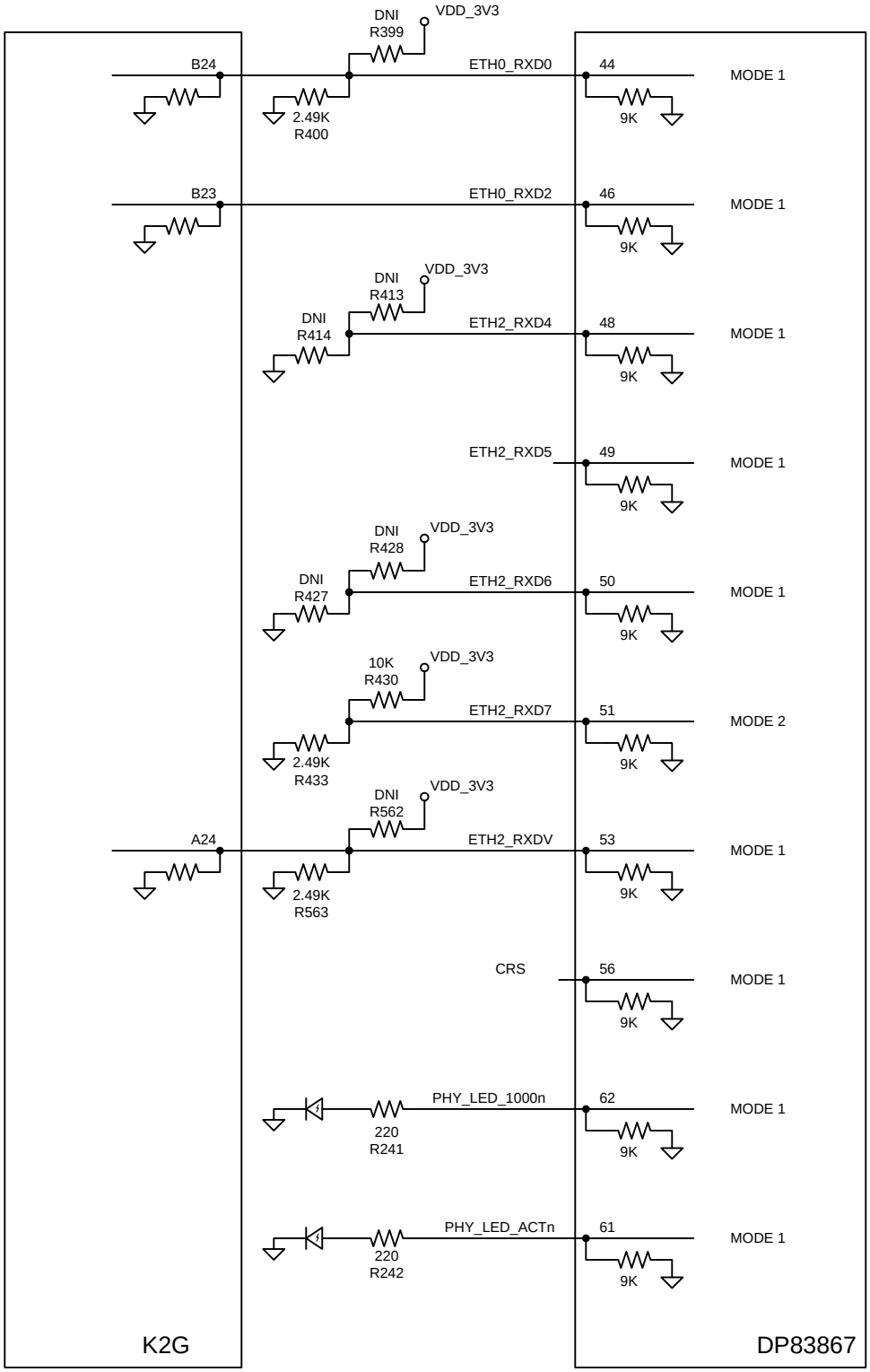
Mode 2 – 0.4884 V to 0.5973 V

Mode 3 – 0.7491 V to 0.9141 V

Mode 4 – 2.2902 V to 3.3 V

Mid-level voltages can result in high leakage currents and are detrimental to the long-term reliability of the K2G I/O cells connected to the strapping resistor. To avoid this situation, only pull-up and pull-down resistors are used to pull the I/O cells as close as possible to either 0 V or 3.3 V. This limits the selection of configurations to those that can be selected by using Mode 1 or Mode 4. Both the DP83867 and the K2G include internal pulling resistors. The value of the external pull resistors are selected to provide a voltage at the pins of the K2G as close to ground or 3.3 V as possible.

Figure 30. Gigabit Ethernet Pulling Resistors



Consult the data manual of the DP83867 for more details on configuring the PHY. The DP83867 strapping can be read from the STRAP_STS1 and STRAP_STS2 registers. The strapping resistors on the K2G ICE configures the DP83867, as show in Table 3.

Table 3. Gigabit PHY Configuration

Bit	BIT NAME	Value	Description
STRAP_STS1.15	STRAP_MIRROR_EN	0	Port mirroring disabled
STRAP_STS1.14	STRAP_LINK_DOWNSHIFT_EN	0	Link downshift disabled
STRAP_STS1.13	STRAP_CLK_OUT_DIS	1	Clock output disabled
STRAP_STS1.12	STRAP_RGMII_DIS	0	RGMII enabled
STRAP_STS1.10	STRAP_AMDIX_DIS	0	Auto-MDIX enabled
STRAP_STS1.9	STRAP_FORCE_MDI_X	0	Force MDI (not used because auto-MDIX is enabled)
STRAP_STS1.8	STRAP_HD_EN	0	Full duplex enabled (not used because auto-MDIX is enabled)
STRAP_STS1.7	STRAP_ANEG_DIS	0	Auto-negotiation enabled
STRAP_STS1.6:5	STRAP_SPEED_SEL	00	Advertise 10/100/1000
STRAP_STS1.4:0	STRAP_PHY_ADD	00000	PHY address = 0x00
STRAP_STS2.10	STRAP_FLD	0	Fast link detect disabled

2.9.3 Gigabit Ethernet Configuration

The DP83867 PHY must be configured using the MDIO register accesses for proper operation of the interface on the K2G ICE.

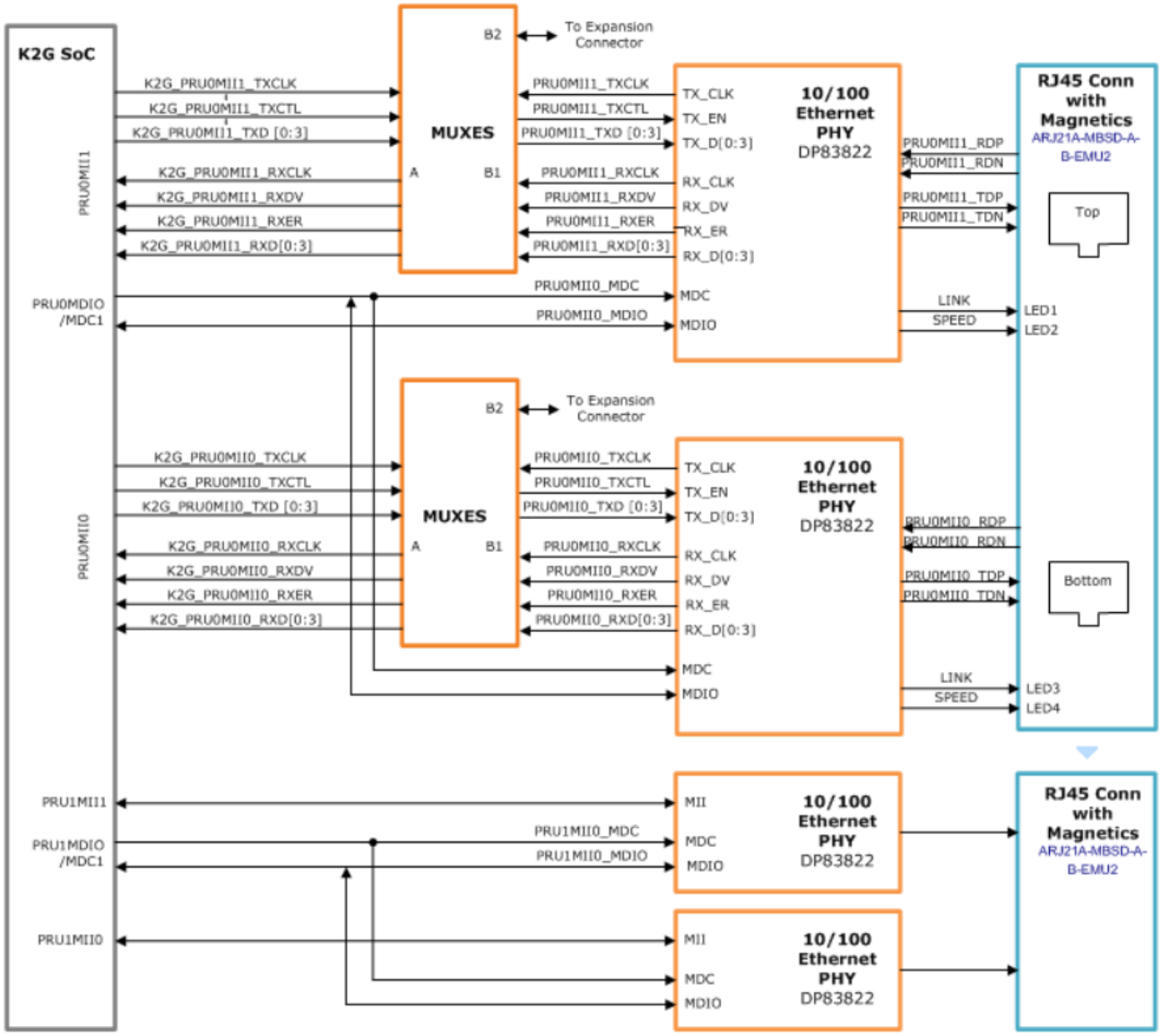
First, the value of 0x170 must be written to register 0x31 of the DP83867 for proper operation of the auto-negotiation function.

Secondly, the DP83867 includes the ability to delay the RGMII TX clock and RX clock relative to the data signals, to compensate for delays introduced in the routing of the RGMII interface. An application note explaining this capability is included on the product page for the DP83867. After analyzing the layout of the RGMII on the K2G ICE, there is a delay of 2.25 nsec for the RX clock and 2.25 nsec for the TX clock. The TX clock delay consists of the 2 nsec of internal delay and 0.25 nsec of PCB delay. The TX clock delay is calculated assuming that the RGMII internal TX clock delay is enabled within the K2G. In the RGMIIDCTL register (0x86), the RGMII_TX_DELAY_CTRL bit field should be set to 0b0000 and the RGMII_RX_DELAY_CTRL field should be set to 0b1000. In the RGMIICTL register (0x32), the RGMII_TX_CLK_DELAY bit should be set to 1 and the RGMII_RX_CLK_DELAY bit should be set to 1 to enable the clock shift specified in the RGMIIDCTL register.

2.10 Industrial Ethernet

The K2G SoC includes two programmable real-time unit subsystems and industrial communications subsystems (PRU-ICSS), which can be configured to support numerous industrial protocols. Each PRU-ICSS unit can support two MII interfaces for connection to two 10/100 Ethernet PHYs. The K2G ICE includes four DP83822I 10/100 Industrial Ethernet PHYs providing four Ethernet connections. The signals for PRU0 are connected to muxes, allowing this interface to be connected to the expansion connector.

Figure 31. Industrial Ethernet Interface



2.10.1 Industrial Ethernet PHY Default Configuration

The default configuration of the DP83822 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes. A configuration pin or groups of configuration pins are used to set the configuration of the PHY after it is released from reset. Configuration settings differ depending on the package type selected for the PHY.

2.10.2 Industrial Ethernet Resistor Strapping

The DP83822 PHY use a four-level configuration based on resistor strappings, which generate four distinct voltages ranges. These resistors are connected to the RX data and control pins, which are normally driven by the PHY and are inputs to the K2G. These voltage ranges are shown below.

Mode 1 – 0 V to 0.3234 V

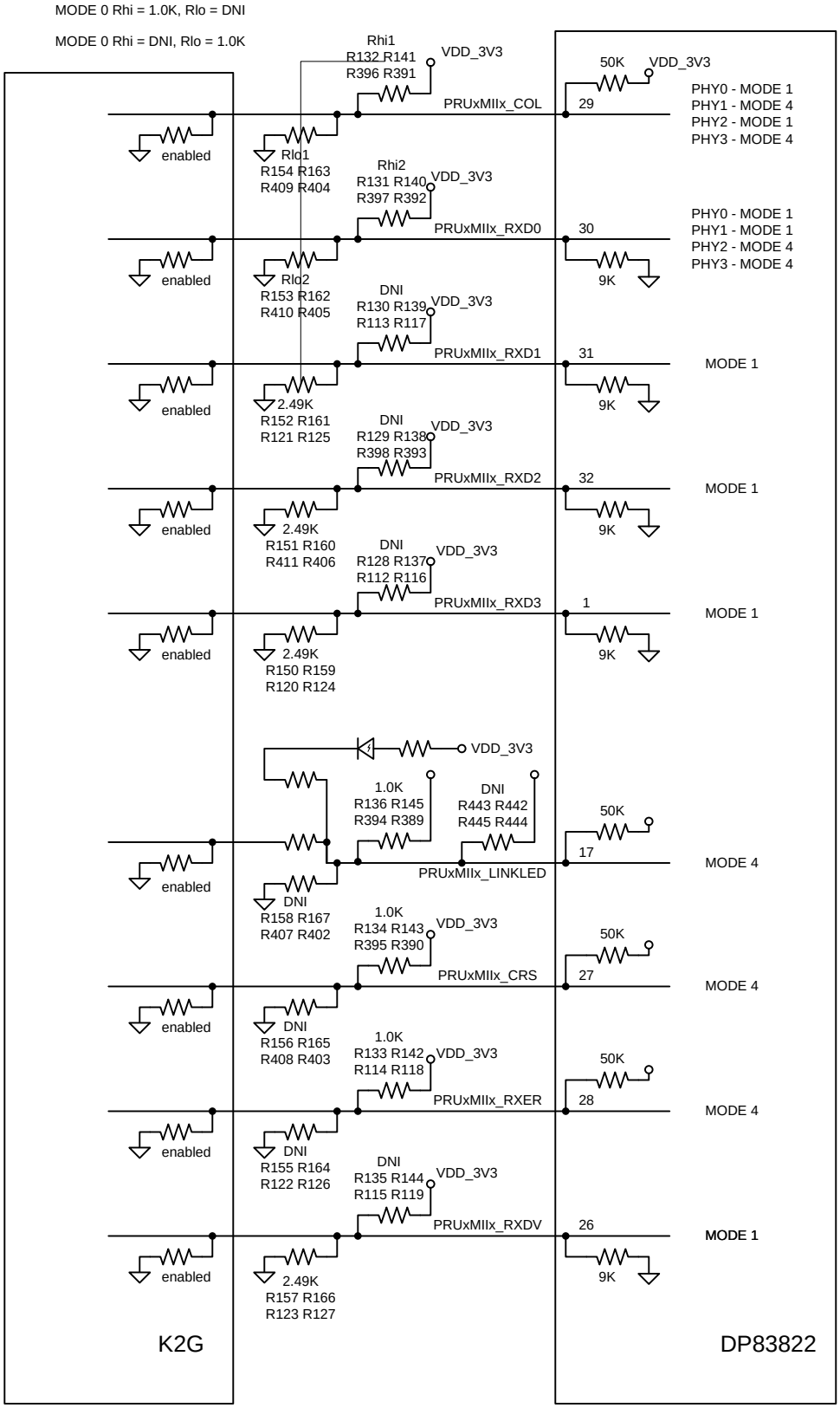
Mode 2 – 0.4884 V to 0.5973 V

Mode 3 – 0.7491 V to 0.9141 V

Mode 4 – 2.2902 V to 3.3 V

Mid-level voltages can result in high leakage currents and are detrimental to the long-term reliability of the K2G I/O cells connected to the strapping resistor. To avoid this situation, only pull-up and pull-down resistors are used to pull the I/O cells as close as possible to either 0 V or 3.3 V. This limits the selection of configurations to those that can be selected by using Mode 1 or Mode 4. Both the DP83822 and the K2G include internal pulling resistors. The value of the external pull resistors is selected to provide a voltage at the pins of the K2G as close to ground or 3.3 V as possible.

Figure 32. Industrial Ethernet Pulling Resistors

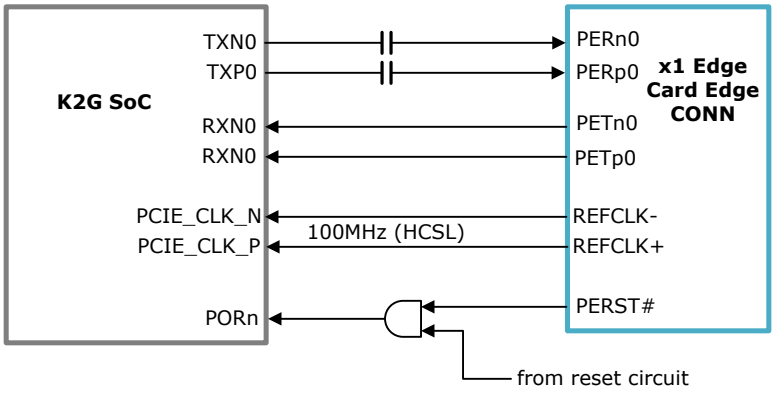


2.11 PCIE Edge Connector

The K2G ICE includes a PCIE x1 edge connector as defined by the PCI Express Electromechanical Specification, Rev 2.0. While the edge connector and the board thickness are compatible with that standard, the K2G ICE was not designed to meet all the requirements for the Electromechanical specification, and is not designed to fit into a standard PC chassis. No I/O bracket is available, and the EVM is not compliant with the PCB form factor or component height restrictions.

Although the K2G can be configured as a PCIE root-complex or endpoint, the K2G ICE only supports PCIE endpoint operations. The PCIE reference clock is only provided by the PCIE connector. No accesses to the PCIE portion of the K2G SOC should be performed unless a PCIE reference clock is present on the PCIE edge connector.

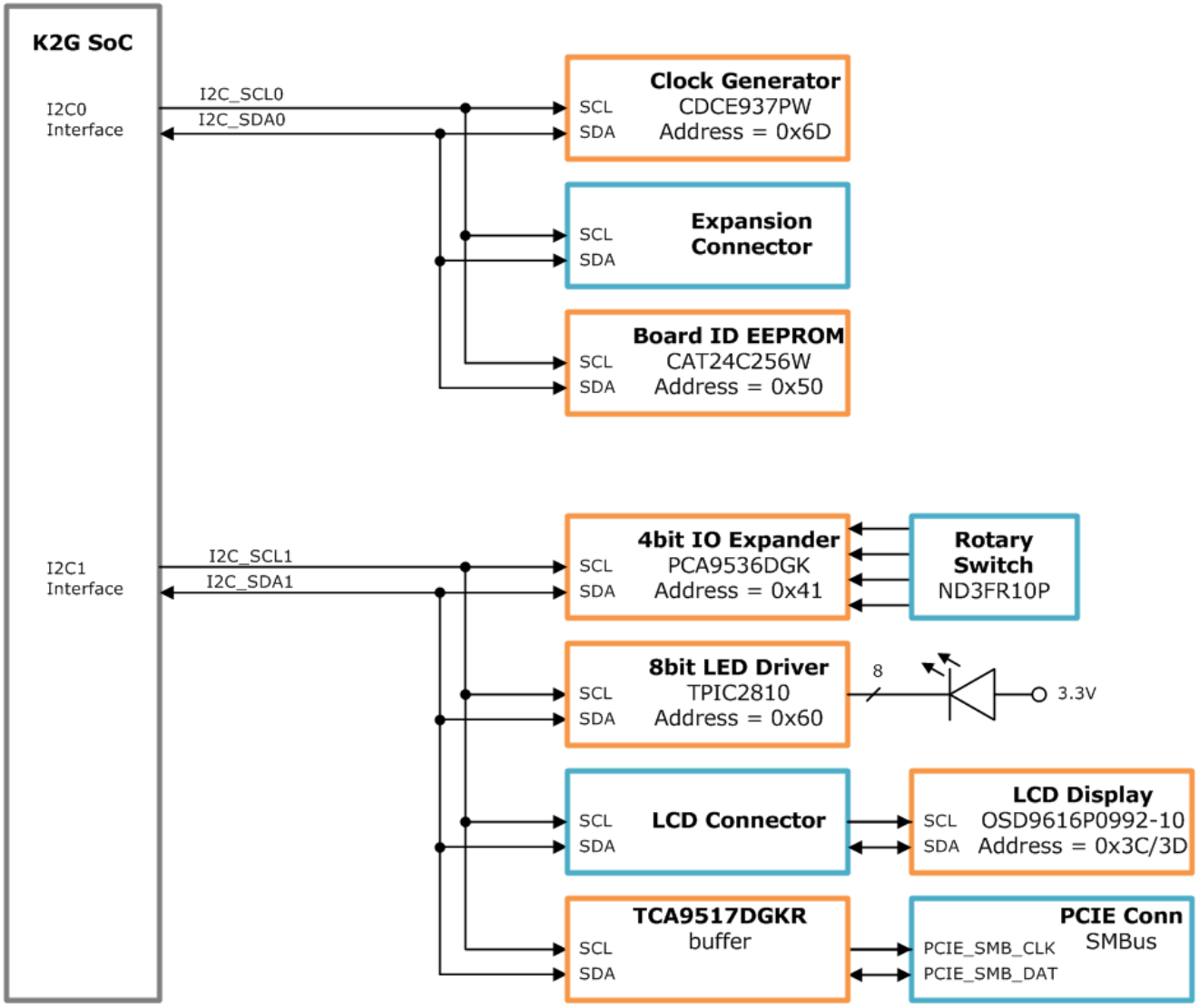
Figure 33. PCI Express Edge Connector



2.12 I2C

The K2G ICE uses two of the three available I2C interfaces: I2C0 and I2C1. I2C0 is connected to the clock generator and the expansion connector. I2C1 is used for the additional peripheral devices needed by the K2G ICE. The devices connected to these interfaces and their function are presented in the following sections.

Figure 34. I2C Connections



2.12.1 CDCE937PW 25-MHz Clock Generator

The CDCE937PW clock generator is preprogrammed to generate the 25-MHz clock outputs needed by the Ethernet PHYs, and for the external clock input to the K2G SoC. No additional programming is required.

2.12.2 I2C on Expansion Connector

Additional I2C devices may be mounted on a daughtercard connected to the expansion connector. All addresses, with the exception of 0x6D, are available for devices on the expansion connector connected to I2C0.

2.12.3 CAT24C256W Board ID Memory

The K2G ICE board includes a CAT24C256W I2C EEPROM ID memory. The initial 72 bytes of the ID memory is preprogrammed with identification information for each board. The remaining 32696 is available to the user for data or code storage. **The initial 72 bytes of the ID memory should never be overwritten**.

Table 4. ID Memory Header Information

Name	Size (bytes)	Contents	Description
Header	4	MSB 0xEE3355AA LSB	Start code
Board name	8	66AK2GIC	Board name in ASCII
Version	4	1.0B	Hardware revision code in ASCII
Serial number	12	WWYY4P62nnnn	WW – Week of production YY – Year of production 4P62 – K2G ICE board code nnnn – Serial number
Configuration option	32		Reserved for board configuration codes
Ethernet MAC address #0	6	MSB to LSB - MAC-ID 70-FF-76-1C-xx-xx	This is the first of a block of six addresses available for the industrial interface ports
Ethernet MAC address #5	6	MSB to LSB - MAC-ID 70-FF-76-1C-xx-xx	This is the last of a block of six addresses available for the industrial interface ports
Available	32696		Available space for user data or code

2.12.4 PCA9536DGK/ ND3FR10P Rotary Switch

The K2G ICE board includes a PCA9536DGK I2C 4-bit IO Expander connected to a ND3FR10P 10-position rotary switch. Selecting a value on the switch presents a four-bit binary code to the PCA9536. This value can be read using the I2C interface.

2.12.5 OSD9616P0992-10 LCD Display

The K2G ICE board includes a OSD9616P0992-10 96×16 pixel LCD display. The display is based on the SSD1606 controller. Communications with the controller uses two slave addresses, 0x3C and 0x3D, for I2C1.

2.12.6 TPIC2810 LED Driver

The K2G ICE board includes a TPIC2810 8-bit LED driver. The driver is used to control eight green LEDs used to define the state of the industrial interfaces.

2.12.7 TCA9517DGKR I2C Buffer

The K2G ICE board includes a TCA9517DGKR buffer between I2C1 and the SMBus interface on the PCIE edge connector. This buffer acts as voltage isolation between the K2G ICE card and the circuit connected to the PCIE bus. The SMBus (System Management Bus) is used by PCIE as a control interface with the PCIE root complex. This interface is provided for future use and is not currently supported by software.

2.13 GPIOs

Almost every I/O pin on the K2G can be configured as a GPIO. A number of GPIO pins are used in the K2G ICE for various control functions. Those GPIOs and their function are listed in Table 5.

Table 5. GPIO Functions

SOC GPIO Name	Ball	Net Name	Dir	Function
GPIO0_00	AC21	GPIO0_00	I/O	Expansion Connector
GPIO0_01	AE20	GPIO0_01	I/O	Expansion Connector
GPIO0_02	AD22	GPIO0_02	I/O	Expansion Connector
GPIO0_03	AD20	GPIO0_03	I/O	Expansion Connector
GPIO0_04	AE21	GPIO0_04	I/O	Expansion Connector
GPIO0_05	AE22	GPIO0_05	I/O	Expansion Connector
GPIO0_06	AC20	GPIO0_06	I/O	Expansion Connector

Table 5. GPIO Functions (continued)

SOC GPIO Name	Ball	Net Name	Dir	Function
GPIO0_07	AD21	GPIO0_07	I/O	Expansion Connector
GPIO0_08	AE23	GPIO0_08	I/O	Expansion Connector
GPIO0_09	AB20	GPIO0_09	I/O	Expansion Connector
GPIO0_11	AD23	LED_1	Out	1 – LED D17 Red on 0 – LED D17 Red off
GPIO0_12	AA21	LED_2	Out	1 – LED D17 Green on 0 – LED D17 Green off
GPIO0_13	AB21	LED_3	Out	1 – LED D17 Blue on 0 – LED D17 Blue off
GPIO0_14	AB22	LED_4	Out	1 – LED D18 Red on 0 – LED D18 Red off
GPIO0_15	AA22	LED_5	Out	1 – LED D18 Green on 0 – LED D18 Green off
GPIO0_16	AB23	LED_6	Out	1 – LED D18 Blue on 0 – LED D18 Blue off
GPIO0_19	Y22	LED_7	Out	1 – LED D19 on 0 – LED D19 off
GPIO0_44	R21	LED_8	Out	1 – LED D14 Red on 0 – LED D14 Red off
GPIO0_43	U24	LED_9	Out	1 – LED D14 Green on 0 – LED D14 Green off
GPIO0_42	V25	LED_10	Out	1 – LED D14 Blue on 0 – LED D14 Blue off
GPIO0_41	T24	LED_11	Out	1 – LED D15 Red on 0 – LED D15 Red off
GPIO0_101	P3	LED_12	Out	1 – LED D15 Green on 0 – LED D15 Green off
GPIO0_102	P4	LED_13	Out	1 – LED D15 Blue on 0 – LED D15 Blue off
GPIO0_107	U1	MUX_MII_CTL_PRU0MII0	Out	1 – PRU0 signals to expansion conn 0 – PRU0MII1 to 10/100 PHY0 (U18)
GPIO0_106	T2	MUX_MII_CTL_PRU0MII1	Out	1 – PRU0 signals to expansion conn 0 – PRU0MII1 to 10/100 PHY1 (U19)
GPIO0_66	H22	OE_PRU0MII0_1	Out	0 – Enable Outputs PRUMII0 Muxes (U10, U41)
GPIO0_67	H21	OE_PRU0MII0_2	Out	0 – Enable Outputs PRUMII0 Muxes (U12, U36)
GPIO0_57	R5	OE_PRU0MII1_1	Out	0 – Enable Outputs PRUMII1 Muxes (U11, U13)
GPIO0_56	P5	OE_PRU0MII1_2	Out	0 – Enable Outputs PRUMII1 Muxes (U37, U40)
GPIO0_28	W23	PR0_MII0_INTn	In	0 – Interrupt from 10/100 Ethernet PHY0 (U18)
GPIO0_29	Y25	PR0_MII1_INTn	In	0 – Interrupt from 10/100 Ethernet PHY1 (U19)
GPIO0_17	AC23	PR1_MII0_INTn	In	0 – Interrupt from 10/100 Ethernet PHY2 (U16)
GPIO0_22	Y24	PR1_MII1_INTn	In	0 – Interrupt from 10/100 Ethernet PHY3 (U17)
GPIO0_23	AA24	GPIO_PR0_MII0_RESETn	Out	0 – Reset 10/100 PHY0 (U18)
GPIO0_21	AB24	GPIO_PR0_MII1_RESETn	Out	0 – Reset 10/100 PHY1 (U19)
GPIO0_20	AC24	GPIO_PR1_MII0_RESETn	Out	0 – Reset 10/100 PHY2 (U16)
GPIO0_24	W25	GPIO_PR1_MII1_RESETn	Out	0 – Reset 10/100 PHY3 (U17)
GPIO0_10	AA20	GB_ETH_RESETn	Out	0 – Resets Gigabit Ethernet PHY (U43)
GPIO0_46	U22	SPIMEM_RST	Out	0 – Reset QSPI Memory
GPIO0_52	E21	OLED_RESETn	Out	0 – Reset the LCD Display
GPIO0_53	D21	LCD_BST_CONV_CTL	Out	0 – Disable LCD backlight 1 – Enable LCD backlight
GPIO0_25	AA25	DDR_VTT_SDn	Out	0 – Shutdown VTT power supply 1 – Enable VTT power supply

2.14 LEDs

The K2G ICE includes a number of LEDs used to provide indications of various conditions. Some LEDs are controlled by user software, and some provide the state of circuitry. Table 6 lists details of the LEDs.

Figure 35. Ethernet LED Positions

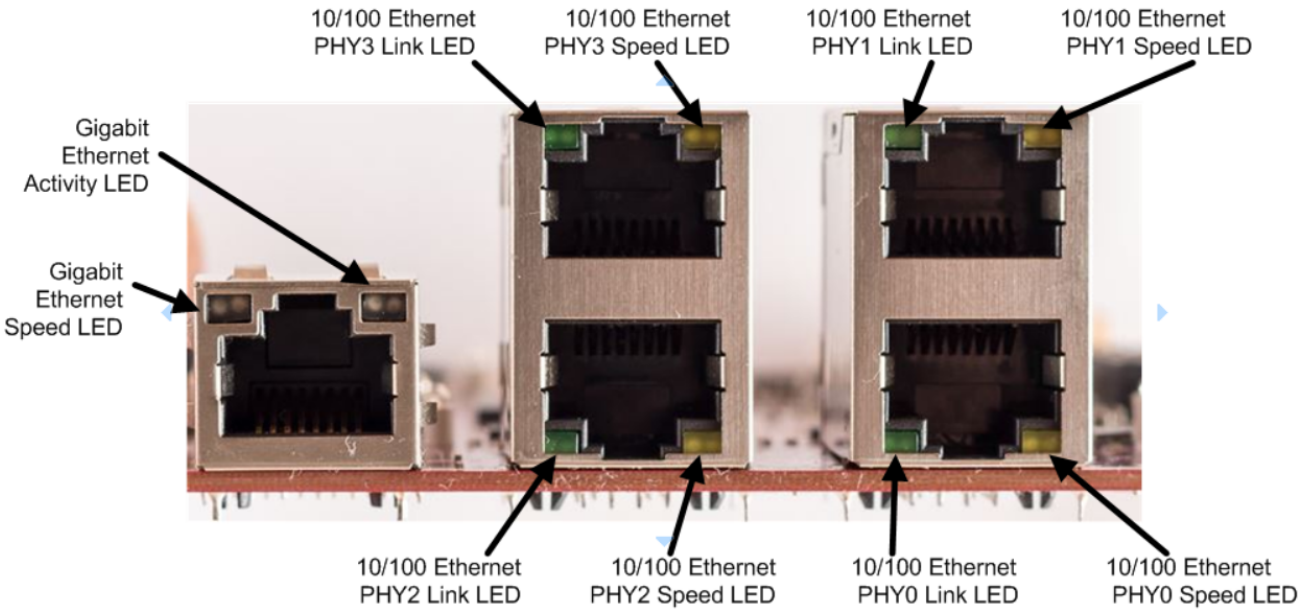


Table 6. LEDs

LED	Color	Control	Software Controlled	Function
D1	Green	+5V	No	Lit when +5 V is present
D2	Green	U3.3	Yes	user LED
D3	Green	U3.4	Yes	user LED
D4	Green	U3.5	Yes	user LED
D5	Green	U3.6	Yes	user LED
D6	Green	U3.11	Yes	user LED
D7	Green	U3.12	Yes	user LED
D8	Green	U3.13	Yes	user LED
D9	Green	U3.14	Yes	user LED
D10	Green	JTAG	No	JTAG connected to USB
D19	Green	GPIO	Yes	Industrial LED
D14	Tri-color	GPIOx3	Yes	Industrial LED
D15	Tri-color	GPIOx3	Yes	Industrial LED
D17	Tri-color	GPIOx3	Yes	Industrial LED
D18	Tri-color	GPIOx3	Yes	Industrial LED
J10 Left	Green	GigPHY	No	Gigabit Ethernet speed
J10 Right	Green	GigPHY	No	Gigabit Ethernet activity
J9 Bottom Left	Green	10/100PHY	No	10/100 Ethernet PHY0 link
J9 Bottom Right	Yellow	10/100PHY	No	10/100 Ethernet PHY0 speed
J9 Top Left	Green	10/100PHY	No	10/100 Ethernet PHY1 link
J9 Top Right	Yellow	10/100PHY	No	10/100 Ethernet PHY1 speed
J8 Bottom Left	Green	10/100PHY	No	10/100 Ethernet PHY2 link

Table 6. LEDs (continued)

LED	Color	Control	Software Controlled	Function
J8 Bottom Right	Yellow	10/100PHY	No	10/100 Ethernet PHY2 speed
J8 Top Left	Green	10/100PHY	No	10/100 Ethernet PHY3 link
J8 Top Right	Yellow	10/100PHY	No	10/100 Ethernet PHY3 speed

2.15 Expansion Connector

The K2G ICE provides a 120-pin expansion connector to allow customers to develop custom daughtercards. The expansion connector includes a number of industrial interfaces, including the signals for PRU0, UART, eCAP, eQEP, SYNC, and LATCH. In addition, SPI0, SPI1, I2C0, and a number of GPIOs are provided for customer-defined functions. The +5 V and +3.3 V are included, but are subject to the limitations of the power supplies found on the ICE EVM. The VMAIN power supply voltage is also provided. This rail is limited to the capabilities of the main power supply for the K2G ICE. A complete list of signals found on the expansion connector can be found in Section 3.3.

3 ICE EVM Board Physical Specifications

This section describes the physical layout of the EVMK2G board and its connectors, switches, and test points.

3.1 Mounting Holes

The kit includes a set of standoffs that may be used for stability. A complete description of the mounting holes use for the standoffs can be found in the K2G ICE Mechanical Accessories Mounting Instructions.

3.2 Board Layout

The K2G ICE PCB layout was developed using Cadence Allegro 16.6. The PCB database is provided with the documentation package for the K2G ICE. A free PCB database viewer is available from Cadence.

3.3 Connector Index

The EVMK2G board has several connectors that provide access to various interfaces on the board, as listed in Table 7 and shown in Figure 2 and Figure 3.

Table 7. Connectors

Conn	Part Number	Pins	Function
J1	ZX62-AB-5PA(31)	5	MIcroAB USB - XDS100 JTAG and UART
J2	FTR-110-03-G-D-06	20	SMT micro header - JTAG
J3	0022032021	2	2X1 2.54-mm header – SYSCLKSEL configuration
J4	SEAF-20-05.0-S-06-A-2-K-TR	120	120 pin – Expansion connector
J5	OSTTC022162	2	Screw terminal (not installed)
J6	RAPC722X	3	Barrel jack – power connector
J7	Edge connector	36	PCIe x1 edge connector
J8	ARJ21A-MBSD-A-B-EMU2	28	Stacked RJ45 – 10/100 Industrial Ethernet
J9	ARJ21A-MBSD-A-B-EMU2	28	Stacked RJ45 – 10/100 Industrial Ethernet
J10	LPJG16314A4NL	14	RJ45 – Gigabit Ethernet
J11	10051922-1410ELF	14	FPC – LCD connector
J12	SCHA5B0200	8	microSD Card Cage
J14	0022032051	5	2X1 2.54-mm header – INA226 interface
J15	0022032021	2	2X1 2.54-mm header – Test Point Header
J16	0022032021	2	2X1 2.54-mm header – I2C_SCL2 Jumper
J17	0022032021	2	2X1 2.54-mm header – I2C_SDA2 Jumper

3.3.1 DC Jack (J6) and Screw Terminal (J5)

The K2G ICE is powered by inserting the DC adapter into this power jack. An input voltage between +12 V and +24 V is supported. Alternatively, a screw terminal can be used to connect individual wires. The screw terminal is not installed on production boards.

3.3.2 MicroAB USB (J1) for XDS100 and UART

The K2G ICE MicroAB USB connector provides two ports for communication. The first port is used to interface with the XDS100 on-board emulation circuit. The second port is used for UART0 console port.

3.3.3 JTAG (J2)

An external JTAG emulation pod may be connected to the compact TI 20-pin JTAG connector. If an external emulation pod is connected to J2, the EMU_DETECT signal, which is pulled high, is shorted to ground. EMU_DETECT disables the onboard XDS100 emulation circuit when grounded. This allows the customer to use a higher performance emulator if available.

Table 8. 20 pin JTAG (J2)

Pin	Signal	Pin	Signal
1	TMS	2	TRSTn
3	TDI	4	TDIS (grounded on K2G ICE)
5	+3.3V	6	Key (no pin)
7	TDO	8	GND
9	TCLKRTN	10	GND
11	TCLK	12	GND
13	EMU0	14	EMU1
15	nRESET	16	GND
17	EMU2	18	EMU3
19	EMU4	20	EMU_DETECT

3.3.4 Expansion Connector (J4)

The K2G ICE is designed to provide four MII connections to 10/100 Ethernet PHYs; however, the ICSS supports other industrial interfaces. A 120-pin expansion connector is provided with connections to other industrial interfaces and to PR0 to allow for customer-designed daughtercards. PR0 signals are connected to a series of muxes controlled by SoC GPIOs. These select between the connection to the expansion connector and two of the 10/100 industrial Ethernet PHYs.

The expansion connector is a Samtec SEAF series high-speed/high-density open-pin field connector designed for board-to-board connections. The part number used is the Samtec SEAF-20-05.0-S-06-A-2-K-TR. This is a 120-pin connector consisting of six rows with 20 pins in each row. The signals available are listed in Table 9. Mating connectors including the SEAM series can be found on the Samtec website.

Table 9. Expansion Connector (J4)

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
5	LED1	6	VMAIN (+12V to +24V)
7	+3.3V	8	+3.3V
11	LED2	12	VMAIN (+12V to +24V)
13	SPI0_CLK	14	PR0_UART0RXD
17	PR0_PRU1_PRU_R30_OUT[0]	18	LED3
19	SPI0_SOMI	20	PR0_UART0TXD
23	PR0_PRU1_PRU_R30_OUT[1]	24	LED4
25	SPI0_SIMO	26	PR0_PRU0_GPO7
29	PR0_PRU1_PRU_R30_OUT[2]	30	GND
31	SPI0_SCS0	32	PR1_UART0RXD
35	PR0_PRU1_PRU_R30_OUT[3]	36	GPIO0_00
37	SPI0_SCS1	38	PR0_PRU1_PRU_R30_OUT[7]
41	PR0_PRU1_PRU_R30_OUT[4]	42	GPIO0_01
43	GND	44	GND
47	PR0_PRU1_PRU_R30_OUT[5]	48	GPIO0_02
49	SPI1_CLK	50	I2C_SCL0
53	PR0_PRU1_PRU_R30_OUT[6]	54	GPIO0_03
55	SPI1_SOMI	56	I2C_SDA0
59	PR0_PRU1_PRU_R30_OUT[8]	60	GPIO0_04
61	SPI1_SIMO	62	GND
65	PR0_PRU1_PRU_R30_OUT[11]	66	GPIO0_05
67	SPI1_SCS0	68	PR1_UART0TXD
71	PR0_PRU1_PRU_R30_OUT[12]	72	GPIO0_06
73	SPI1_SCS1	74	
77	PR0_PRU1_PRU_R30_OUT[13]	78	GPIO0_07
79	GND	80	PR1_ECAP0_ECAP_SYNCIN
83	PR0_PRU1_PRU_R30_OUT[14]	84	GPIO0_08
85	PR0_EDC_LATCH0_IN	86	PR1_ECAP0_ECAP_SYNCOUT
89	PR0_PRU1_PRU_R30_OUT[9]	90	GPIO0_09
91	PR0_EDC_LATCH1_IN	92	GND
95	PR0_PRU1_PRU_R30_OUT[10]	96	PR1_PRU0_GPO7
97	PR0_EDC_SYNC0_OUT	98	PR1_ECAP0_ECAP_CAPIN_APWM_O
101	PR0_PRU1_PRU_R30_OUT[15]	102	GND
103	PR0_EDC_SYNC1_OUT	104	PR0_ECAP0_ECAP_CAPIN_APWM_O
107	PR0_PRU1_PRU_R30_OUT[16]	108	GND
109	GND	110	GND
113	GND	114	GND
115	GND	116	GND
119	GND	120	GND

3.3.5 PCIe Edge Connector (J7)

The K2G ICE includes a x1 PCI Express endpoint connector capable of insertion into a PCI Express backplane connector. The K2G ICE is not compliant with the PCI Express Card Electromechanical Specification and is not designed to be inserted into a personal computer.

The K2G ICE does not include an onboard 100-MHz PCIe reference clock. If the PCIe interface is active, a 100-MHz clock must be present on pins A13 and A14 for proper operation. While the K2G SoC can support both root complex and endpoint operation, this EVM is only designed to act as an endpoint.

The PCIe backplane specification includes +12 V and +3.3 V to power cards inserted into the connector. The +12 V from the PCIe backplane can be used to power the K2G ICE. If +12 V is present on the backplane connector, there is no need to connect a power source to the DC jack (J6). If both voltage sources are present, the power supply uses the higher of the two voltages.

Table 10. PCI Express Edge Connector (J7)

Pin	Side B		Side A	
	Signal name	Description	Signal name	Description
1	V12_0D	+12 V from connector	PRESENTn	Backplane presence detect
2	V12_0D	+12 V from connector	V12_0D	+12 V from connector
3	V12_0D	+12 V from connector	V12_0D	+12 V from connector
4	DGND	ground	DGND	ground
5	PCIE_SMB_CLK	System management bus clock	nc	no connect
6	PCIE_SMB_DATA	System management bus data	nc	no connect
7	DGND	ground	nc	no connect
8	V3_3_PCIE	+3.3 V from connector	nc	no connect
9	nc	no connect	V3_3_PCIE	+3.3 V from connector
10	V3_3AUX_PCIE	+3.3 V auxiliary from connector	V3_3_PCIE	+3.3 V from connector
11	PCIE_WAKEn_CONN	Test point	PERST_CON	Reset from connector
Mechanical Key				
12	nc	no connect	DGND	ground
13	DGND	ground	PCIE_REFCLKP	100-MHz ref clock in (P)
14	K2G_PCIE_RXn0	Transmit pair from RC (n)	PCIE_REFCLKN	100-MHz ref clock in (N)
15	K2G_PCIE_RXp0	Transmit pair from RC (p)	DGND	ground
16	DGND	ground	K2G_PCIE_TXp0	Receive pair from RC (p)
17	PRESENTn	Backplane presence detect	K2G_PCIE_TXn0	Receive pair from RC (n)
18	DGND	ground	DGND	ground

3.3.6 RJ45 Gigabit Ethernet (J10)

The K2G ICE a single RJ45 connector with magnetics for the gigabit Ethernet interface. It is connected to the Ethernet PHY transceiver, as defined by the PHY data manual. The connector also includes two integrated LEDs indicating the speed and the activity. The pinout of the connector is shown in Table 11.

Table 11. Gigabit Ethernet (J10)

Pin	Signal	Description
1	DGND	Ground
2		No connect
3	ETHER0_D3P	Differential Transmit/Receive Pair 3
4	ETHER0_D3N	
5	ETHER0_D2P	Differential Transmit/Receive Pair 2
6	ETHER0_D2N	
7	ETHER0_D1P	Differential Transmit/Receive Pair 1
8	ETHER0_D1N	
9	ETHER0_D0P	Differential Transmit/Receive Pair 0
10	ETHER0_D0N	
11	PHY_LED_ACTn	Activity LED
12	DGND	Ground
13	DGND	Ground
14	PHY_LED_100n	Speed LED

3.3.7 Stacked RJ45 10/100 Ethernet (J8 and J9)

The K2G ICE has two stacked RJ45 connectors with magnetics for the 10/100 industrial Ethernet interfaces. It is connected to the four Ethernet PHY transceivers, as defined by the PHY data manual. Each connector also includes four integrated LEDs indicating the speed and the activity. J9 provides the two Ethernet interfaces provided by PRU0, and J8 provides the two Ethernet interfaces provided by PRU1. The pinout for connector J9 is shown in Table 12 and the pinout for connector J8 is shown in Table 13.

Table 12. Stacked PRU0 Ethernet (J9)

Pin	Signal	Description	Pin	Signal	
A1	PRU0MII0_RDP	Ethernet Receive Differential Pair	B1	PRU0MII1_RDP	Ethernet Receive Differential Pair
A2	PRU0MII0_RDN		B2	PRU0MII1_RDN	
A3	+3.3 V		B3	+3.3 V	
A4			B4		
A5			B5		
A6			B6		
A7			B7		
A8	PRU0MII0_TDP	Ethernet Transmit Differential Pair	B8	PRU0MII1_TDP	Ethernet Transmit Differential Pair
A9	PRU0MII0_TDN		B9	PRU0MII1_TDN	
A10			B10		
15	+3.3 V		11	+3.3 V	
16	PRU0MII0_LINKLED	Link LED	12	PRU0MII1_LINKLED	Link LED
17	+3.3 V		13	+3.3 V	
18	PRU0MII0_SPEEDLED	Speed LED	14	PRU0MII1_SPEEDLED	Speed LED

Table 13. Stacked PRU1 Ethernet (J8)

Pin	Signal	Description	Pin	Signal	
A1	PRU0MII2_RDP	Ethernet Receive Differential Pair	B1	PRU0MII3_RDP	Ethernet Receive Differential Pair
A2	PRU0MII2_RDN		B2	PRU0MII3_RDN	
A3	+3.3 V		B3	+3.3 V	
A4			B4		
A5			B5		
A6			B6		
A7			B7		
A8	PRU0MII2_TDP	Ethernet Transmit Differential Pair	B8	PRU0MII3_TDP	Ethernet Transmit Differential Pair
A9	PRU0MII2_TDN		B9	PRU0MII3_TDN	
A10			B10		
15	+3.3 V		11	+3.3 V	
16	PRU0MII2_LINKLED	Link LED	12	PRU0MII3_LINKLED	Link LED
17	+3.3 V		13	+3.3 V	
18	PRU0MII2_SPEEDLED	Speed LED	14	PRU0MII3_SPEEDLED	Speed LED

3.3.8 MicroSD Card Cage (J12)

The K2G ICE includes a card cage for a microSD card. The microSD is used as storage for application code. The pinout for connector J12 is shown in Table 14.

Table 14. microSD Card Cage (J12)

Pin	Signal	Description
1	MMC_D2	SD Data bit2
2	MMC_D3	SD Data bit3
3	MMC_CMD	SD Command bit
4	VDD_3V3	3.3V
5	MMC_CLK	SD Clock
6	DGND	ground
7	MMC_D0	SD Data bit0
8	MMC_D1	SD Data bit1
9	DGND	ground
10	SD_DETECT	SD card detect
11	DGND	ground
12	DGND	ground
13	DGND	ground
14	DGND	ground

3.3.9 LCD (J11)

The K2G ICE includes a 96×16 pixel LCD display connected with a flex PCB cable. The flex PCB connector (J11) interfaces with this cable. The pinout for connector J11 is shown in Table 15.

Table 15. Flex PCB Connector for LCD (J11)

Pin	Signal	Description
1	VCC_LCD	Supply for OEL panel generated on the display. Connect a capacitor between this pin and ground.
2	VCOMH	Voltage high level for COM signal generated on the display. Connect a capacitor between this pin and ground.
3	IREF	Current reference for brightness adjustment. Connect a resistor between this pin and ground. Resistor value adjusts the brightness. `12.5 µA maximum.
4	I2C_SDA1	I2C1 data for control
5	I2C_SCL1	I2C1 clock for control
6	RESn	Reset to LCD
7	VDD_3V3	3.3 V
8	DGND	Ground
9		No connect
10	VDDB	Switched 3.3 V
11	C1N	Negative terminal of flying inverting capacitor
12	C1P	Positive terminal of flying inverting capacitor
13	C2N	Negative terminal of flying inverting capacitor
14	C2P	Positive terminal of flying inverting capacitor

3.3.10 Current Measurement (J14)

The K2G ICE includes a 5-pin header designed for internal use. The connector provides an I2C interface to the four INA226 current/power monitor components connected to the four main power rails. The pinout for connector J14 is shown in Table 16.

Table 16. Current Measurement Connector (J14)

Pin	Signal	Description
1	PMBUS_SDA	I2C data
2	PMBUS_SDA	I2C clock
3	DGND	ground
4		No connect
5		No connect

3.3.11 SOC I2C2 Header (J16 and J17)

The K2G ICE includes two 2-pin headers used to short the I2C2 bus from the SOC to the PMBUS I2C interface for the INA226 current/power measurement components. These headers do not have shunts installed by default. The pinout for header J16 is shown in Table 17, and the pinout for header J17 is shown in Table 18.

Table 17. I2C2 Clock Header (J16)

Pin	Signal	Description
1	I2C_SCL2	shunt in – connects the PMBUS and I2C2 clocks shunt out – isolates the PMBUS and I2C2 clocks
2	PMBUS_SCL	

Table 18. I2C2 Data Header (J17)

Pin	Signal	Description
1	I2C_SDA2	shunt in – connects the PMBUS and I2C2 data shunt out – isolates the PMBUS and I2C2 data
2	PMBUS_SDA	

3.3.12 SYSCLKSEL Header (J3)

The K2G ICE includes two 2-pin headers used to select the source of the system clock for the K2G. If a shunt is installed on J2, the SYSCLKSEL configuration signal for the K2G is pulled low, which selects the internal HF oscillator as the clock source for the K2G. If the shunt is not installed, the external 25-MHz clock generator connected to the SYSCLKP and SYSCLKN is used as the system clock by the K2G. The pinout for header J3 is shown in Table 19.

Table 19. SYSCLKSEL Header (J3)

Pin	Signal	Description
1	SYSCLKSEL	shunt in – internal HF oscillator used for 24-MHz system clock shunt out – external 25-MHz clock generator used for system clock
2	1K resistor to ground	

3.3.13 VINPUT/VMAIN Testpoint Header (J15)

The K2G ICE includes two 2-pin headers used as test measurement accesses for the input voltage to the board, and the voltage after the overvoltage protection circuit. A shunt should never be installed on J15. The pinout for header J15 is shown in Table 20.

Table 20. VINPUT/VMAIN Testpoint Header (J15)

Pin	Signal	Description
1	VINPUT	+12-V to +24-V input voltage
2	VMAIN	+12-V to +24-V voltage after overvoltage protection

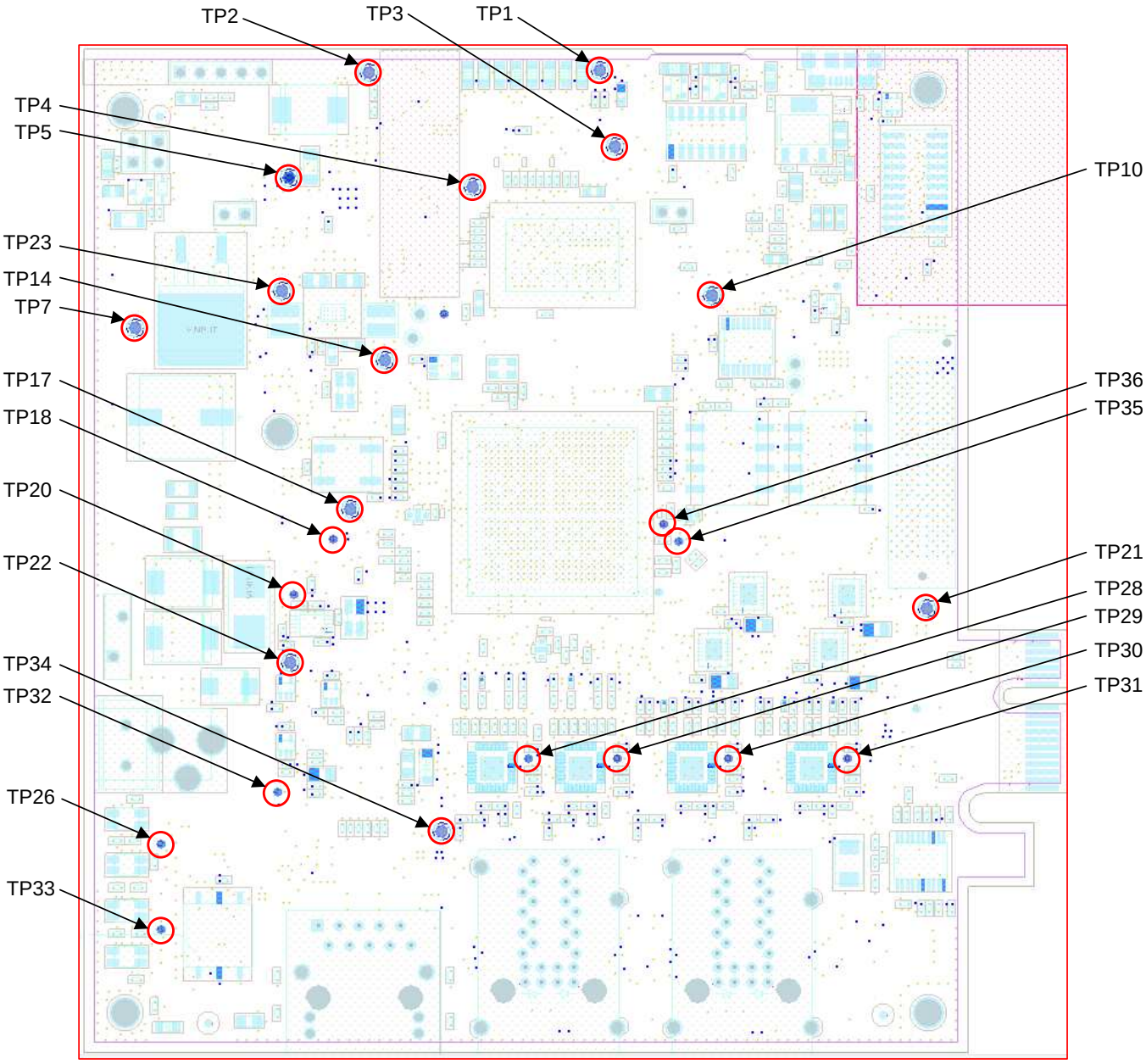
3.4 Test Points

The EVMK2G board has several test points to signals of interest on the board, as listed in Table 21 and shown in Figure 36.

Table 21. Test Points

Test Point	Signal	PCB Side	Description
TP1	DGND	TOP	Ground
TP2	VCC_LCD	TOP	Backlight voltage for LCD (generated internally)
TP3	VREF_DDR	TOP	0.675-V DDR3L reference voltage
TP4	VDDS_DDR	TOP	1.375 DDR3L I/O voltage
TP5	VDD_3V3	TOP	3.3-V I/O voltage
TP7	VINPUT	TOP	+12-V to +24-V input voltage
TP9	SUSPEND#	TOP	SUSPEND# signal from FTDI FT2232HL
TP10	RESETZ	TOP	RESETn signal to SOC
TP11	RSV3	TOP	reserved
TP12	DDR3_RST	TOP	DDR3 Reset out signal
TP13	RSV4	TOP	reserved
TP14	VDD_0V9	TOP	0.9-V core voltage
TP15	RSV9	TOP	reserved
TP17	VDD_1V8	TOP	1.8-V I/O Voltage
TP18	SYSCLKOUT	TOP	SYSCLKOUT (core clock /6)
TP19	RSV5	TOP	reserved
TP20	RMIIREFCLK	TOP	RMII reference clock out (not used)
TP21	DGND	TOP	Ground
TP22	DGND	TOP	Ground
TP23	PORz	TOP	PORn signal to SoC
TP24	RSV8	TOP	reserved
TP25	PCIE_WAKEn_CONN	TOP	PCIE_WAKEn signal on PCIE connector (J7.B11)
TP26	LED_11	TOP	LED_11 control signal
TP27	RSV7	TOP	reserved
TP28	PR1_MII0_25MHzCLK	TOP	10/100 PHY 25-MHz reference clock (U16)
TP29	PR1_MII1_25MHzCLK		10/100 PHY 25-MHz reference clock (U17)
TP30	PR0_MII0_25MHzCLK		10/100 PHY 25-MHz reference clock (U18)
TP31	PR0_MII1_25MHzCLK		10/100 PHY 25-MHz reference clock (U19)
TP32	CLK_OUT	TOP	Gig PHY reference clock out
TP33	LED_4	TOP	LED_4 control signal
TP34	DGND	TOP	Ground
TP35	OBSCLK_P	TOP	Observation clock output (positive)
TP36	OBSCLK_N	TOP	Observation clock output (negative)

Figure 36. Test Point Diagram



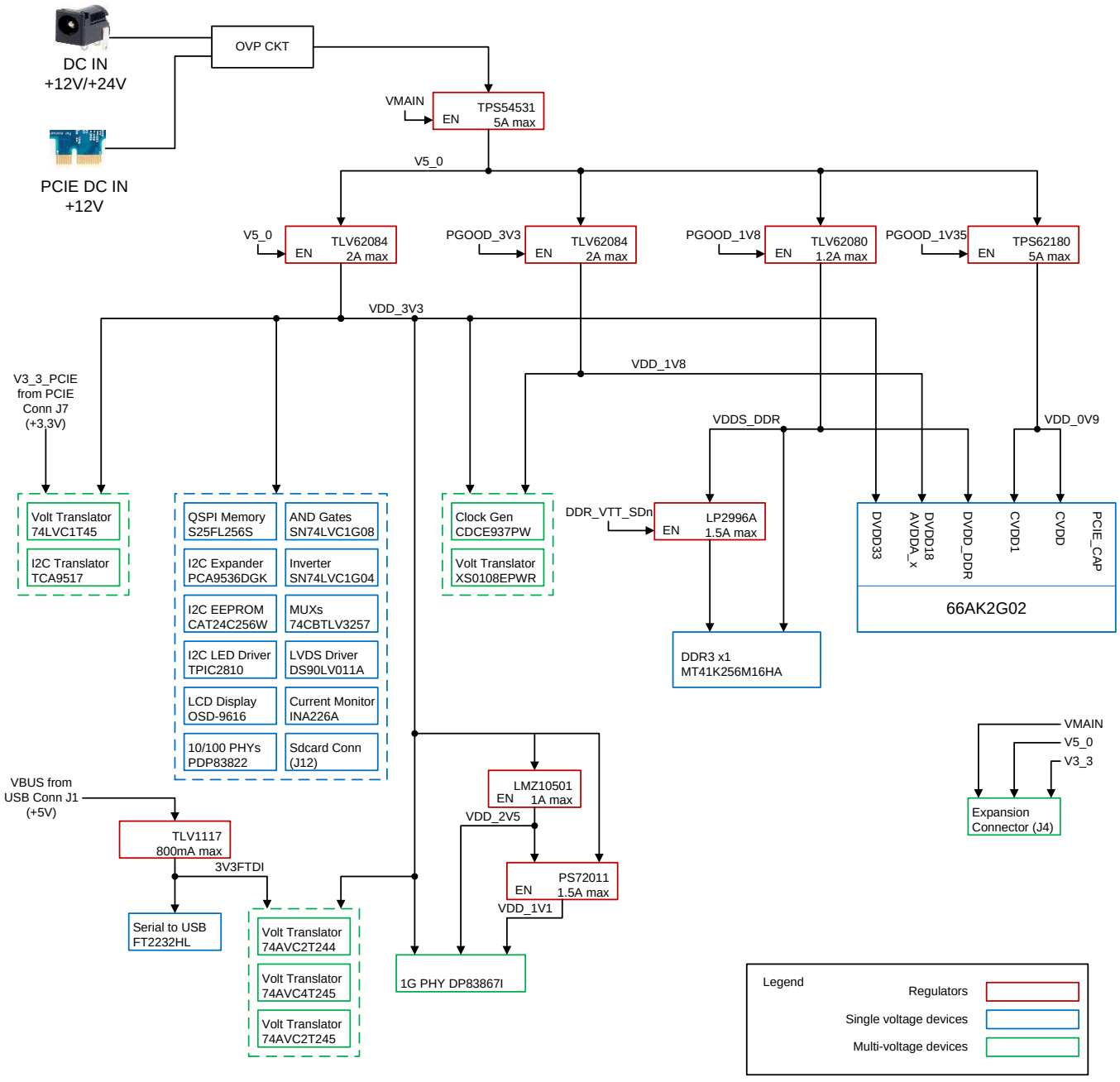
4 ICE EVM Power Requirements

This section describes the power supply used for the K2G ICE and the main power supply requirements.

4.1 Power Distribution Diagram

Figure 37 shows the power distribution for the K2G ICE.

Figure 37. Power Distribution Diagram



4.2 Power Supply Calculation

Table 22 provides the maximum current requirements for the K2G ICE.

Table 22. ICE EVM Power Consumption

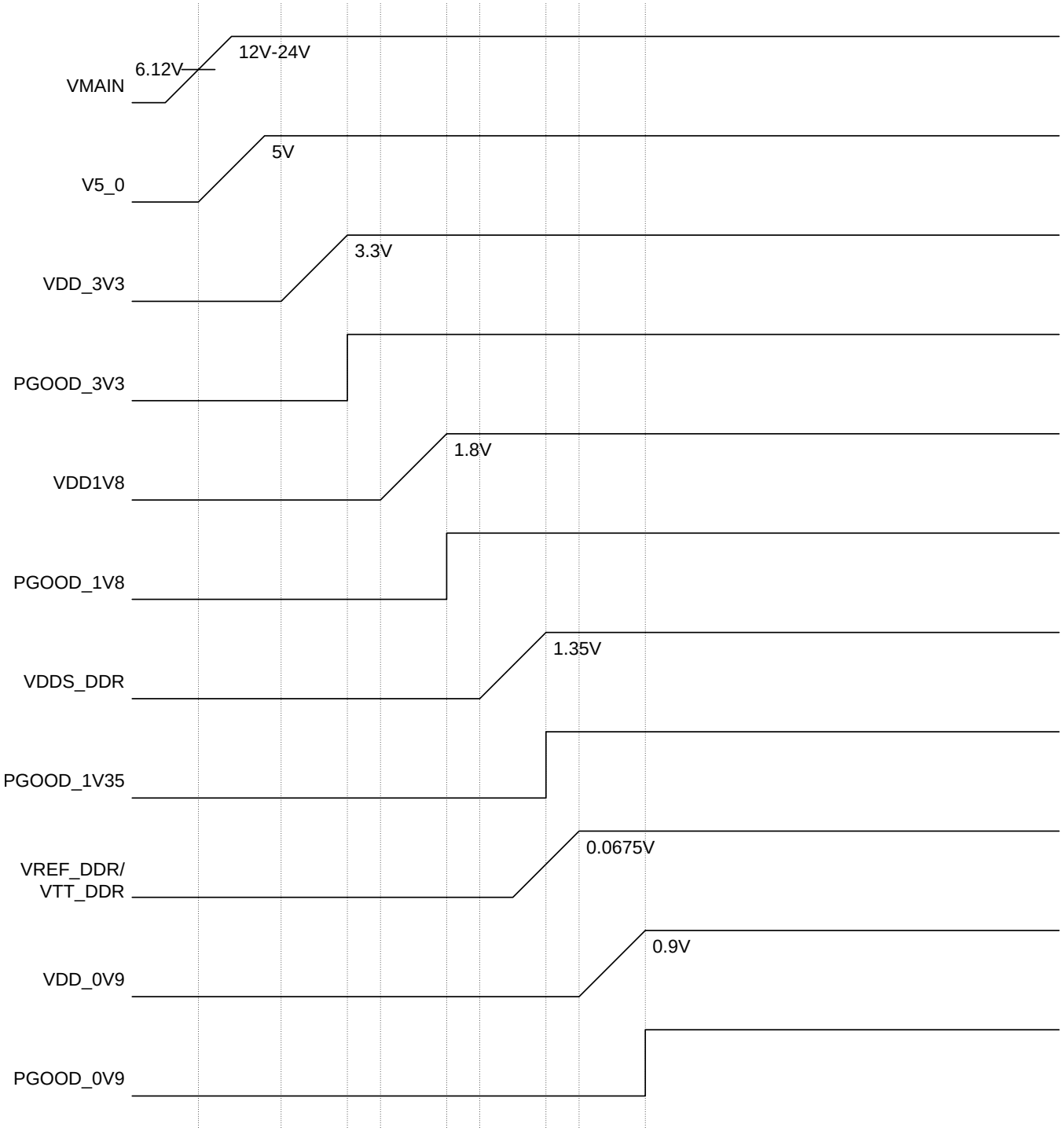
Qty	Description	Manufacturers Part Number	Max Current Vmain (mA)
13	LED Green SMD 20-mA 2-V 0805	5988170107F	89.375
4	LED RedGreenBlue tricolor 20-mA 1.9/2.1-V 1210 smd	SM1210RGB	82.5
1	LED ALINGAP RED CLEAR 0805 SMD	5988110107F	6.875
1	Connector RJ-45 jack with mag and LED gigabit	LPJG16314A4NL	13.75
1	Connector 0.5-mm pitch, 14 Pin, FPC	10051922-1410ELF	6.875
1	Connector compact low-profile push-type microSD	SCHA5B0200	13.75
1	High density 20×6 female connector 120 POS	SEAF-20-05.0-S-06-A-2-K-TR	480
2	RJ45 with LED, stacked vertical	ARJ21A-MBSD-A-B-EMU2	55
1	MicroSD card		31.0077
7	Dual transistor NPN 50 V 100 mA	DMC564040R	0.48125
3	IC MOSFET N-CHANNEL 50-V 200-mA SOT23-3	BSS138-7-F	0.000515625
1	IC POWER MOSFET N-CHANNEL D2PAK	SUM60N10-17-E3	0.0859375
1	TRANSISTOR NPN 50-V 100-mA SOT23-3	MMUN2214LT1G	0.0859375
8	4-bit 1-4 FET Mux/Demux	SN74CBTLV3257RGYR	0.825
7	Single logic AND Gate	SN74LVC1G08DCKR	60.15625
1	IC LOW INPUT VOLTAGE CURRENT LIMITED LOAD SWITCH SC70-5	TPS22945DCKR	0.275
1	IC TRANSLATOR BIDIRECTIONAL VOLTAGE-LEVEL 8-BIT TSSOP20	TXS0108EPWR	17.1875
4	IC BI-DIRECTIONAL CURRENT MONITER MSOP10	INA226AIDGSR	1.375
1	IC µP SUPERVISOR CIRCUITS SOT23-6	TPS3808G09DBVR	0.0034375
1	IC SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER SOT-23	SN74LVC1T45DBVR	8.25
1	IC CONTROLLER HIGH-SIDE PROTECTION VSSOP10	LM5060MM/NOPB	0.6875
2	IC DUAL-BIT DUAL SUPPLY BUS TRANSCEIVER QFN10	SN74AVC2T245RSWR	8.25
1	IC 2-CHANNEL I2C BUS REPEATER VSSOP8	TCA9517DGKR	2.0625
4	Industrial Ethernet 10/100 Mb/s PHY transceiver	PDP83822RHBT	96.25
1	ESD protection array 2Chan +-15 kV	TPD2E001DRLR	0
1	PROGRAMMABLE 3-PLL VCXO CLOCK SYNTHESIZER with 7 outputs	CDCE937PW	10.3125
1	DDR termination regulator	LP2996AMR/NOPB	0.171875
1	USBHS Dual UART/FIFO	FT2232HL-REEL	24.0625
1	E2PROM 2Kbit 3-Mhz memory	93LC56B-I/SN	0.6875
1	Dual buffer with open-drain outputs	SN74LVC2G07DCKR	0.171875
1	8-bit LED driver with I2C interface	TPIC2810DR	0.34375
1	2-bit undirectional voltage translator	SN74AVC2T244DQMR	0.006875
1	Single two-input positive NAND	SN74LVC1G00DCKR	34.375
1	Bus transceiver 4-bit voltage translator	SN74AVC4T245PW	34.375
1	Quad serial NOR flash memory 256Mb 3.3 V	S25FL256SAGMFIR01	34.375
1	DDR3 SDRAM 4 Gb (256Mx16) 1.35 V	MT41K256M16HA-125 IT:E	28.125
1	Ethernet PHY Gb/100Mb/10Mb	DP83867IRPAPT	36.45833333
2	ESD protection device 2 DiffPair Chan +-15 kV	TPD4E05U06DQAR	0.006875
1	I2C to I/O expander 4 bit	PCA9536DGKR	55
1	EEPROM 256Kb I2C SOIC8	CAT24C256WI-G	1.03125
1	LVDS interface IC SGL HIGH SPD DIFF DRVR	DS90LV011ATMF/NOPB	3.4375
1	IC SINGLE INVERTER GATE SC70-5	SN74LVC1G04DCKR	8.25
1	Cortex A15 with C66X SOC 66AK2G02	66AK2G02_ZBB	480.54

	Maximum
Total maximum current consumption in mA	1726.839361
Total maximum power consumption for 12-V supply in mW	20722.0723

4.3 Power Sequencing

Figure 38 shows the power sequencing the K2G ICE. This diagram represents the sequencing implemented on the K2G ICE. The power sequencing for the K2G is represented in the data manual for the device. Refer to the data manual when designing power sequencing for this device.

Figure 38. Power Sequencing



5 Comparison to K2G General Purpose EVM

The K2G ICE uses a subset of the capabilities of the K2G specifically targeting industrial communications applications. The K2G GP EVM provides a platform designed to be used in a number of different applications. This section provides a comparison between the GP EVM and the ICE EVM.

Table 23. K2G GP EVM and ICE EVM Comparison

Interface	GP EVM	ICE EVM
Power	+12 V in from J3. Uses TPS659118 PMIC. Separate supplies for CVDD and CVDD1. AVS capable.	+12 V to +24 V in from either J6 or PCIE edge connector. Uses discrete power supplies. Common supply for CVDD and CVDD1. Fixed voltage.
JTAG	Onboard XDS200	Onboard XDS100v2
SYSCLK	Internal – 24-MHz crystal External – 24-MHz from CDCM6208 clock generator	Internal – 24-MHz crystal External – 25-MHz from CDCE937PW clock generator
DDRCLK	Internal – based on SYSCLK External – 100-MHz from CDCM6208 clock generator	Internal – Based on SYSCLK
PCIECLK	100 MHz from CDCM6208 clock generator	100 MHz from PCIE edge connector
USBCLK	Internal – based on SYSCLK	Internal – based on SYSCLK
AUDIOOSC	22.5792-MHz crystal	Not present
CPTSREFCLK	250 MHz from CDCM6208 clock generator	Not present
DDR3	32bits + ECC based on MT41K512M8RH-125	16bits based on MT41K256M16HA-125
MMC0	MicroSD card +3.3 V only	Pins used for PRU interface
MMC1	eMMC Flash memory	MicroSD card +3.3 V only
QSPI	512-Mbit QSPI memory	256-Mbit QSPI memory
SPI0	Expansion connector	Expansion connector
SPI1	SPI NOR flash	Expansion connector
SPI2	Audio expansion connector	Pins used for GPIO
SPI3	AVB clock generator	eCAP0
I2C0	Board ID memory, BMC,	Board ID memory, clock generator, expansion connector
I2C1	Audio clock generator, HDMI transmitter, audio codec, touchscreen, I/O expander, MLB connector, expansion connector	OLED display, LED drivers, I/O expander
I2C2	PMIC	INA226AIDGSR
UART0	USBtoUART CP2105	USBtoUART FT2232
UART1	COM8 connector	unused
UART2	BMC UART1	Pins used for GPIO
ICSS PR0	Pins used for McASP	MII for 10/100 Ethernet PHY0 and PHY1/ expansion connector
ICSS PR1	Pins used for GPIO	MII for 10/100 Ethernet PHY2 and PHY3
McASP	Audio expansion connector	Pins used for PRU interface
McBSP	Audio expansion connector	Pins used for PRU interface
DCAN	DCAN connectors	Pins used for PRU interface
DSS	LCD display/BOOTMODE	Pins used for GPIO/BOOTMODE
GPMC	NAND flash	Pins used for GPIO
USB	USB connectors	unused
PCIE	PCIE backplane connector – supports PCIE root complex and endpoint	PCIE endpoint cardedge connector – supports endpoint only

6 Known Issues

There are currently no known issues identified for the K2G ICE.

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